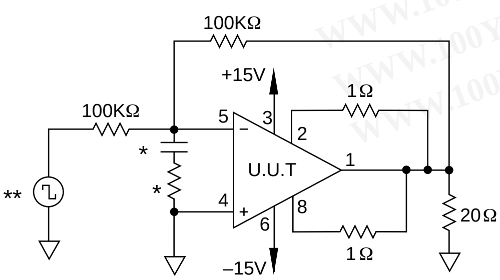
APEX MICROTECHNOLOGY

TABLE 4 GROUP A INSPECTION

PA61M/883

SG	PARAMETER	SYMBOL	TEMP.	POWER	TEST CONDITIONS	MIN	MAX	UNITS
1	Quiescent Current	I_Q	25°C	±32V	V_{IN} = 0, A_V = 100		10	mA
1	Input Offset Voltage	V_{OS}	25°C	±32V	V_{IN} = 0, A_V = 100		±6	mV
1	Input Offset Voltage	V_{OS}	25°C	±10V	V_{IN} = 0, A_V = 100		±10.4	mV
1	Input Offset Voltage	V_{OS}	25°C	±45V	V_{IN} = 0, A_V = 100		±8.6	mV
1	Input Bias Current, +IN	$+I_B$	25°C	±32V	V_{IN} = 0		±30	nA
1	Input Bias Current, –IN	$-I_B$	25°C	±32V	V_{IN} = 0		±30	nA
1	Input Offset Current	I_{OS}	25°C	±32V	V_{IN} = 0		±30	nA
3	Quiescent Current	I_Q	–55°C	±32V	V_{IN} = 0, A_V = 100		10	mA
3	Input Offset Voltage	V_{OS}	–55°C	±32V	V_{IN} = 0, A_V = 100		±11.2	mV
3	Input Offset Voltage	V_{OS}	–55°C	±10V	V_{IN} = 0, A_V = 100		±15.6	mV
3	Input Offset Voltage	V_{OS}	–55°C	±45V	V_{IN} = 0, A_V = 100		±13.8	mV
3	Input Bias Current, +IN	$+I_B$	–55°C	±32V	V_{IN} = 0		±115	nA
3	Input BiasCurrent, –IN	$-I_B$	–55°C	±32V	V_{IN} = 0		±115	nA
3	Input Offset Current	I_{OS}	–55°C	±32V	V_{IN} = 0		±115	nA
2	Quiescent Current	I_Q	125°C	±32V	V_{IN} = 0, A_V = 100		15	mA
2	Input Offset Voltage	V_{OS}	125°C	±32V	V_{IN} = 0, A_V = 100		±12.5	mV
2	Input Offset Voltage	V_{OS}	125°C	±10V	V_{IN} = 0, A_V = 100		±16.9	mV
2	Input Offset Voltage	V_{OS}	125°C	±45V	V_{IN} = 0, A_V = 100		±15.1	mV
2	Input Bias Current, +IN	$+I_B$	125°C	±32V	V_{IN} = 0		±70	nA
2	Input Bias Current, –IN	$-I_B$	125°C	±32V	V_{IN} = 0		±70	nA
2	Input Offset Current	I_{OS}	125°C	±32V	V_{IN} = 0		±70	nA
4	Output Voltage, I_O = 10A	V_O	25°C	±17V	R_L = 1Ω	10		V
4	Output Voltage, I_O = 80mA	V_O	25°C	±45V	R_L = 500Ω	40		V
4	Output Voltage, I_O = 4A	V_O	25°C	± 30V	R_L = 6Ω	24		V
4	Current Limits	I_{CL}	25°C	±15V	R_L = 6Ω, R_{CL} = 1Ω	.56	.88	A
4	Stability/Noise	E_N	25°C	±32V	R_L = 500Ω, A_V = 1, C_L = 10nF		1	mV
4	Slew Rate	SR	25°C	±32V	R_L = 500Ω	1	10	V/µs
4	Open Loop Gain	A_{OL}	25°C	±32V	R_L = 500Ω, F = 10Hz	96		dB
4	Common Mode Rejection	CMR	25°C	±15V	R_L = 500Ω, F = DC, V_{CM} = ±9V	74		dB
6	Output Voltage, I_O = 10A	V_O	–55°C	±17V	R_L = 1Ω	10		V
6	Output Voltage, I_O = 80mA	V_O	–55°C	±45V	R_L = 500Ω	40		V
6	Output Voltage, I_O = 4A	V_O	–55°C	±30V	R_L = 6Ω	24		V
6	Stability/Noise	E_N	–55°C	±32V	R_L = 500Ω, A_V = 1, C_L = 10nF		1	mV
6	Slew Rate	SR	–55°C	±32V	R_L = 500Ω	1	10	V/µs
6	Open Loop Gain	A_{OL}	–55°C	±32V	R_L = 500Ω, F = 10Hz	96		dB
6	CommonMode Rejection	CMR	–55°C	±15V	R_L = 500Ω, F = DC, V_{CM} = ±9V	74		dB
5	Output Voltage, I_O = 8A	V_O	125°C	±15V	R_L = 1Ω	8		V
5	Output Voltage, I_O = 80mA	V_O	125°C	±45V	R_L = 500Ω	40		V
5	Output Voltage, I_O = 4A	V_O	125°C	±30V	R_L = 6Ω	24		V
5	Stability/Noise	E_N	125°C	±32V	R_L = 500Ω, A_V = 1, C_L = 10nF		1	mV
5	Slew Rate	SR	125°C	±32V	R_L = 500Ω	1	10	V/µs
5	Open Loop Gain	A_{OL}	125°C	±32V	R_L = 500Ω, F = 10Hz	96		dB
5	Common Mode Rejection	CMR	125°C	±15V	R_L = 500Ω, F = DC, V_{CM} = ±9V	74		dB

BURN IN CIRCUIT



* These components are used to stabilize device due to poor high frequency characteristics of burn in board.

** Input signals are calculated to result in internal power dissipation of approximately 2.1W at case temperature = 125°C.

FEATURES
- WIDE SUPPLY RANGE — ±10 to ±45V
- HIGH OUTPUT CURRENT — ±10A Peak
- LOW COST — Class "C" output stage
- LOW QUIESCENT CURRENT — 3mA

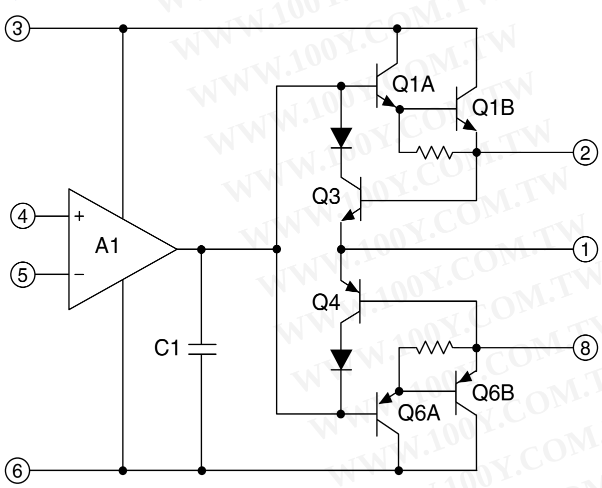
8-PIN TO-3
PACKAGE STYLE CE

APPLICATIONS
- PROGRAMMABLE POWER SUPPLY
- MOTOR/SYNCRO DRIVER
- VALVE AND ACTUATOR CONTROL
- DC OR AC POWER REGULATOR
- FIXED FREQUENCY POWER OSCILLATOR

DESCRIPTION
The PA61 and PA61A are high output current operational amplifiers designed to drive resistive, inductive and capacitive loads. Their complementary emitter follower output stage is the simple class C type and optimized for low frequency applications where crossover distortion is not critical. These amplifiers are not recommended for audio, transducer or deflection coil drive circuits above 1kHz or when distortion is critical. The safe operating area (SOA) is fully specified and can be observed for all operating conditions by selection of user programmable current limiting resistors. Both amplifiers are internally compensated for all gain settings. For continuous operation under load, mounting on a heatsink of proper rating is recommended.

This hybrid circuit utilizes thick film conductors, ceramic capacitors, and semiconductor chips to maximize reliability, minimize size, and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8-pin TO-3 package is electrically isolated and hermetically sealed. The use of compressible thermal washers and/or improper mounting torque voids the product warranty. Please see "General Operating Considerations".

EQUIVALENT SCHEMATIC



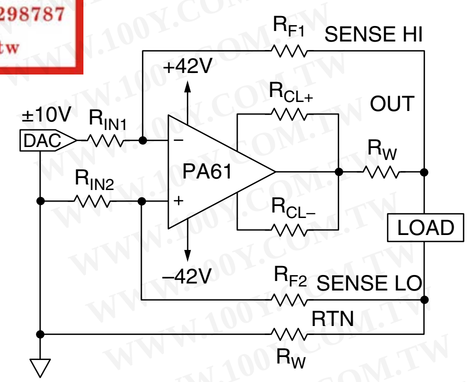
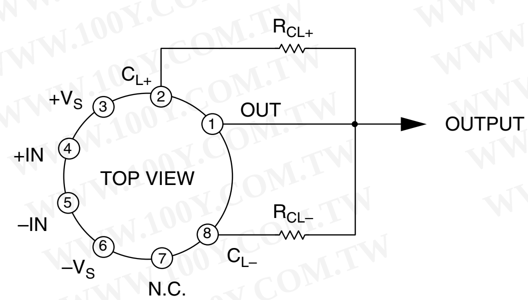


FIGURE 1. PROGRAMMABLE POWER SUPPLY WITH REMOTE SENSING

TYPICAL APPLICATION
Due to its high current drive capability, PA61 applications often utilize remote sensing to compensate IR drops in the wiring. The importance of remote sensing increases as accuracy requirements, output currents, and distance between amplifier and load go up. The circuit above shows wire resistance from the PA61 to the load and back to the local ground via the power return line. Without remote sensing, a 7.5A load current across only 0.05 ohm in each line would produce a 0.75V error at the load.

With the addition of the second ratio matched R_F/R_{IN} pair and two low current sense wires, IR drops in the power return line become common mode voltages for which the op amp has a very high rejection ratio. Voltage drops in the output and power return wires are inside the feedback loop. Therefore, as long as the Power Op Amp has the voltage drive capability to overcome the IR losses, accuracy remains the same. Application Note 7 presents a general discussion of PPS circuits.

EXTERNAL CONNECTIONS



ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$	90V
OUTPUT CURRENT, within SOA	10A
POWER DISSIPATION, internal	97W
INPUT VOLTAGE, differential	±37V
INPUT VOLTAGE, common mode	$\pm V_S$
TEMPERATURE, pin solder-10s	300°C
TEMPERATURE, junction[1]	200°C
TEMPERATURE RANGE, storage	–65 to +150°C
OPERATING TEMPERATURE RANGE, case	–55 to +125°C

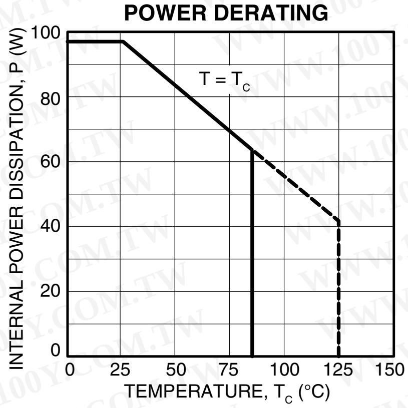
SPECIFICATIONS

PARAMETER	TEST CONDITIONS[2]	PA61 MIN	PA61 TYP	PA61 MAX	PA61A MIN	PA61A TYP	PA61A MAX	UNITS
INPUT								
OFFSET VOLTAGE, initial	T_C = 25°C		±2	±6		±1	±4	mV
OFFSET VOLTAGE, vs. temperature	Specified temperature range		±10	±65		*	±40	μV/°C
OFFSET VOLTAGE, vs. supply	T_C = 25°C		±30	±200		*	*	μV/V
OFFSET VOLTAGE, vs. power	T_C = 25°C		±20			*		μV/W
BIAS CURRENT, initial	T_C = 25°C		12	30		10	20	nA
BIAS CURRENT, vs. temperature	Specified temperature range		±50	±500		*	*	pA/°C
BIAS CURRENT, vs. supply	T_C = 25°C		±10			*		pA/V
OFFSET CURRENT, initial	T_C = 25°C		±12	±30		±5	±10	nA
OFFSET CURRENT, vs. temperature	Specified temperature range		±50			*		pA/°C
INPUT IMPEDANCE, DC	T_C = 25°C		200			*		MΩ
INPUT CAPACITANCE	T_C = 25°C		3			*		pF
COMMON MODE VOLTAGE RANGE[3]	Specified temperature range	$\pm V_S-5$	$\pm V_S-3$		*	*		V
COMMON MODE REJECTION, DC[3]	Specified temperature range	74	100		*	*		dB
GAIN								
OPEN LOOP GAIN at 10Hz	Full temp. range, full load	96	108		*	*		dB
GAIN BANDWIDTH PRODUCT at 1MHz	T_C = 25°C, full load		1			*		MHz
POWER BANDWIDTH	T_C = 25°C, I_O = 8A, V_O = $40V_{PP}$	10	16		*	*		kHz
PHASE MARGIN	Full temperature range		45			*		°
OUTPUT								
VOLTAGE SWING[3]	T_C = 25°C, I_O = 10A	$\pm V_S-7$	$\pm V_S-5$		$\pm V_S-6$	*		V
VOLTAGE SWING[3]	Full temp. range, I_O = 4A	$\pm V_S-6$	$\pm V_S-4$		*	*		V
VOLTAGE SWING[3]	Full temp. range, I_O = 68mA	$\pm V_S-5$			*			V
CURRENT	T_C = 25°C	±10			*			A
SETTLING TIME to .1%	T_C = 25°C, 2V step		2			*		μs
SLEW RATE	T_C = 25°C, R_L = 6Ω	1.0	2.8		*	*		V/μs
CAPACITIVE LOAD, unit gain	Full temperature range			1.5			*	nF
CAPACITIVE LOAD, gain>4	Full temperature range			SOA			*	
POWER SUPPLY								
VOLTAGE	Full temperature range	±10	±32	±45	*	*	*	V
CURRENT, quiescent	T_C = 25°C		3	10		*	*	mA
THERMAL								
RESISTANCE, AC, junction to case[4]	F > 60Hz		1.0	1.2		*	*	°C/W
RESISTANCE, DC, junction to case	F < 60Hz		1.5	1.8		*	*	°C/W
RESISTANCE, junction to air			30			*		°C/W
TEMPERATURE RANGE, case	Meets full range specification	–25	25	+85	*	*	*	°C

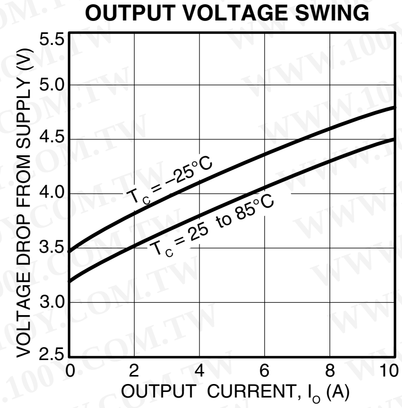
NOTES:
* The specification of PA61A is identical to the specification for PA61 in applicable column to the left.
1. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.
2. The power supply voltage for all specifications is the TYP rating unless noted as a test condition.
3. $+V_S$ and $-V_S$ denote the positive and negative supply rail respectively. Total V_S is measured from $+V_S$ to $-V_S$.
4. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.

CAUTION The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

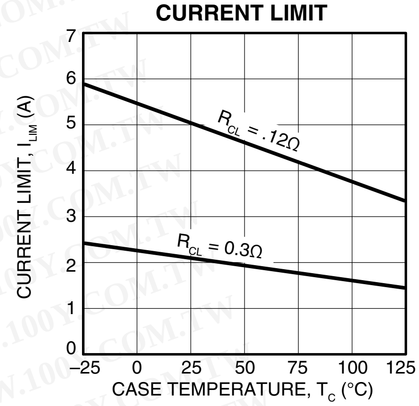
POWER DERATING



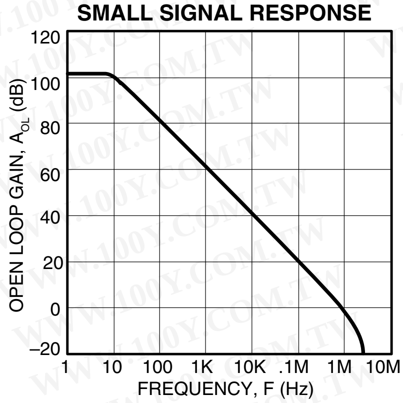
OUTPUT VOLTAGE SWING



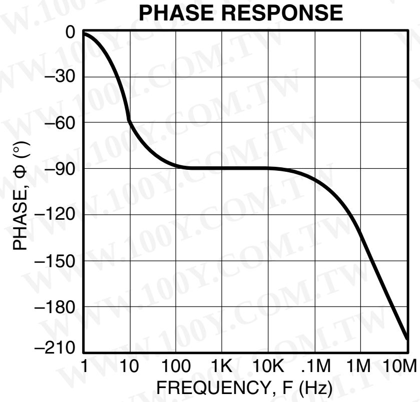
CURRENT LIMIT



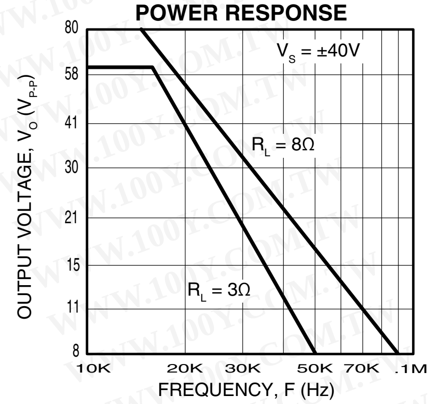
SMALL SIGNAL RESPONSE



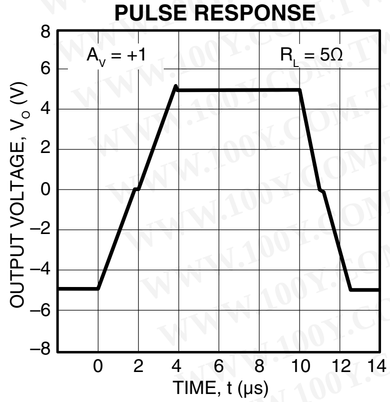
PHASE RESPONSE



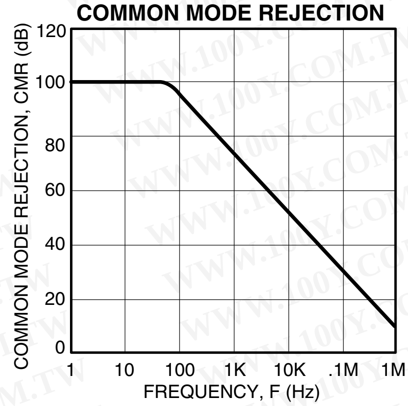
POWER RESPONSE



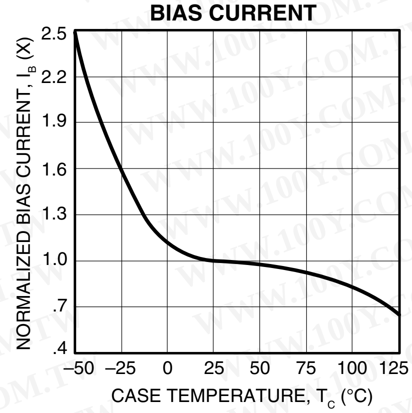
PULSE RESPONSE



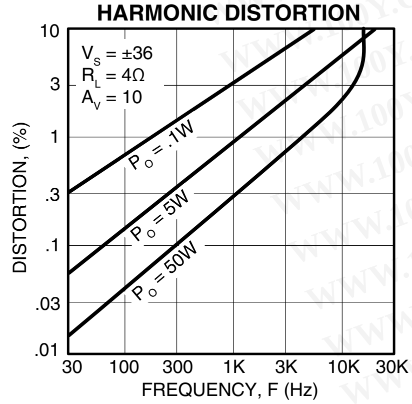
COMMON MODE REJECTION



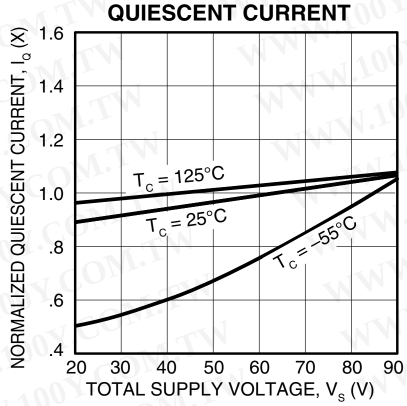
BIAS CURRENT



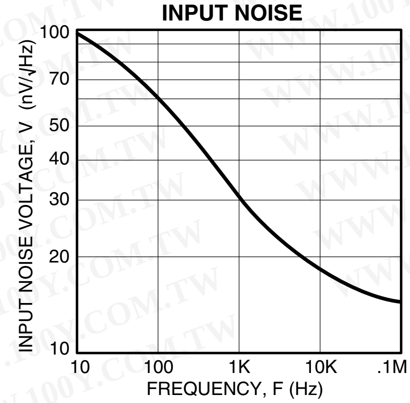
HARMONIC DISTORTION



QUIESCENT CURRENT



INPUT NOISE



GENERAL

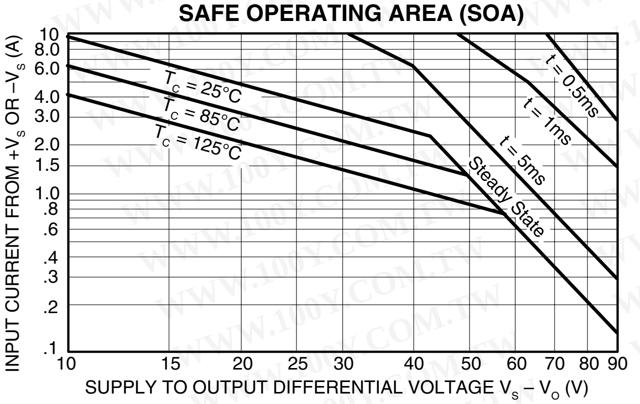
Please read Application Note 1 "General Operating Considerations" which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.apexmicrotech.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit and heat sink selection. The "Application Notes" and "Technical Seminar" sections contain a wealth of information on specific types of applications. Package outlines, heat sinks, mounting hardware and other accessories are located in the "Packages and Accessories" section. Evaluation Kits are available for most Apex product models, consult the "Evaluation Kit" section for details. For the most current version of all Apex product data sheets, visit www.apexmicrotech.com.

SAFE OPERATING AREA (SOA)

The output stage of most power amplifiers has 3 distinct limitations:

1. The current handling capability of the transistor geometry and the wire bonds.
2. The second breakdown effect which occurs whenever the simultaneous collector current and collector-emitter voltage exceeds specified limits.
3. The junction temperature of the output transistors.

SAFE OPERATING AREA (SOA)



The SOA curves combine the effect of all limits for this Power Op Amp. For a given application, the direction and magnitude of the output current should be calculated or measured and checked against the SOA curves. This is simple for resistive loads but more complex for reactive and EMF generating loads. The following guidelines may save extensive analytical efforts.

1. Under transient conditions, capacitive and dynamic* inductive loads up to the following maximum are safe:

	CAPACITIVE LOAD		INDUCTIVE LOAD	
V_S	I_{LIM} = 5A	I_{LIM} = 10A	I_{LIM} = 5A	I_{LIM} = 10A
45V	200 F	150 F	8mH	2.8mH
40V	400 F	200 F	11mH	4.3mH
35V	800 F	400 F	20mH	5.0mH
30V	1600 F	800 F	35mH	6.2mH
25V	5.0mF	2.5mF	50mH	15mH
20V	10mF	5.0mF	400mH	20mH
15V	20mF	10mF	**	100mH

* If the inductive load is driven near steady state conditions, allowing the output voltage to drop more than 8V below the supply rail with I_{LIM} = 10A or 15V below the supply rail with I_{LIM} = 5A while the amplifier is current limiting, the inductor should be capacitively coupled or the current limit must be lowered to meet SOA criteria.

** Second breakdown effect imposes no limitation but thermal limitations must still be observed.

2. The amplifier can handle any EMF generating or reactive load and short circuits to the supply rail or shorts to common if the current limits are set as follows at T_C=85°C.

±V_S	SHORT TO V_S ± C, L, OR EMF LOAD	SHORT TO COMMON
45V	0.1A	1.3A
40V	0.2A	1.5A
35V	0.3A	1.6A
30V	0.5A	2.0A
25V	1.2A	2.4A
20V	1.5A	3.0A
15V	2.0A	4.0A

These simplified limits may be exceeded with further analysis using the operating conditions for a specific application.

3. The output stage is protected against transient flyback. However, for protection against sustained, high energy flyback, external fast-recovery diodes should be used.

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