

FEATURES

- HIGH VOLTAGE — 400V (± 200 V)
- LOW QUIESCENT CURRENT — 10mA
- HIGH OUTPUT CURRENT — 200mA
- PROGRAMMABLE CURRENT LIMIT
- HIGH SLEW RATE — 300V/ μ s

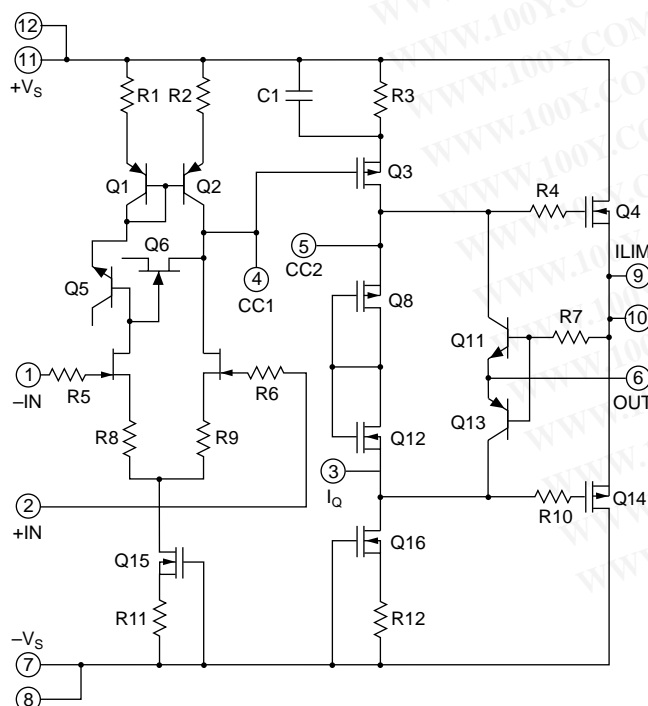
APPLICATIONS

- PIEZOELECTRIC POSITIONING
- HIGH VOLTAGE INSTRUMENTATION
- ELECTROSTATIC TRANSDUCERS
- PROGRAMMABLE POWER SUPPLIES UP TO 390V

DESCRIPTION

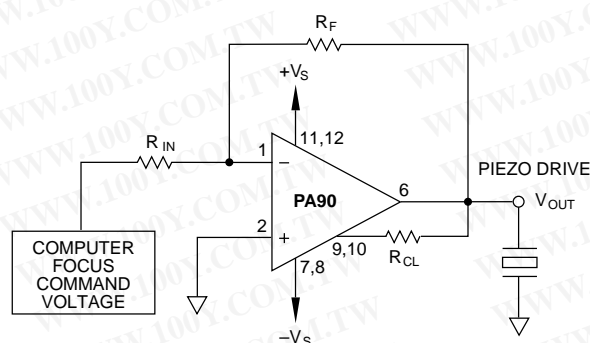
The PA90 is a high voltage, low quiescent current MOSFET operational amplifier designed as a low cost solution for driving continuous output currents up to 200mA and pulse currents up to 350mA. The safe operating area (SOA) has no second breakdown limitations and can be observed for all type loads by choosing an appropriate current limiting resistor. The MOSFET output stage is biased AB for linear operation. External compensation provides flexibility in choosing bandwidth and slew rate for the application. APEX's Power SIP package uses a minimum of board space allowing for high density circuit boards. The 12-pin PowerSIP package is electrically isolated.

EQUIVALENT SCHEMATIC



12-pin SIP
PACKAGE STYLE DP

TYPICAL APPLICATION



LOW POWER, PIEZOELECTRIC POSITIONING

Piezo positioning may be applied to the focusing of segmented mirror systems. The composite mirror may be composed of hundreds of elements, each requiring focusing under computer control. In such complex systems the PA90 reduces the costs of power supplies and cooling with its advantages of low cost and low quiescent power consumption while increasing circuit density with the SIP package.

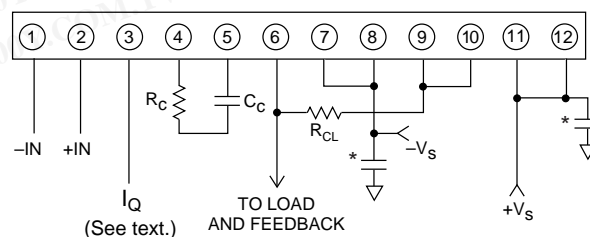
PHASE COMPENSATION

GAIN	C_c^*	R_c
≥ 1	68pF	100 Ω
≥ 5	10pF	100 Ω
≥ 10	4.7pF	0 Ω
≥ 30	NONE	0 Ω

* C_c To be rated for the full supply voltage
+V to -Vs. Use NPO ceramic (COG) type.

EXTERNAL CONNECTIONS

Package: SIP03



* Bypassing required.

PA90

ABSOLUTE MAXIMUM RATINGS SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$	400V
OUTPUT CURRENT, source, sink, peak	350mA, within SOA
POWER DISSIPATION, continuous @ $T_C = 25^\circ\text{C}$	30W
INPUT VOLTAGE, differential	$\pm 20\text{V}$
INPUT VOLTAGE, common mode	$\pm V_S$
TEMPERATURE, pin solder - 10s max.	260°C
TEMPERATURE, junction ²	150°C
TEMPERATURE RANGE, storage	-40 to $+85^\circ\text{C}$
OPERATING TEMPERATURE RANGE, case	-25 to $+85^\circ\text{C}$

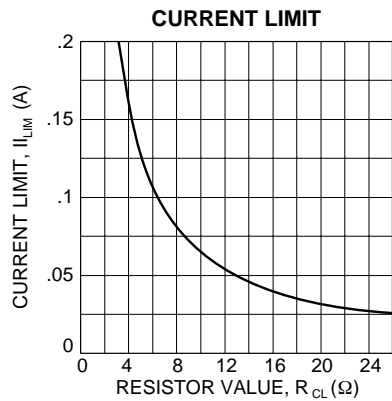
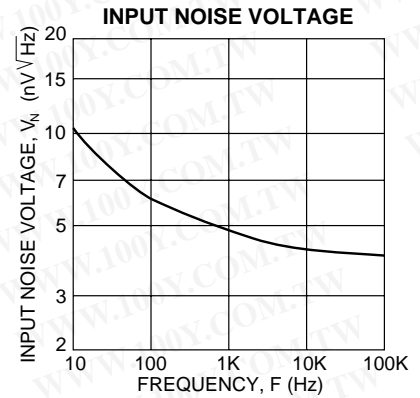
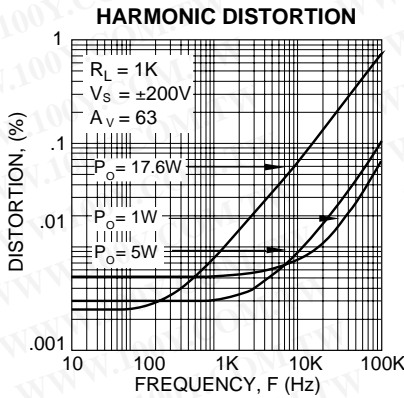
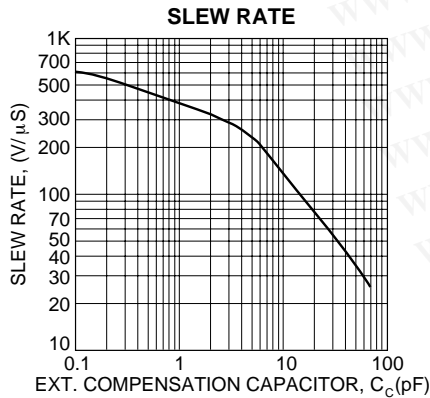
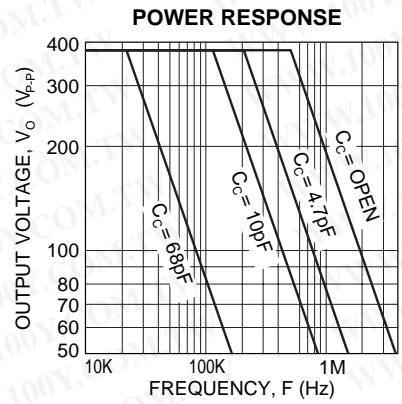
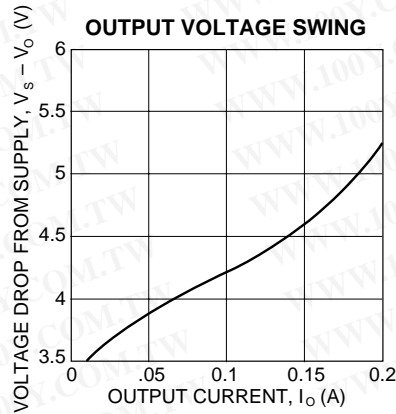
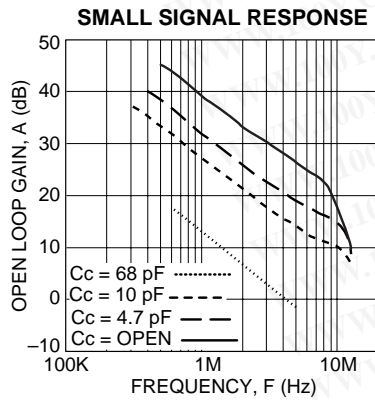
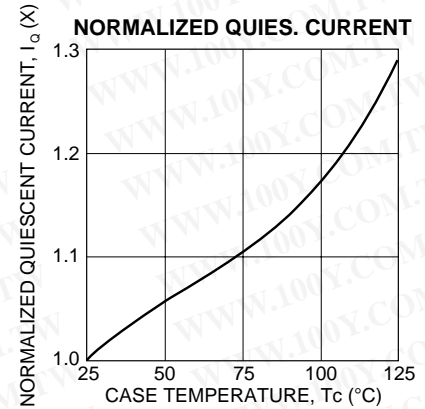
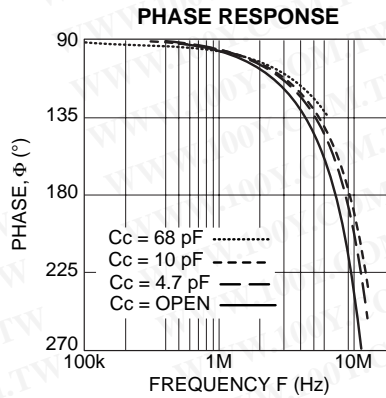
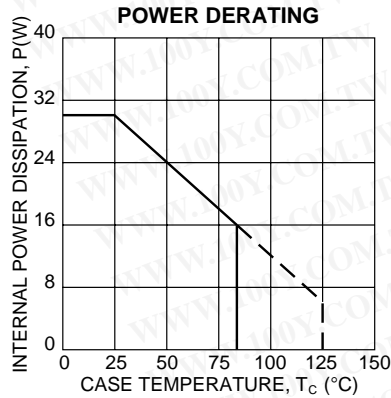
SPECIFICATIONS

PARAMETER	TEST CONDITIONS ¹	MIN	TYP	MAX	UNITS
INPUT					
OFFSET VOLTAGE, initial	Full temperature range		.5	2	mV
OFFSET VOLTAGE, vs. temperature			15	50	μV/°C
OFFSET VOLTAGE, vs. supply			10	25	μV/V
OFFSET VOLTAGE, vs. time			75		μV/√kh
BIAS CURRENT, initial			200	2000	pA
BIAS CURRENT, vs. supply	$V_{CM} = \pm 90V$ 100KHz BW, $R_s = 1K\Omega$, $C_c = OPEN$		4		pA/V
OFFSET CURRENT, initial			50	500	pA
INPUT IMPEDANCE, DC			10^{11}		Ω
INPUT CAPACITANCE			4		pF
COMMON MODE VOLTAGE RANGE ³		$\pm V_s \mp 15$			V
COMMON MODE REJECTION, DC		80	98		dB
NOISE			1		μVrms
GAIN					
OPEN LOOP, @ 15Hz	$R_L = 2K\Omega$, $C_c = OPEN$	94	111		dB
GAIN BANDWIDTH PRODUCT at 1MHz	$R_L = 2K\Omega$, $C_c = OPEN$		100		MHz
POWER BANDWIDTH	$R_L = 2K\Omega$, $C_c = OPEN$		470		kHz
PHASE MARGIN	Full temperature range		60		°
OUTPUT					
VOLTAGE SWING ³	$I_o = 200mA$	$\pm V_s \mp 12$	$\pm V_s \mp 10$		V
CURRENT, continuous	$C_c = OPEN$ Full temperature range $C_c = OPEN$, 2V step	200			mA
SLEW RATE, $A_v = 100$		240	300		V/μs
CAPACITIVE LOAD, $A_v = +1$		470			pF
SETTLING TIME to .1%			1		μs
RESISTANCE, no load			50		Ω
POWER SUPPLY					
VOLTAGE ⁵	See note 5	±40	±150	±200	V
CURRENT, quiescent,			10	14	mA
THERMAL					
RESISTANCE, AC, junction to case ⁴	Full temperature range, $F > 60Hz$			2.5	°C/W
RESISTANCE, DC, junction to case	Full temperature range, $F < 60Hz$			4.2	°C/W
RESISTANCE, junction to air	Full temperature range		30		°C/W
TEMPERATURE RANGE, case	Meets full range specifications	-25		+85	°C

- NOTES: 1. Unless otherwise noted: $T_C = 25^\circ\text{C}$, DC input specifications are \pm value given. Power supply voltage is typical rating. $R_C = 100\Omega$, $C_C = 68\text{pF}$.
2. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.
3. $+V_S$ and $-V_S$ denote the positive and negative power supply rail respectively.
4. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.
5. Derate max supply rating .625 V/ $^\circ\text{C}$ below 25°C case. No derating needed above 25°C case.

CAUTION

The PA90 is constructed from MOSFET transistors. ESD handling procedures must be observed. The exposed substrate contains beryllia (BeO). Do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.



GENERAL

Please read Application Note 1 "General Operating Considerations" which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.apexmicrotech.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit; heat sink selection; Apex's complete Application Notes library; Technical Seminar Workbook; and Evaluation Kits.

CURRENT LIMIT

For proper operation, the current limit resistor (R_{CL}) must be connected as shown in the external connection diagram. For optimum reliability the resistor value should be set as high as possible. The value is calculated as follows; with the maximum practical value of 32 ohms.

$$R_{CL} = \frac{.65}{I_{LIM}}$$

SAFE OPERATING AREA (SOA)

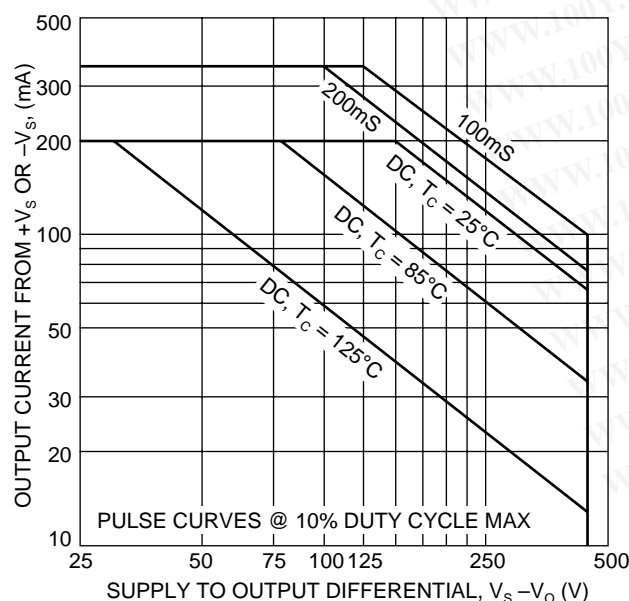
The MOSFET output stage of this power operational amplifier has two distinct limitations:

1. The current handling capability of the MOSFET geometry and the wire bonds.
2. The junction temperature of the output MOSFETs.

NOTE: The output stage is protected against transient flyback. However, for protection against sustained, high energy flyback, external fast-recovery diodes should be used.

SAFE OPERATING CURVES

The safe operating area curves define the maximum additional internal power dissipation the amplifier can tolerate when it produces the necessary output to drive an external load.



INPUT PROTECTION

Although the PA90 can withstand differential voltages up to $\pm 20V$, additional external protection is recommended. Low leakage, low capacitance JFETs connected as diodes are recommended (e.g. 2N4416, Q1-Q4 in Figure 2). The differential input voltage will be clamped to $\pm 1.4V$. This is sufficient overdrive to produce maximum power bandwidth.

POWER SUPPLY PROTECTION

Unidirectional zener diode transient suppressors are recommended as protection on the supply pins. See Figure 2. The zeners clamp transients to voltages within the power supply rating and also clamp power supply reversals to ground. Whether the zeners are used or not, the system power supply should be evaluated for transient performance including power-on overshoot and power-off polarity reversals as well as line regulation.

Conditions which can cause open circuits or polarity reversals on either power supply rail should be avoided or protected against. Reversals or opens on the negative supply rail is known to induce input stage failure. Unidirectional transzorbs prevent this, and it is desirable that they be both electrically and physically as close to the amplifier as possible.

STABILITY

The PA90 is externally compensated and performance can be tailored to the application. Use the graphs of small signal response and power response as a guide. The compensation capacitor C_c must be rated at 500V working voltage. An NPO capacitor is recommended. The compensation network $C_c R_c$ must be mounted closely to the amplifier pins 4 and 5 to avoid spurious oscillation.

QUIESCENT CURRENT REDUCTION

When pin 3 (I_Q) is shorted to pin 5 (CC2) the AB biasing of the output stage is disabled. This lowers quiescent power but also raises distortion since the output stage is then class C biased. The output stage bias current is nominally set at 1mA. Pin 3 may be left open if not used.

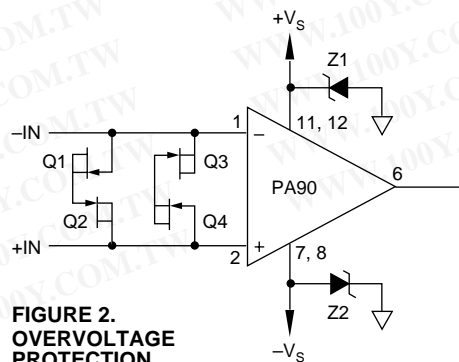


FIGURE 2.
OVERVOLTAGE
PROTECTION