DATA SHEET

PCA9517
Level translating I²C-bus repeater

Product data sheet

2004 Oct 05

Philips
Semiconductors

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Level translating I²C-bus repeater

PCA9517

DESCRIPTION

The PCA9517 is a CMOS integrated circuit that provides level shifting between low voltage (down to 0.9 V) and higher voltage (2.7 V to 5.5 V) I²C or SMBus applications. While retaining all the operating modes and features of the I²C system during the level shifts, it also permits extension of the I²C-bus by providing bi-directional buffering for both the data (SDA) and the clock (SCL) lines, thus enabling two buses of 400 pF. Using the PCA9517 enables the system designer to isolate two halves of a bus for both voltage and capacitance. The SDA and SCL pins are over voltage tolerant and are high-impedance when the PCA9517 is unpowered.

The 2.7 V to 5.5 V bus B side drivers behave much like the drivers on the PCA9515A device while the adjustable voltage bus A side drivers drive more current and eliminate the static offset voltage. This results in a LOW on the B side translating into a nearly 0 V LOW on the A side which accommodates smaller voltage swings of lower voltage logic.

The static offset design of the B side PCA9517 I/O drivers prevent them from being connected to another PCA9510, PCA9511, PCA9512, PCA9513, PCA9514, PCA9515A, PCA9516A, PCA9517 (B side), or PCA9518. The A side of two or more PCA9517s can be connected together, however, to allow a star topography with the A side on the common bus, and the A side can be connected directly to any other buffer with static or dynamic offset voltage. Multiple PCA9517s can be connected in series, A side to B side, with no build-up in offset voltage with only time of flight delays to consider.

The PCA9517 drivers are not enabled unless V_{CCA} is above 0.8 V and V_{CC} is above 2.5 V. The EN pin can also be used to turn the drivers on and off under system control. Caution should be observed to only change the state of the enable pin when the bus is idle.

FEATURES

- 2 channel, bi-directional buffer isolates capacitance and allows 400 pF on either side of the device
- Voltage level translation from 0.9 V to 5.5 V and from 2.7 V to 5.5 V
- Footprint and functions replacement for PCA9515/15A
- I²C-bus and SMBus compatible
- Active-HIGH repeater enable input
- Open-drain input/outputs
- Lock-up free operation
- Supports arbitration and clock stretching across the repeater
- Accommodates standard mode and fast mode I²C devices and multiple masters
- Powered-off high-impedance I²C pins
- Operating supply voltage range of 2.7 V to 3.6 V
- 5 V tolerant I²C and enable pins
- 0 kHz to 400 kHz clock frequency[1]
- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115, and 1000 V CDM per JESD22-C101.
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA.
- Packages offered: SO8, TSSOP8 (MSOP8)

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	TOPSIDE MARK	DRAWING NUMBER
8-pin plastic SO	–40 to +85 °C	PCA9517D	PCA9517	SOT96-1
8-pin plastic TSSOP (MSOP)	–40 to +85 °C	PCA9517DP	9517	SOT505-1

Standard packing quantities and other packaging data are available at www.standardproducts.philips.com/packaging/.

PIN CONFIGURATION

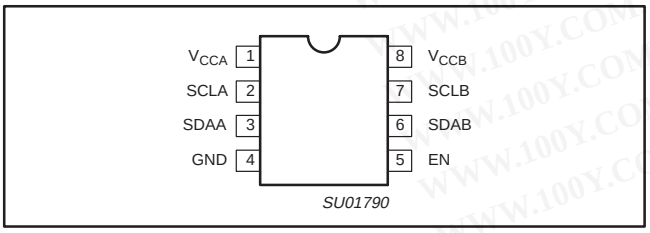


Figure 1. Pin configuration

PIN DESCRIPTION

PIN	SYMBOL	FUNCTION
1	V_{CCA}	A side supply voltage (0.9 V to 5.5 V)
2	SCLA	Serial clock A side bus
3	SDAA	Serial data A side bus
4	GND	Supply ground
5	EN	Active-HIGH repeater enable input
6	SDAB	Serial data B side bus
7	SCLB	Serial clock B side bus
8	V_{CCB}	B side and device supply voltage (2.7 V to 3.6 V)

1. The maximum system operating frequency may be less than 400 kHz because of the delays added by the repeater.

BLOCK DIAGRAM

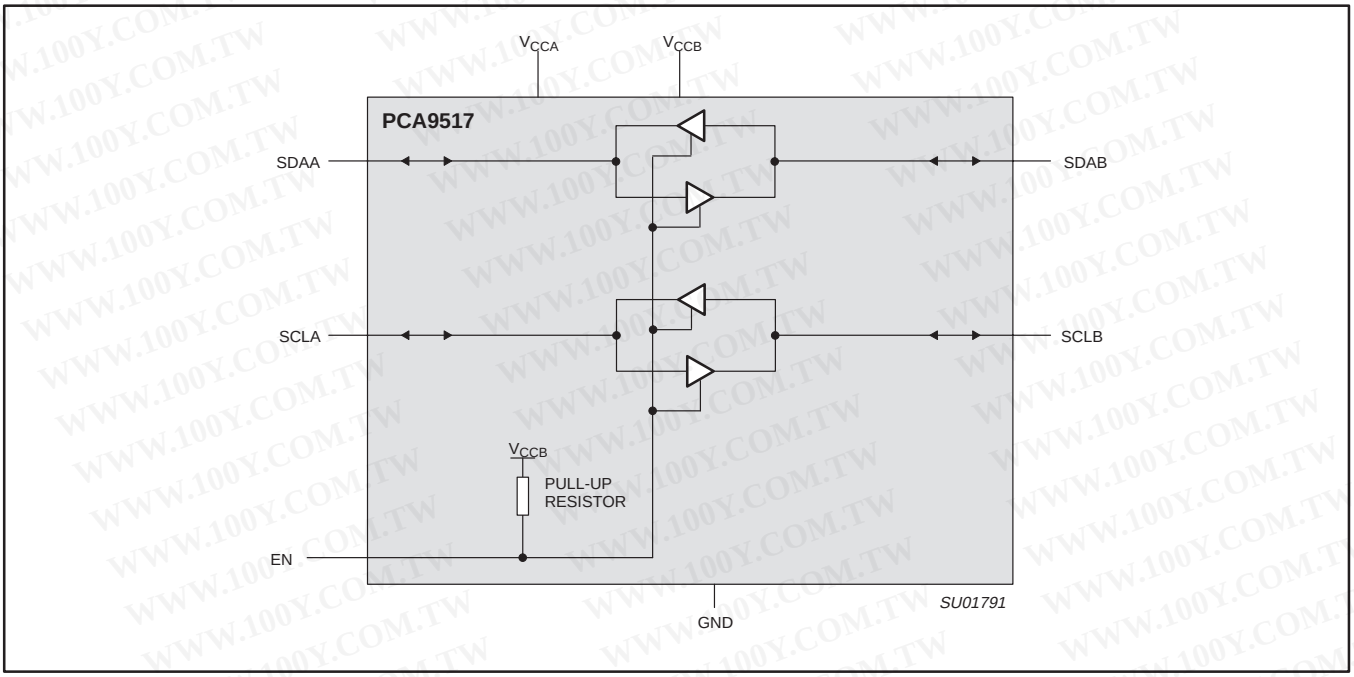


Figure 2. PCA9517 block diagram

The output pull-down on the B side internal buffer LOW is set for approximately 0.5 V, while the input threshold of the internal buffer is set about 70 mV lower (0.43 V). When the B side I/O is driven LOW internally, the LOW is not recognized as a LOW by the input. This prevents a lock-up condition from occurring. The output pull-down on the A side drives a hard LOW and the input level is set at 0.3 V_{CCA} to accommodate the need for a lower LOW level in systems where the low voltage side supply voltage is as low as 0.9 V.

FUNCTIONAL DESCRIPTION

The PCA9517 enables I²C-bus or SMBus translation down to V_{CCA} as low as 0.9 V without degradation of system performance. The PCA9517 contains two bi-directional, open drain buffers specifically designed to support up-translation/down-translation between the low voltage (as low as 0.9 V) and a 3.3 V or 5 V I²C-bus or SMBuses. All inputs and I/Os are over voltage tolerant to 5.5 V even when the device is unpowered (V_{CCB} and/or V_{CCA} = 0 V). The PCA9517 includes a power-up circuit that keeps the output drivers turned off until V_{CCB} is above 2.5 V and the V_{CCA} is above 0.8 V. V_{CCB} and V_{CCA} can be applied in any sequence at power-up. After power-up and with the enable (EN) HIGH, a LOW level on the A side (below 0.3V_{CCA}) turns the corresponding B side driver (either SDA or SCL) on and drives the B side down to about 0.5 V. When the A side rises above 0.3V_{CCA} the B side pull-down driver is turned off and the external pull-up resistor pulls the pin HIGH. When the B side falls first and goes below 0.3V_{CCB} the A side driver is turned on and the A side pulls down to 0 V. The B side pull-down is not enabled unless the B side voltage goes below 0.4 V. If the B side low voltage does not go below 0.5 V, the A side driver will turn off when the B side voltage is above 0.7V_{CCB}. If the B side low voltage goes below 0.4 V, the B side pull-down driver is enabled and the B side will only be able to rise to 0.5 V until the A side rises above 0.3V_{CCA}, then the B side will continue to rise being pulled up by the external pull-up resistor. The V_{CCA} is only used to provide the 0.3V_{CCA} reference to the A side input comparators and for the power good detect circuit. The PCA9517 logic and all I/Os are powered by the V_{CCB} pin.

Enable

The EN pin is active-HIGH with an internal pull-up to V_{CCB} and allows the user to select when the repeater is active. This can be used to isolate a badly behaved slave on power-up until after the system power-up reset. It should never change state during an I²C operation because disabling during a bus operation will hang the bus and enabling part way through a bus cycle could confuse the I²C parts being enabled.

The enable pin should only change state when the global bus and the repeater port are in an idle state to prevent system failures.

I²C Systems

As with the standard I²C system, pull-up resistors are required to provide the logic HIGH levels on the Buffered bus (Standard open-collector configuration of the I²C-bus). The size of these pull-up resistors depends on the system, but each side of the repeater must have a pull-up resistor. This part designed to work with standard mode and fast mode I²C devices in addition to SMBus devices. Standard mode I²C devices only specify 3 mA output drive, this limits the termination current to 3 mA in a generic I²C system where standard mode devices and multiple masters are possible. Under certain conditions higher termination currents can be used.

Please see Application Note AN255 *"I²C & SMBus Repeaters, Hubs and Expanders"* for additional information on sizing resistors and precautions when using more than one PCA9517 in a system or using the PCA9517 in conjunction with other bus buffers.

APPLICATION INFORMATION

A typical application is shown in Figure 3. In this example, the system master is running on a 3.3 V I²C-bus while the slave is connected to a 1.2 V bus. Both buses run at 400 kHz. Master devices can be placed on either bus.

The PCA9517 is 5 V tolerant so it does not require any additional circuitry to translate between 0.9 V to 5.5 V bus voltages and 2.7 V to 5.5 V bus voltages.

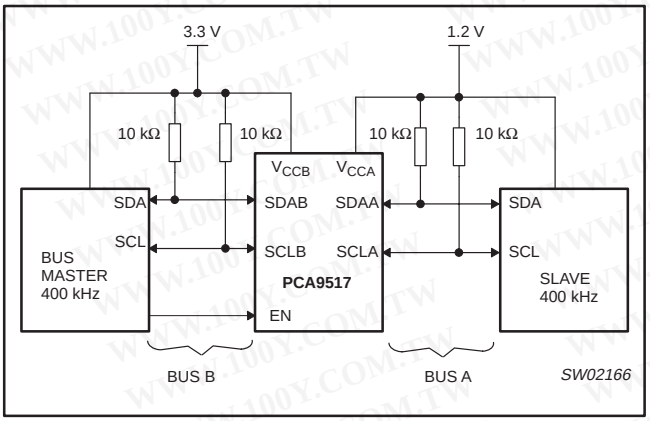


Figure 3. Typical application

When the A side of the PCA9517 is pulled LOW by a driver on the I²C-bus, a comparator detects the falling edge when it goes below $0.3V_{CCA}$ and causes the internal driver on the B side to turn on, causing the B side to pull down to about 0.5 V. When the B side of the PCA9517 falls, first a CMOS hysteresis type input detects the falling edge and causes the internal driver on the A side to turn on and pull the A side pin down to ground. In order to illustrate what would be seen in a typical application, refer to Figures 6 and 7. If the bus master in Figure 3 were to write to the slave through the PCA9517, waveforms shown in Figure 6 would be observed on the A bus. This looks like a normal I²C transmission except that the HIGH level may be as low as 0.9 V, and the turn on and turn off of the acknowledge signals are slightly delayed.

On the B bus side of the PCA9517, the clock and data lines would have a positive offset from ground equal to the V_{OL} of the PCA9517. After the 8th clock pulse, the data line will be pulled to the V_{OL} of the slave device which is very close to ground in this example. At the end of the acknowledge, the level rises only to the LOW level set by the driver in the PCA9517 for a short delay while the A bus side rises above $0.3V_{CCA}$ then it continues HIGH. It is important to note that any arbitration or clock stretching events require that the LOW level on the B bus side at the input of the PCA9517 (V_{IL}) be at or below 0.4 V to be recognized by the PCA9517 and then transmitted to the A bus side.

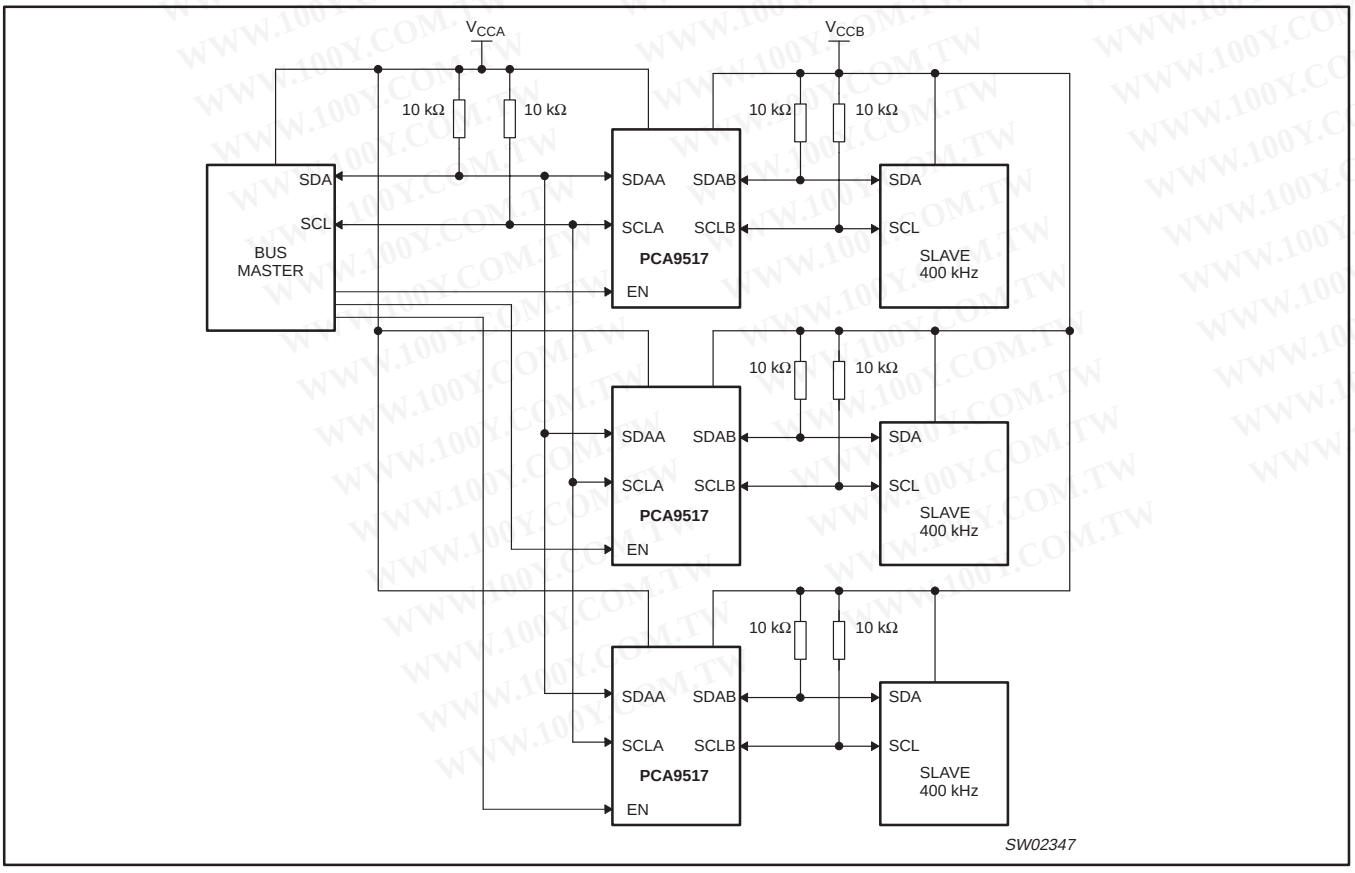


Figure 4. Typical star application

Multiple PCA9517 A sides can be connected in a star configuration, allowing all nodes to communicate with each other.

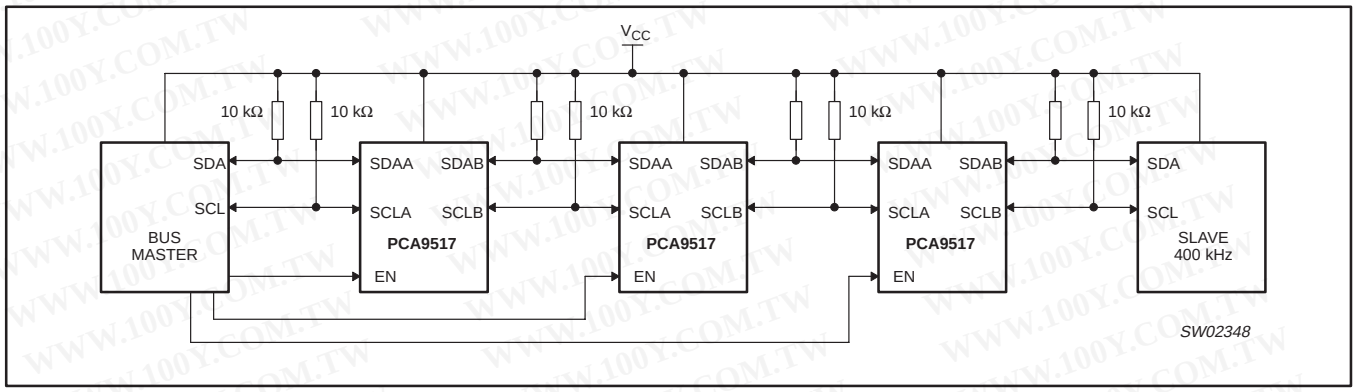


Figure 5. Typical series application

Multiple PCA9517s can be connected in series as long as the A side is connected to the B side. I²C-bus slave devices can be connected to any of the bus segments. The number of devices that can be connected in series is limited by repeater delay/time of flight considereations on the maximum bus speed requirements.

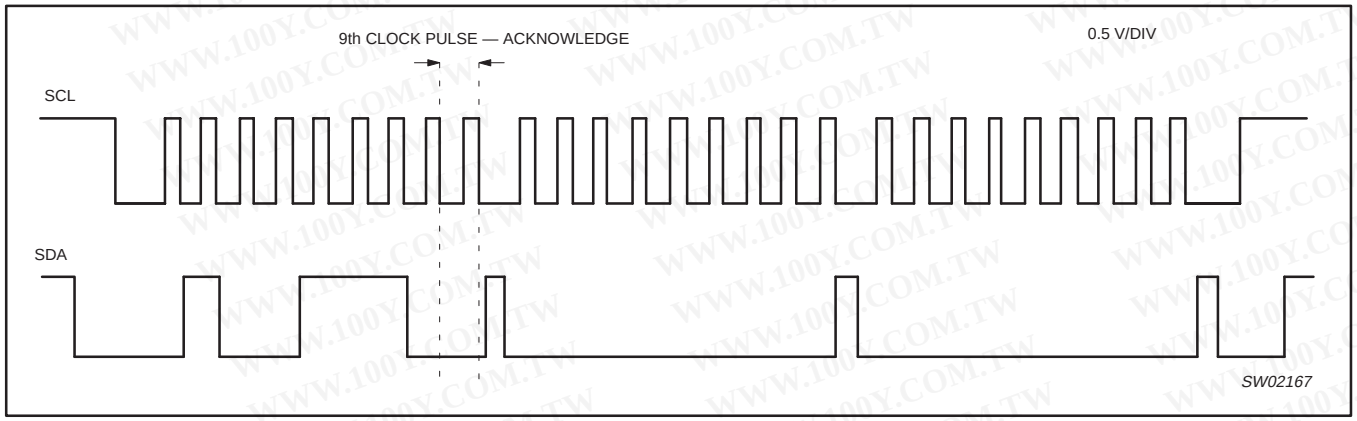


Figure 6. Bus A (0.9 V to 5.5 V bus) waveform

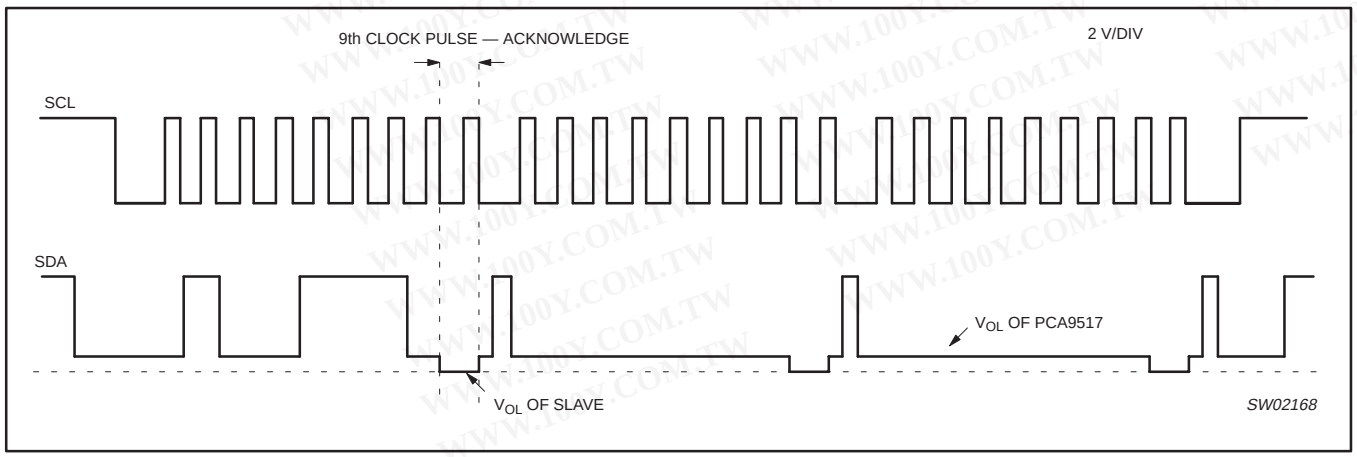


Figure 7. Bus B (2.7 V to 5.5 V bus) waveform

ABSOLUTE MAXIMUM RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134).
Voltages with respect to pin GND.

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN.	MAX.	
V_{CCB}	2.7 V to 3.3 V bus supply voltage range	–0.5	+7	V
V_{CCA}	Adjustable bus supply voltage range	–0.5	+7	V
V_{bus}	Voltage range I²C-bus, SCL or SDA or enable (EN)	–0.5	+7	V
I	DC current (any pin)	—	50	mA
P_{tot}	Power dissipation	—	100	mW
T_{stg}	Storage temperature range	–55	+125	°C
T_{amb}	Operating ambient temperature range	–40	+85	°C
T_j	Junction temperature	–	+125	°C

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 2.7 V to 3.3 V; GND = 0 V; T_{amb} = –40 °C to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	TYP.	MAX.	
Supplies						
V_{CCB}	DC supply voltage		2.7	—	3.3	V
V_{CCA}	LOW-level DC supply voltage		0.9	—	5.5	V
I_{CC}	Quiescent supply current for V_{CCA}		—	—	1	mA
I_{CCH}	Quiescent supply current, both channels HIGH	V_{CC} = 3.6 V; SDAn = SCLn = V_{CC}	—	1.5	5	mA
I_{CCA}	Quiescent supply current, both channels LOW	V_{CC} = 3.6 V; one SDA and one SCL = GND, other SDA and SCL open	—	1.5	5	mA
I_{CCAc}	Quiescent supply current in contention	V_{CC} = 3.6 V; SDAn = SCLn = GND	—	1.5	5	mA
Input and output SDAB and SCLB						
V_{IH}	HIGH-level input voltage		0.7V_{CCB}	—	5.5	V
V_{IL}	LOW-level input voltage (Note 1)		–0.5	—	0.3V_{CCB}	V
V_{ILc}	LOW-level input voltage contention (Note 1)		–0.5	—	0.4	V
V_{IK}	Input clamp voltage	I_I = –18 mA	—	—	–1.2	V
I_I	Input leakage current	V_I = 3.6 V	—	—	±1	μA
I_{IL}	Input current LOW, SDA, SCL	V_I = 0.2 V, SDA, SCL	—	—	10	μA
V_{OL}	LOW-level output voltage	I_{OL} = 100 μA or 6 mA	0.47	0.52	0.6	V
V_{OL}–V_{ILc}	LOW-level input voltage below output low level voltage	Guaranteed by design	—	—	70	mV
I_{OH}	Output HIGH-level leakage current	V_O = 3.6 V	—	—	10	μA
$C_{I/O}$	Input/output capacitance	V_I = 3 V or 0 V; V_{CC} = 3.3 V	—	6	7	pF
$C_{I/O}$	Input/output capacitance	V_I = 3 V or 0 V; V_{CC} = 0 V	—	6	7	pF
Input and output SDAA and SCLA						
V_{IH}	HIGH-level input voltage		0.7V_{CCA}	—	5.5	V
V_{IL}	LOW-level input voltage (Note 1)		–0.5	—	0.3V_{CCA}	V
V_{IK}	Input clamp voltage	I_I = –18 mA	—	—	–1.2	V
I_I	Input leakage current	V_I = 3.6 V	—	—	±1	μA
I_{IL}	Input current LOW, SDA, SCL	V_I = 0.2 V, SDA, SCL	—	—	10	μA
V_{OL}	LOW-level output voltage	I_{OL} = 6 mA	—	0.1	0.2	V
I_{OH}	Output HIGH-level leakage current	V_O = 3.6 V	—	—	10	μA
$C_{I/O}$	Input/output capacitance	V_I = 3 V or 0 V; V_{CC} = 3.3 V	—	6	7	pF
$C_{I/O}$	Input/output capacitance	V_I = 3 V or 0 V; V_{CC} = 0 V	—	6	7	pF
Enable						
V_{IL}	LOW-level input voltage		–0.5	—	0.3V_{CCB}	V
V_{IH}	HIGH-level input voltage		0.7V_{CCB}	—	5.5	V
I_{IL}	Input current LOW, EN	V_I = 0.2 V, EN; V_{CC} = 3.6 V	—	10	30	μA
I_{LI}	Input leakage current		–1	—	1	μA
C_I	Input capacitance	V_I = 3.0 V or 0 V	—	6	7	pF

NOTE:

1. V_{IL} specification is for the first LOW level seen by the SDAx/SCLx lines. V_{ILc} is for the second and subsequent LOW levels seen by the SDAx/SCLx lines.

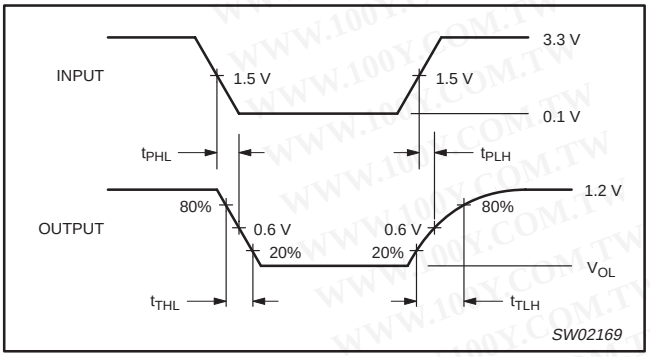
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	TYP.	MAX.	
t_{PLH}	Propagation delay, B to A side	Waveform 3; Note 3	100	170	250	ns
t_{PHL}	Propagation delay, B to A side	$V_{CCA} \leq 2.7$ V; Waveform 1	30	80 [7]	110	ns
		$V_{CCA} \geq 3$ V; Waveform 1	10	66	300	ns
t_{TLH}	Transition time, A side	Waveform 2	10	20	30	ns
t_{THL}	Transition time, A side	$V_{CCA} \leq 2.7$ V; Waveform 2	1	77 [7]	105	ns
		$V_{CCA} \geq 3$ V; Waveform 2	20	70	175	ns
t_{PLH}	Propagation delay, A to B side	Waveform 2; Note 2	25	53	110	ns
t_{PHL}	Propagation delay, A to B side	Waveform 2; Note 2	60	79	230	ns
t_{TLH}	Transition time, B side	Waveform 1	120	140	170	ns
t_{THL}	Transition time, B side	Waveform 1	30	48	90	ns
t_{SET}	Enable HIGH before Start condition	Note 6	100	–	–	ns
t_{HOLD}	Enable HIGH after Stop condition	Note 6	100	–	–	ns

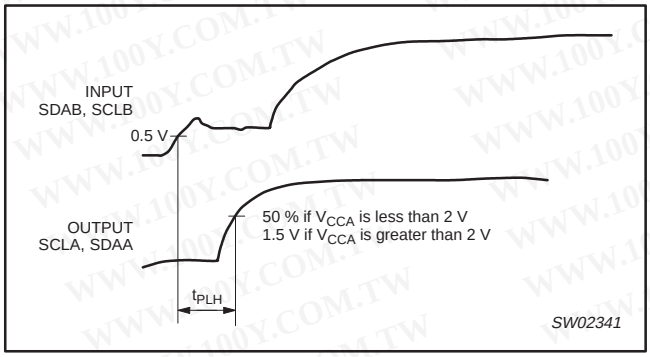
NOTES:

1. Times are specified with loads of 1.35 kΩ pull-up resistance and 57 pF load capacitance on the B side and 167 Ω pull-up and 57 pF load capacitance on the A side. Different load resistnace and capacitance will alter the RC time constant, thereby changing the propagation delay and transition times.
2. The proportional delay data from A to B side is measured at $0.3V_{CCA}$ on the A side to 1.5 V on the B side.
3. The t_{PLH} delay data from B to A side is measured at 0.5 V on the B side to $0.5V_{CCA}$ on the A side when V_{CCA} is less than 2 V, and 1.5 V on the A side if V_{CCA} is greater than 2 V.
4. Pull-up voltages are V_{CCA} on the A side and V_{CCB} on the B side.
5. Typical values were measured with $V_{CCA} = 3.6$ V at $T_{amb} = 25$ °C, unless otherwise noted.
6. The enable pin, EN, should only change state when the global bus and the repeater port are in an idle state.
7. Typical value measured with $V_{CCA} = 2.7$ V at $T_{amb} = 25$ °C.

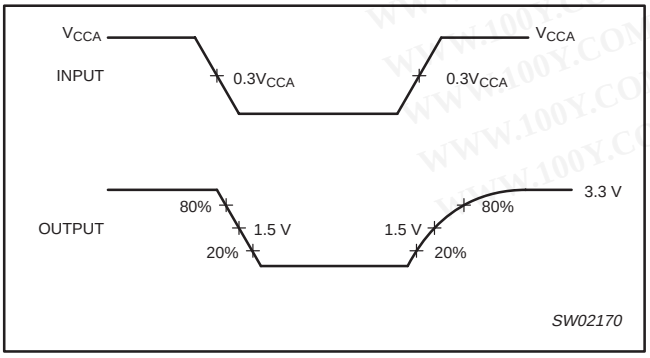
AC WAVEFORMS



Waveform 1.

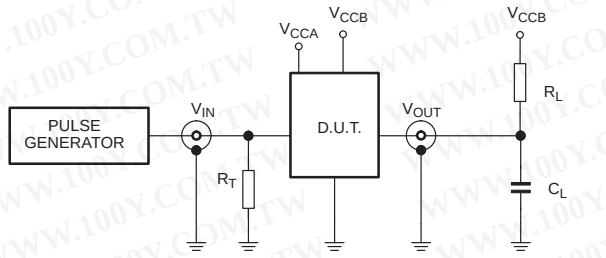


Waveform 3.



Waveform 2.

TEST CIRCUIT



Test Circuit for Open Drain Outputs

DEFINITIONS

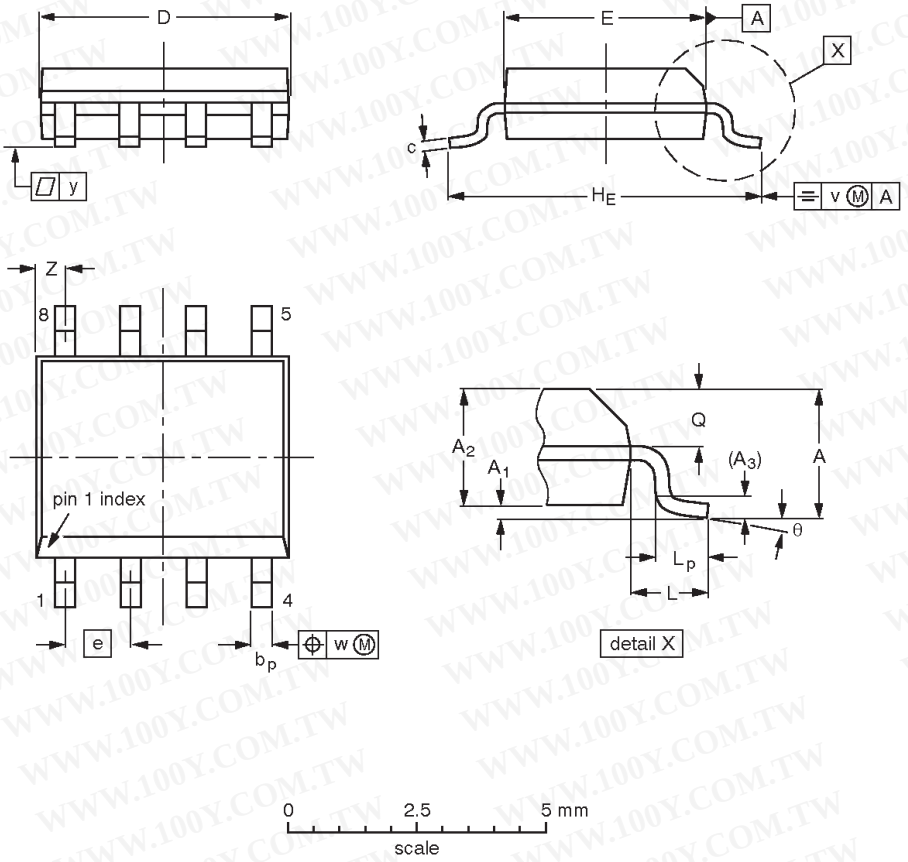
R_L = Load resistor; 1.35 kΩ on B side, 167 Ω on A side

C_L = Load capacitance includes jig and probe capacitance; 57 pF

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SW02342

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

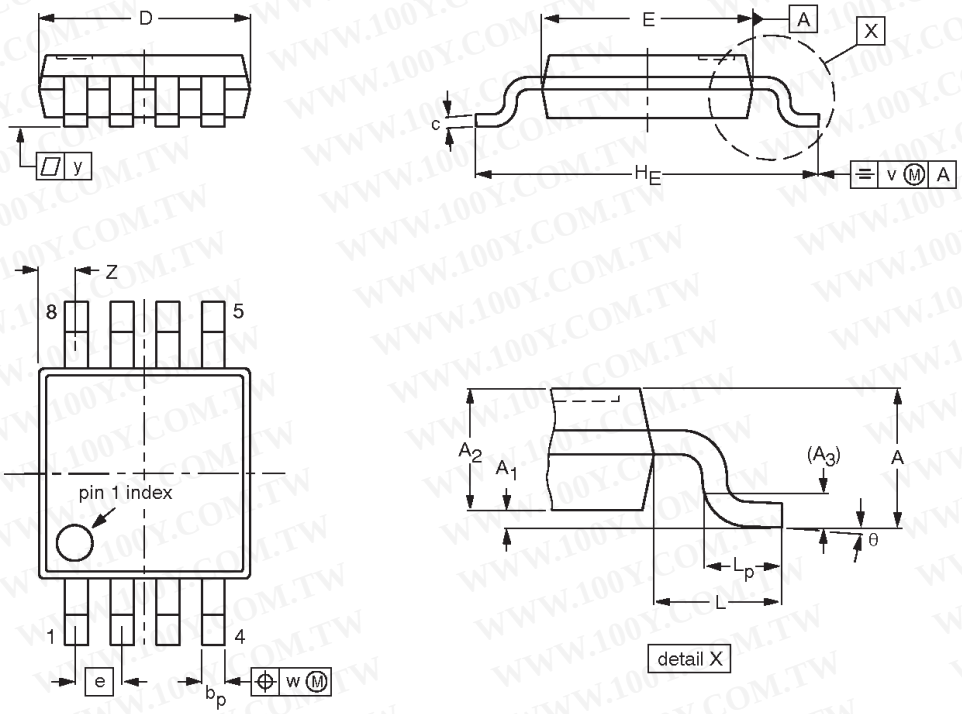
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

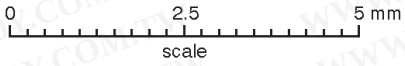
Notes

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT96-1	076E03	MS-012				~~99-12-27~~ 03-02-18

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm **SOT505-1**





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.45 0.25	0.28 0.15	3.1 2.9	3.1 2.9	0.65	5.1 4.7	0.94	0.7 0.4	0.1	0.1	0.1	0.70 0.35	6° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT505-1						~~99-04-09~~ 03-02-18

REVISION HISTORY

Rev	Date	Description
_1	20041005	**Product data sheet (9397 750 13252).**

Level translating I²C-bus repeater

PCA9517

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specifications defined by Philips. This specification can be ordered using the code 9398 393 40011.

Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definitions
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

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Contact information

For additional information please visit
http://www.semiconductors.philips.com. Fax: **+31 40 27 24825**

For sales offices addresses send e-mail to:
sales.addresses@www.semiconductors.philips.com.

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