

PH4530L

N-channel TrenchMOS™ logic level FET

Rev. 02 — 26 January 2005

Product data sheet

1. Product profile

1.1 General description

Logic level N-channel enhancement mode field effect transistor in a plastic package using TrenchMOS™ technology.

1.2 Features

- Low thermal resistance
- Logic level gate drive
- SO8 equivalent area footprint
- Low on-state resistance.

1.3 Applications

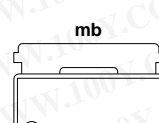
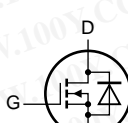
- DC-to-DC converters
- Portable appliances
- Switched-mode power supplies
- Notebook computers.

1.4 Quick reference data

- $V_{DS} \leq 30$ V
- $I_D \leq 80$ A
- $P_{tot} \leq 62.5$ W
- $R_{DSon} \leq 5.7$ m Ω .

2. Pinning information

Table 1: Discrete pinning

Pin	Description	Simplified outline	Symbol
1,2,3	source		
4	gate		
mb	mounting base; connected to drain		

Top view

SOT669 (LFAK)

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PHILIPS

3. Ordering information

Table 2: Ordering information

Type number	Package		Version
	Name	Description	
PH4530L	LFAK	plastic single-ended surface mounted package (LFAK); 4 leads	SOT669

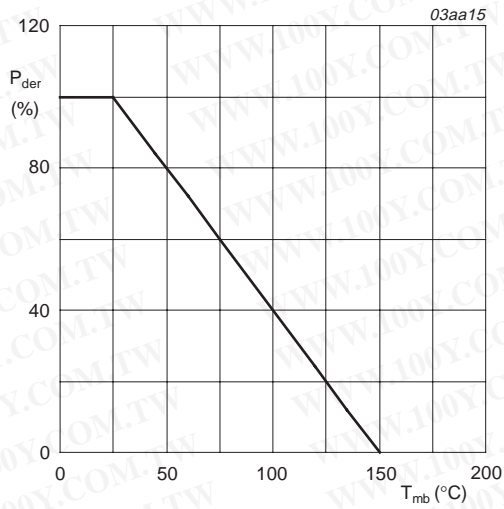
4. Limiting values

Table 3: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

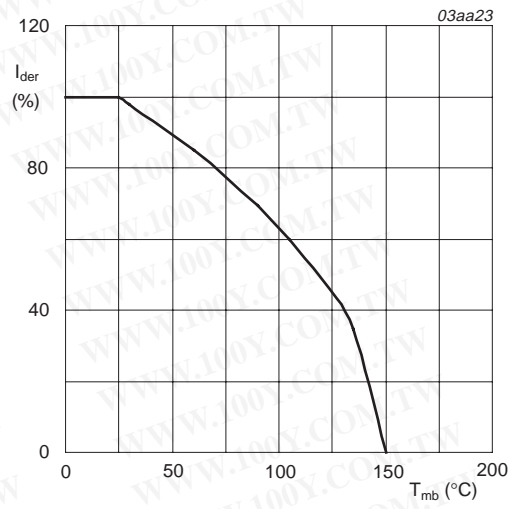
Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage (DC)	$25\text{ °C} \leq T_j \leq 150\text{ °C}$	-	30	V
V_{GS}	gate-source voltage (DC)		-	± 20	V
I_D	drain current (DC)	$T_{mb} = 25\text{ °C}; V_{GS} = 10\text{ V};$ Figure 2 and 3	-	80	A
		$T_{mb} = 100\text{ °C}; V_{GS} = 10\text{ V};$ Figure 2	-	240	A
I_{DM}	peak drain current	$T_{mb} = 25\text{ °C};$ pulsed; $t_p \leq 10\text{ }\mu\text{s};$ Figure 3	-	50.7	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C};$ Figure 1	-	62.5	W
T_{stg}	storage temperature		-55	+150	°C
T_j	junction temperature		-55	+150	°C
Source-drain diode					
I_S	source (diode forward) current (DC)	$T_{mb} = 25\text{ °C}$	-	52	A
I_{SM}	peak source (diode forward) current	$T_{mb} = 25\text{ °C};$ pulsed; $t_p \leq 10\text{ }\mu\text{s}$	-	150	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	unclamped inductive load; $I_D = 36.2\text{ A};$ $t_p = 0.24\text{ ms}; V_{DD} \leq 30\text{ V}; V_{GS} = 10\text{ V};$ starting $T_j = 25\text{ °C}$	-	130	mJ

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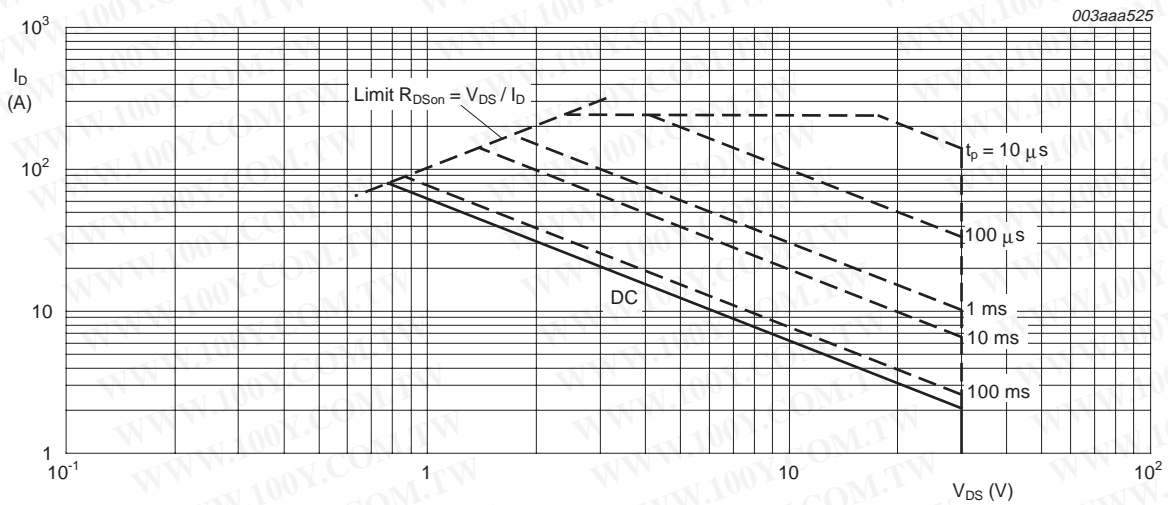
$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ C)}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of mounting base temperature.



$$I_{der} = \frac{I_D}{I_{D(25^\circ C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of mounting base temperature.



T_{mb} = 25 °C; I_{DM} is single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

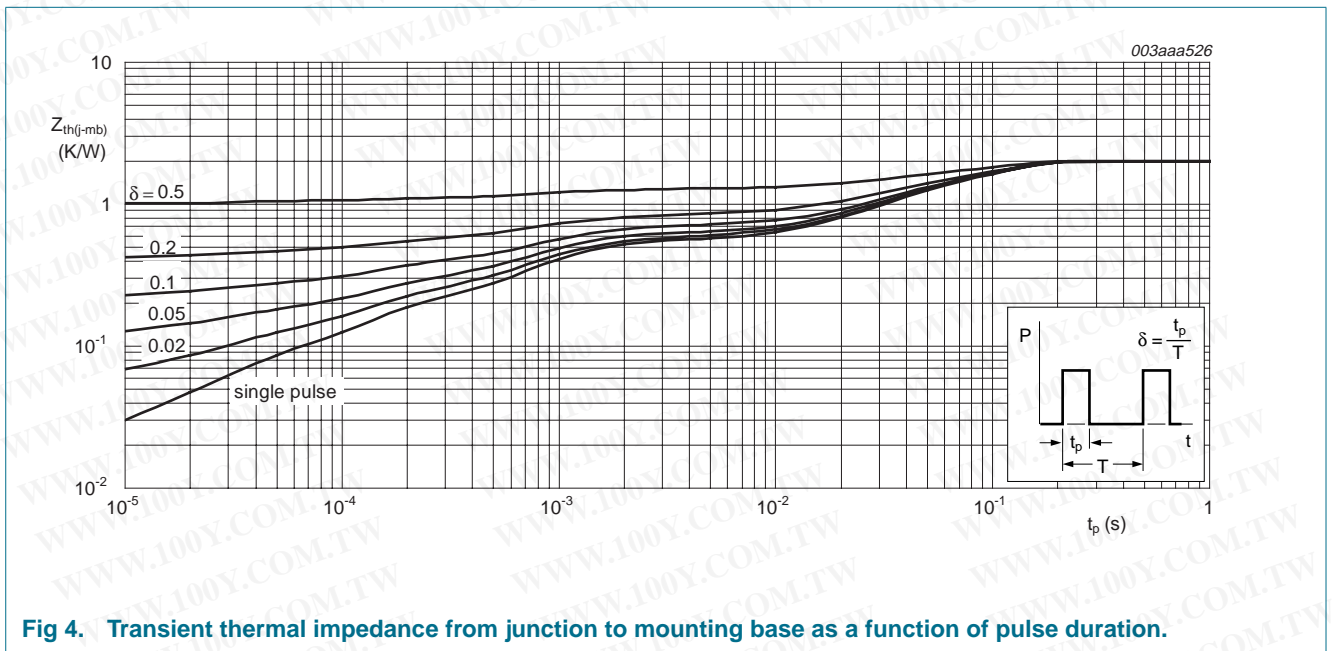
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5. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Figure 4	-	-	2	K/W

5.1 Transient thermal impedance



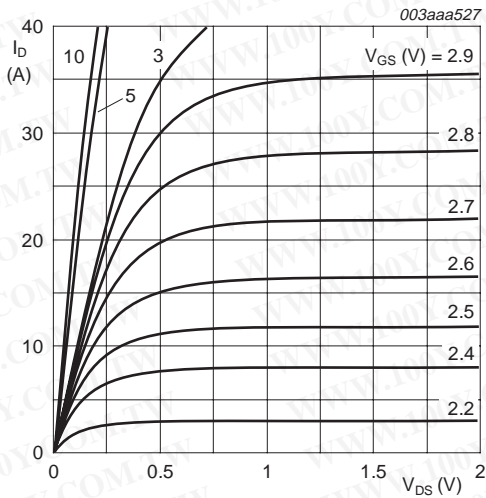
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6. Characteristics

Table 5: Characteristics
 $T_j = 25\text{ }^\circ\text{C}$ unless otherwise specified.

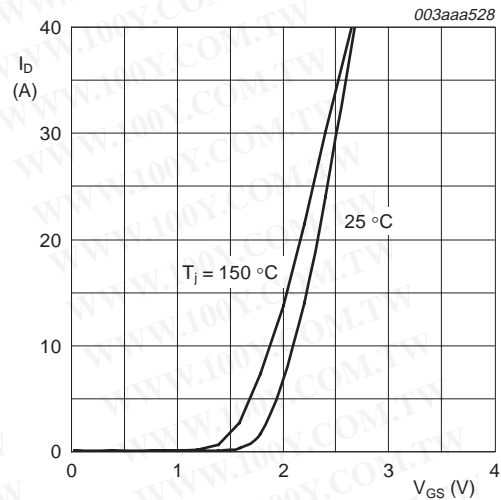
Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
Static characteristics							
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250\ \mu\text{A}$; $V_{GS} = 0\ \text{V}$	30	-	-	V	
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\ \text{mA}$; $V_{DS} = V_{GS}$; Figure 9	1	1.5	2	V	
I_{DSS}	drain-source leakage current	$V_{DS} = 30\ \text{V}$; $V_{GS} = 0\ \text{V}$		$T_j = 25\text{ }^\circ\text{C}$	0.06	1	μA
				$T_j = 150\text{ }^\circ\text{C}$	-	500	μA
I_{GSS}	gate-source leakage current	$V_{GS} = \pm 15\ \text{V}$; $V_{DS} = 0\ \text{V}$	-	2	100	nA	
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\ \text{V}$; $I_D = 15\ \text{A}$; Figure 7 and 8		$T_j = 25\text{ }^\circ\text{C}$	4.8	5.7	m Ω
				$T_j = 150\text{ }^\circ\text{C}$	8.2	9.7	m Ω
				$V_{GS} = 5\ \text{V}$; $I_D = 15\ \text{A}$; Figure 7 and 8	5.8	7.2	m Ω
Dynamic characteristics							
$Q_{g(tot)}$	total gate charge	$I_D = 25\ \text{A}$; $V_{DS} = 10\ \text{V}$; $V_{GS} = 5\ \text{V}$; Figure 13	-	23.5	-	nC	
Q_{gs}	gate-source charge		-	5.8	-	nC	
Q_{gd}	gate-drain (Miller) charge		-	6.5	-	nC	
C_{iss}	input capacitance	$V_{GS} = 0\ \text{V}$; $V_{DS} = 10\ \text{V}$; $f = 1\ \text{MHz}$; Figure 11	-	1972	-	pF	
C_{oss}	output capacitance		-	769	-	pF	
C_{rss}	reverse transfer capacitance		-	304	-	pF	
$t_{d(on)}$	turn-on delay time	$V_{DS} = 10\ \text{V}$; $I_D = 25\ \text{A}$;	-	22	-	ns	
t_r	rise time	$V_{GS} = 5\ \text{V}$; $R_G = 4.7\ \Omega$	-	40	-	ns	
$t_{d(off)}$	turn-off delay time		-	48	-	ns	
t_f	fall time		-	18	-	ns	
Source-drain diode							
V_{SD}	source-drain (diode forward) voltage	$I_S = 15\ \text{A}$; $V_{GS} = 0\ \text{V}$; Figure 12	-	0.85	1.2	V	
t_{rr}	reverse recovery time	$I_S = 20\ \text{A}$; $di/dt = -100\ \text{A}/\mu\text{s}$; $V_{GS} = 0\ \text{V}$	-	38	-	ns	

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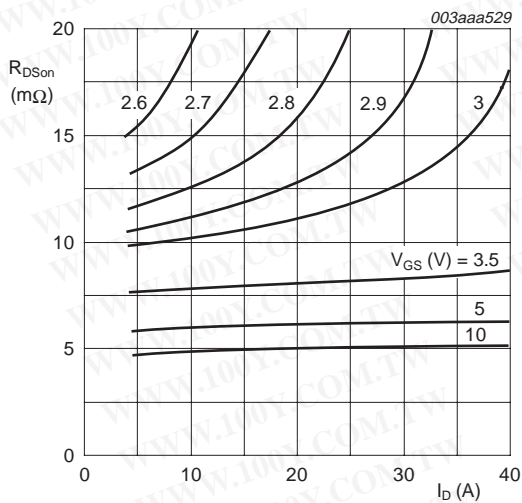
Tj = 25 °C

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



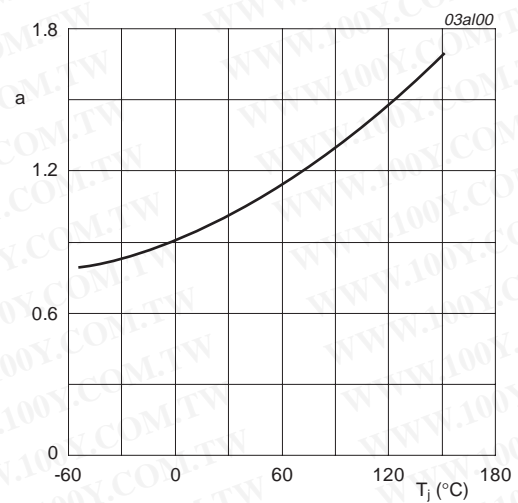
Tj = 25 °C and 150 °C; VDS > Id x RDSon

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



Tj = 25 °C

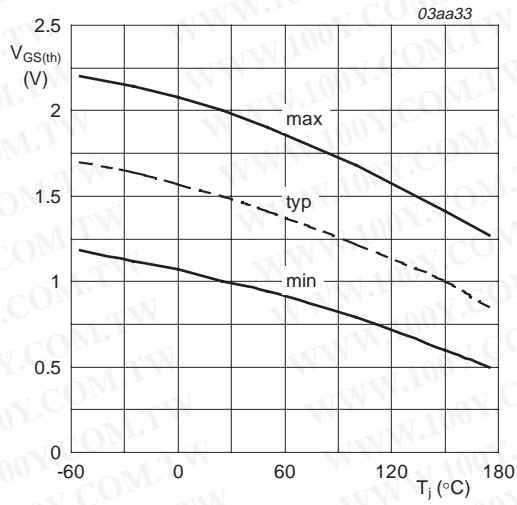
Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}C)}}$$

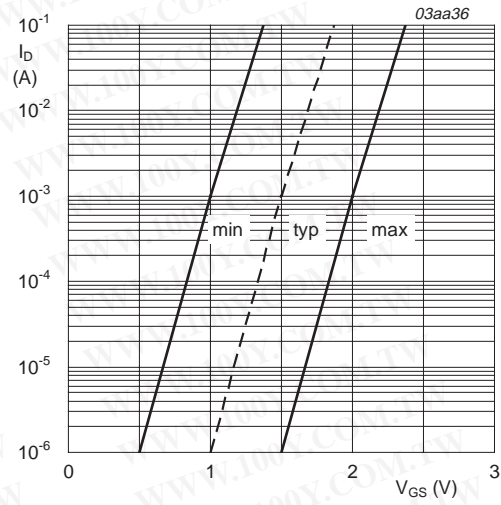
Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.

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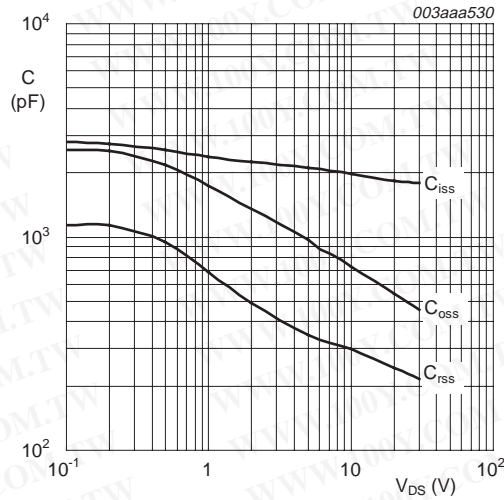
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature.



$T_j = 25 \text{ °C}; V_{DS} = 5 \text{ V}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

Fig 11. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.

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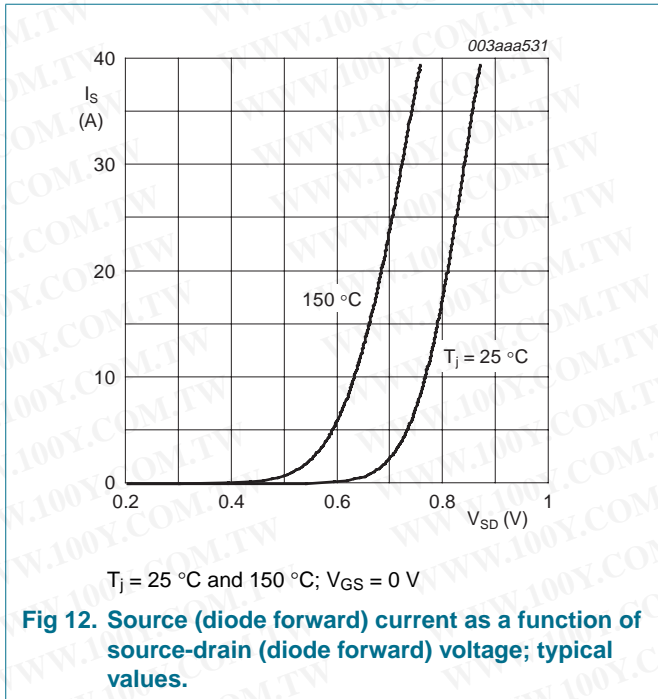


Fig 12. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.

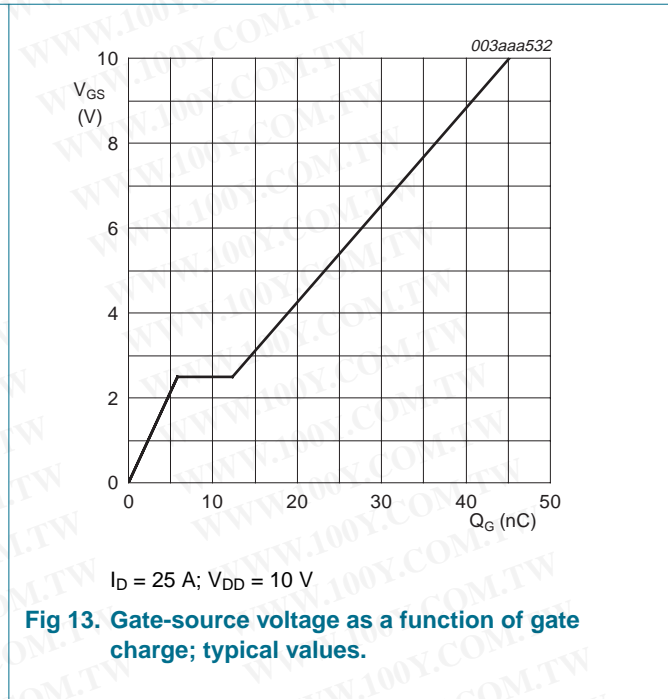


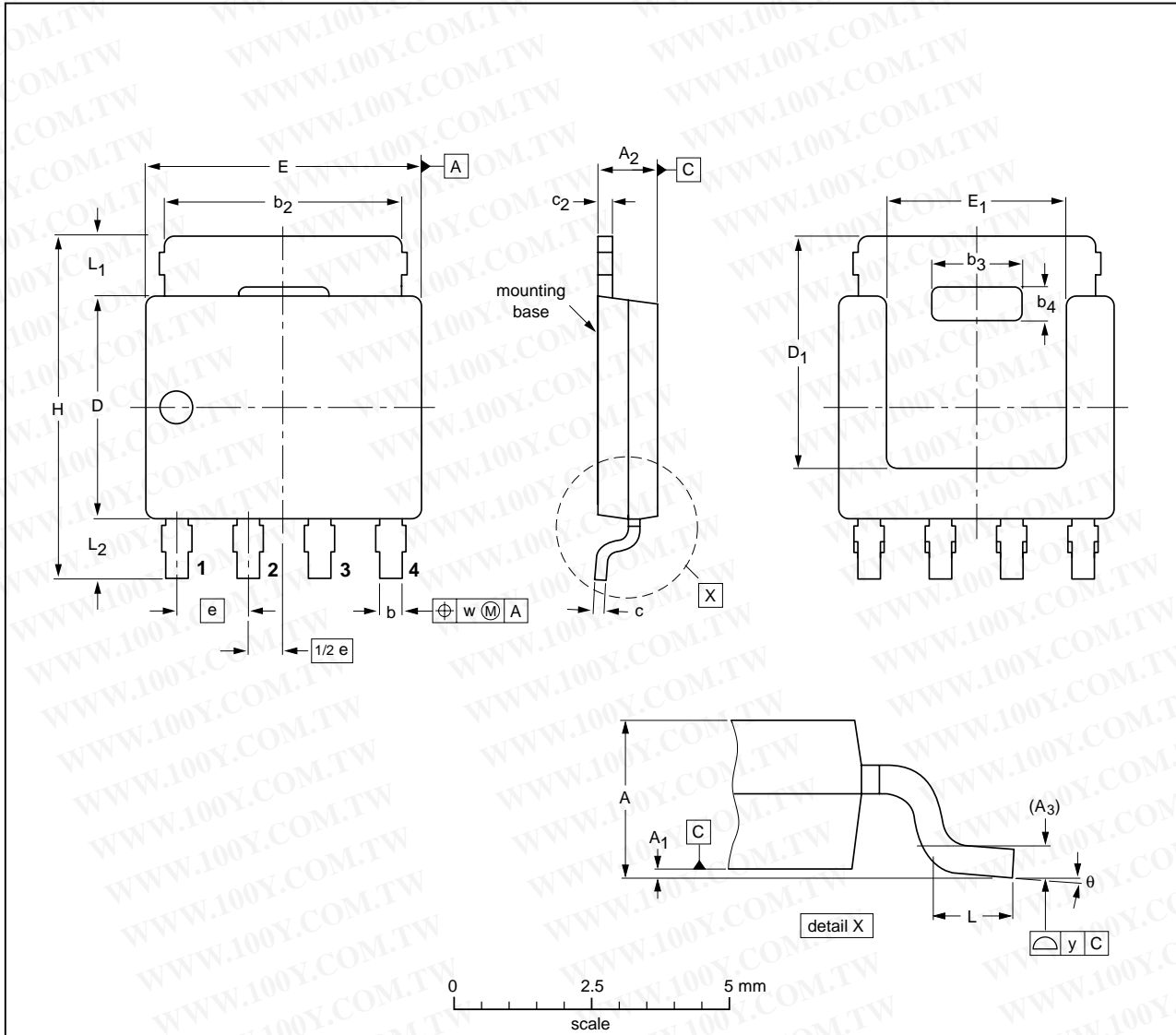
Fig 13. Gate-source voltage as a function of gate charge; typical values.

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7. Package outline

Plastic single-ended surface mounted package (LFAK); 4 leads

SOT669



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁	A ₂	A ₃	b	b ₂	b ₃	b ₄	c	c ₂	D ⁽¹⁾	D ₁ ⁽¹⁾ max	E ⁽¹⁾	E ₁ ⁽¹⁾	e	H	L	L ₁	L ₂	w	y	θ
mm	1.20 1.01	0.15 0.00	1.10 0.95	0.25	0.50 0.35	4.41 3.62	2.2 2.0	0.9 0.7	0.25 0.19	0.30 0.24	4.10 3.80	4.20	5.0 4.8	3.3 3.1	1.27	6.2 5.8	0.85 0.40	1.3 0.8	1.3 0.8	0.25	0.1	8° 0°

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT669		MO-235			03-09-15 04-10-13

Fig 14. SOT669 (LFAK) package outline.

8. Revision history

Table 6: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
PH4530L_2	20050126	Product data sheet	-	9397 750 14031	PH4530L_1
Modifications:					
<ul style="list-style-type: none"> • Section 1.4 "Quick reference data" I_D and R_{DSon} values updated • Table 3 "Limiting values" I_D and I_{DM} values updated • Figure 3, Figure 6, Figure 11 and Figure 13 updated • Table 5 "Characteristics" R_{DSon}, $Q_{g(tot)}$, Q_{gs}, Q_{gd}, C_{iss}, C_{oss} and C_{rss} values updated. 					
PH4530L_1	20040304	Preliminary data sheet	-	9397 750 12813	-

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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