

# DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

勝特力材料 886-3-5753170  
勝特力电子(上海) 86-21-54151736  
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## 74HC/HCT238 3-to-8 line decoder/demultiplexer

Product specification  
File under Integrated Circuits, IC06

December 1990

## 3-to-8 line decoder/demultiplexer

## 74HC/HCT238

## FEATURES

- Demultiplexing capability
- Multiple input enable for easy expansion
- Ideal for memory chip select decoding
- Active HIGH mutually exclusive outputs
- Output capability: standard
- I<sub>CC</sub> category: MSI

## GENERAL DESCRIPTION

The 74HC/HCT238 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT238 decoders accept three binary weighted address inputs (A<sub>0</sub>, A<sub>1</sub>, A<sub>2</sub>) and when enabled,

provide 8 mutually exclusive active HIGH outputs (Y<sub>0</sub> to Y<sub>7</sub>).

The "238" features three enable inputs: two active LOW ( $\bar{E}_1$  and  $\bar{E}_2$ ) and one active HIGH (E<sub>3</sub>). Every output will be LOW unless  $\bar{E}_1$  and  $\bar{E}_2$  are LOW and E<sub>3</sub> is HIGH.

This multiple enable function allows easy parallel expansion of the "238" to a 1-of-32 (5 lines to 32 lines) decoder with just four "238" ICs and one inverter.

The "238" can be used as an eight output demultiplexer by using one of the active LOW enable inputs as the data input and the remaining enable inputs as strobes. Unused enable inputs must be permanently tied to their appropriate active HIGH or LOW state.

The "238" is identical to the "138" but has non-inverting outputs.

## QUICK REFERENCE DATA

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay A <sub>n</sub> to Y <sub>n</sub> E <sub>3</sub> to Y <sub>n</sub> $\bar{E}_n$ to Y <sub>n</sub>	C <sub>L</sub> = 15 pF; V <sub>CC</sub> = 5 V	14 16 17	18 20 21	ns ns ns
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per package	notes 1 and 2	72	76	pF

## Notes

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz

f<sub>o</sub> = output frequency in MHz

$\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs

C<sub>L</sub> = output load capacitance in pF

V<sub>CC</sub> = supply voltage in V

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

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## ORDERING INFORMATION

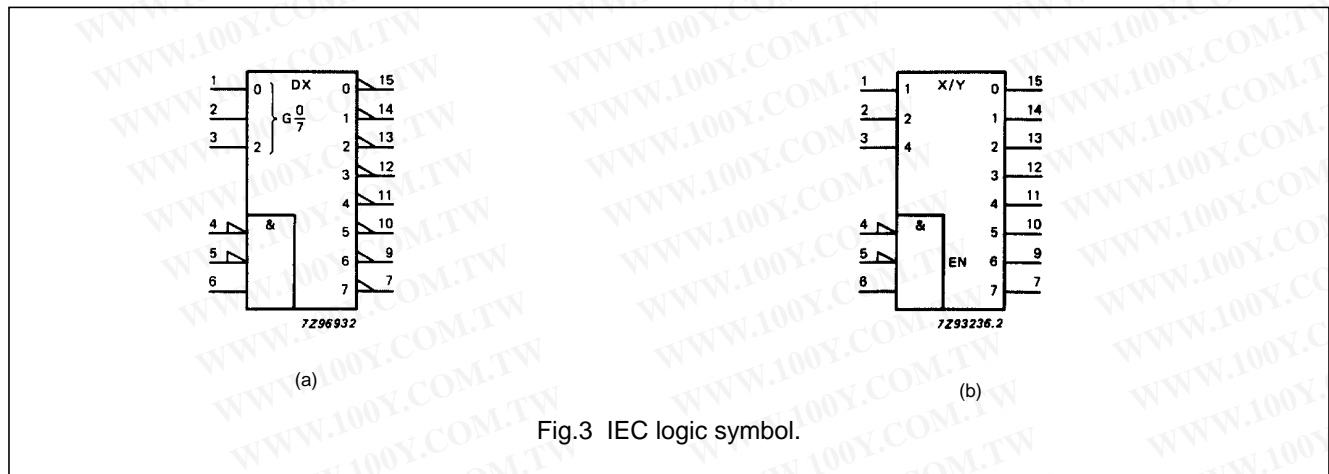
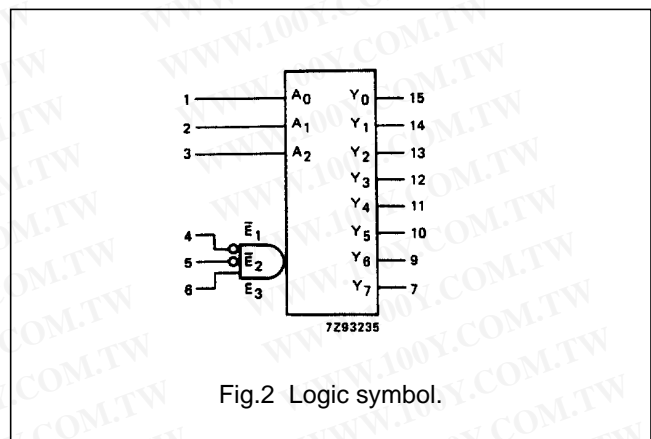
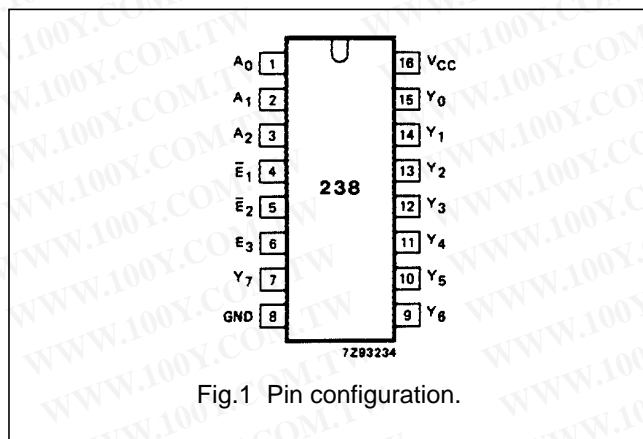
See "74HC/HCT/HCU/HCMOS Logic Package Information".

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PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 2, 3	A <sub>0</sub> to A <sub>2</sub>	address inputs
4, 5	$\bar{E}_1, \bar{E}_2$	enable inputs (active LOW)
6	E <sub>3</sub>	enable input (active HIGH)
8	GND	ground (0 V)
15, 14, 13, 12, 11, 10, 9, 7	Y <sub>0</sub> to Y <sub>7</sub>	outputs (active HIGH)
16	V <sub>CC</sub>	positive supply voltage



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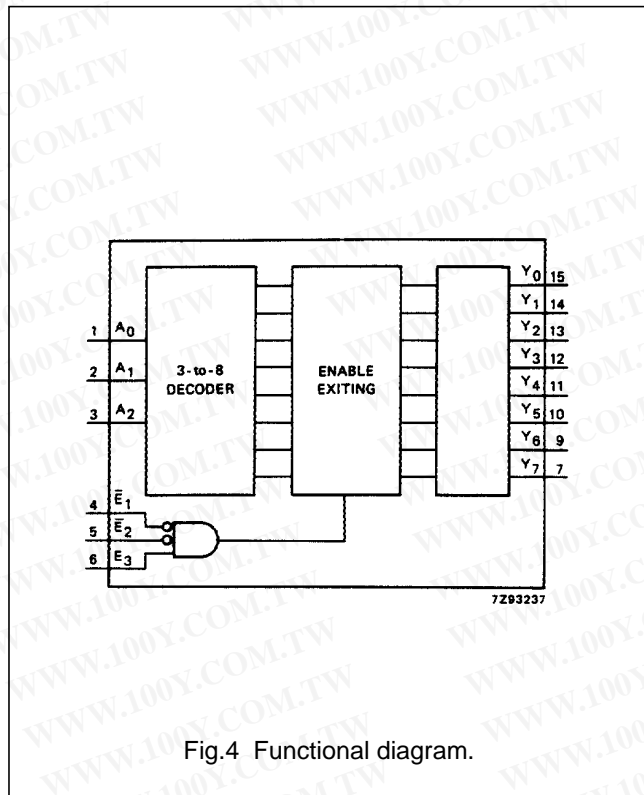


Fig.4 Functional diagram.

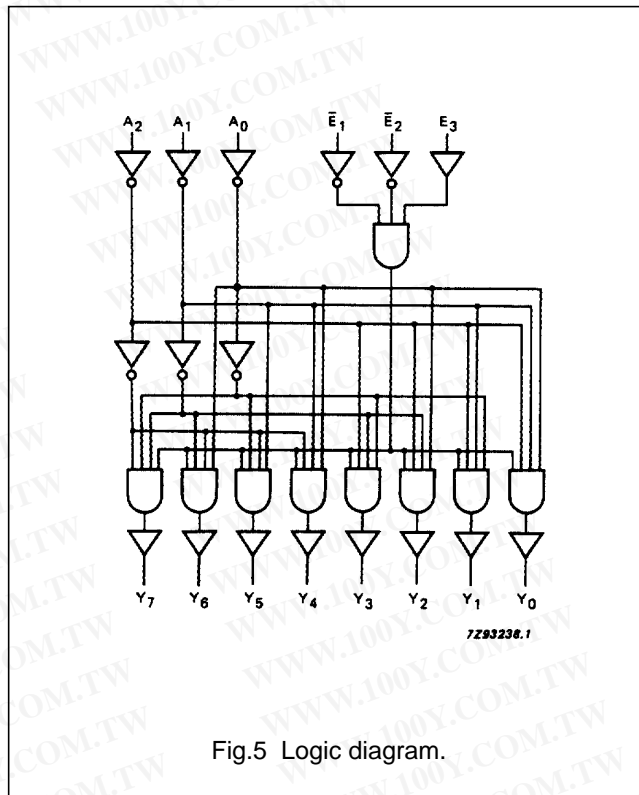


Fig.5 Logic diagram.

FUNCTION TABLE

INPUTS						OUTPUTS							
$\bar{E}_1$	$\bar{E}_2$	$E_3$	$A_0$	$A_1$	$A_2$	$Y_0$	$Y_1$	$Y_2$	$Y_3$	$Y_4$	$Y_5$	$Y_6$	$Y_7$
H	X	X	X	X	X	L	L	L	L	L	L	L	L
X	H	X	X	X	X	L	L	L	L	L	L	L	L
X	X	L	X	X	X	L	L	L	L	L	L	L	L
L	L	H	L	L	L	H	L	L	L	L	L	L	L
L	L	H	H	L	L	L	H	L	L	L	L	L	L
L	L	H	L	H	L	L	L	H	L	L	L	L	L
L	L	H	L	L	H	L	L	L	L	H	L	L	L
L	L	H	H	L	H	L	L	L	L	L	H	L	L
L	L	H	L	H	H	L	L	L	L	L	L	H	L
L	L	H	H	H	H	L	L	L	L	L	L	L	H

Note

- 1. H = HIGH voltage level
- L = LOW voltage level
- X = don't care

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## 74HC/HCT238

**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I<sub>CC</sub> category: MSI

**AC CHARACTERISTICS FOR 74HC**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> (V)	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay A <sub>n</sub> to Y <sub>n</sub>		47 17 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig.6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay E <sub>3</sub> to Y <sub>n</sub>		52 19 15	160 32 27		200 40 34		240 48 41	ns	2.0 4.5 6.0	Fig.6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay $\bar{E}_n$ to Y <sub>n</sub>		50 18 14	155 31 26		195 39 33		235 47 40	ns	2.0 4.5 6.0	Fig.7
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Figs 6 and 7

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**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see "74HC/HCT/HCU/HCMOS Logic Family Specifications".

Output capability: standard

I<sub>CC</sub> category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
A <sub>n</sub>	0.70
$\bar{E}_n$	0.40
E <sub>3</sub>	1.45

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**AC CHARACTERISTICS FOR 74HCT**

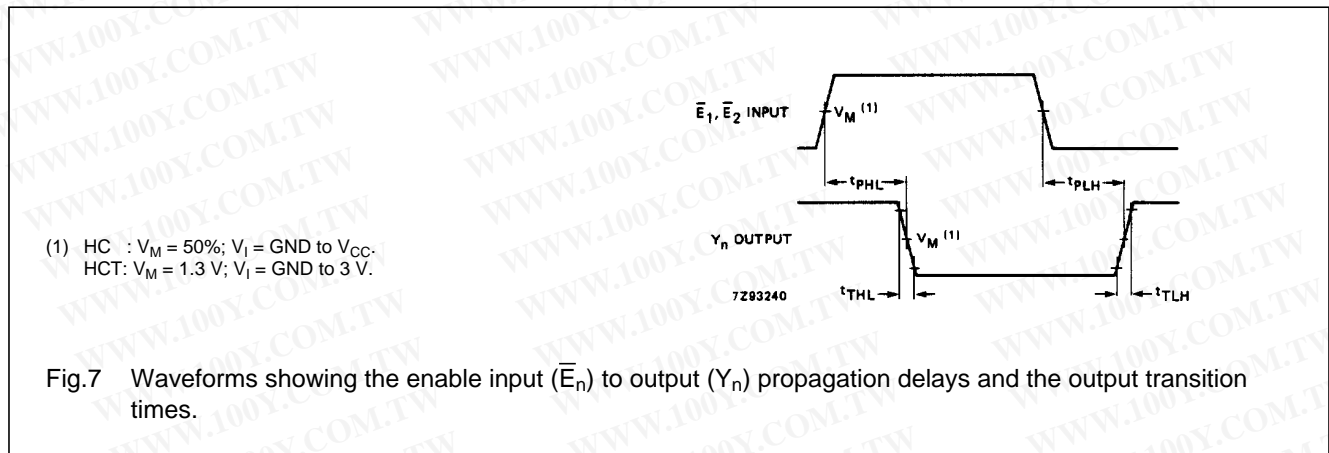
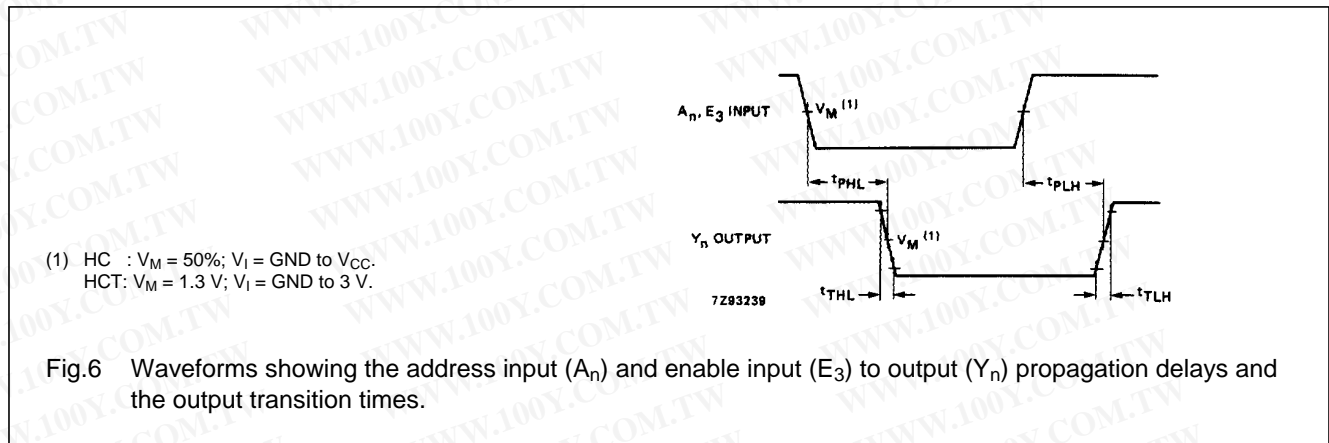
GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> (V)	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub>	propagation delay A <sub>n</sub> to Y <sub>n</sub>		21	35		44		53	ns	4.5	Fig.6
t <sub>PLH</sub>	propagation delay A <sub>n</sub> to Y <sub>n</sub>		17	35		44		53	ns	4.5	Fig.6
t <sub>PHL</sub>	propagation delay E <sub>3</sub> to Y <sub>n</sub>		22	37		46		56	ns	4.5	Fig.6
t <sub>PLH</sub>	propagation delay E <sub>3</sub> to Y <sub>n</sub>		18	37		46		56	ns	4.5	Fig.6
t <sub>PHL</sub>	propagation delay $\bar{E}_n$ to Y <sub>n</sub>		21	35		44		53	ns	4.5	Fig.7
t <sub>PLH</sub>	propagation delay $\bar{E}_n$ to Y <sub>n</sub>		18	35		44		53	ns	4.5	Fig.7
t <sub>THL</sub> /t <sub>TLH</sub>	output transition time		7	15		19		22	ns	4.5	Figs 6 and 7

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## AC WAVEFORMS



## PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".

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