



8-Bit CMOS Microcontrollers

Devices included in this data sheet:

PIC16C61

PIC16C64A

PIC16C62

PIC16CR64

PIC16C62A

PIC16C65

PIC16CR62

PIC16C65A

PIC16C63

PIC16CR65

PIC16CR63

PIC16C66

PIC16C64

PIC16C67

PIC16C6X Microcontroller Core Features:

- · High performance RISC CPU
- Only 35 single word instructions to learn
- All single cycle instructions except for program branches which are two-cycle
- Operating speed: DC 20 MHz clock input DC - 200 ns instruction cycle
- · Interrupt capability
- Eight level deep hardware stack
- · Direct, indirect, and relative addressing modes
- Power-on Reset (POR)
- Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Watchdog Timer (WDT) with its own on-chip RC oscillator for reliable operation
- Programmable code-protection
- Power saving SLEEP mode
- Selectable oscillator options

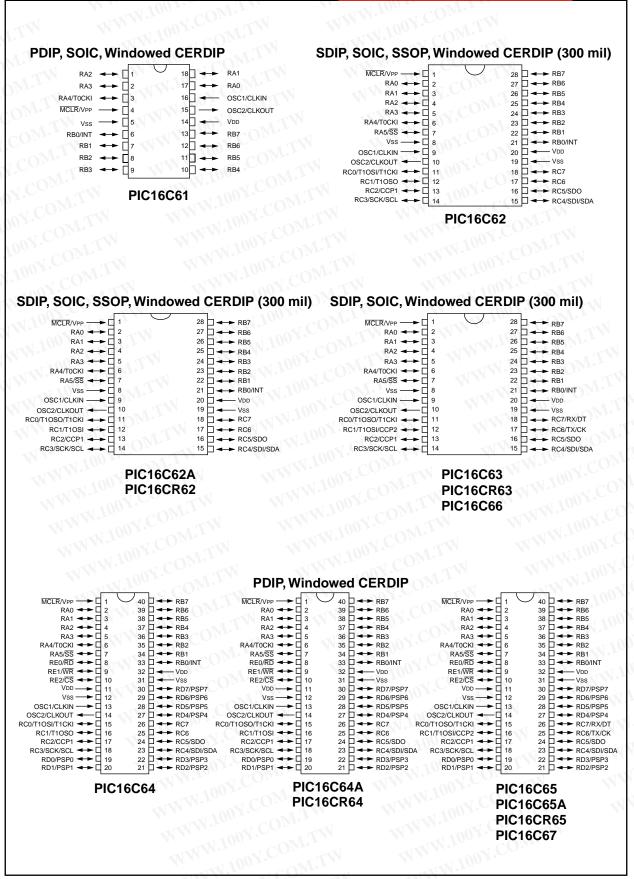
- Low-power, high-speed CMOS EPROM/ROM technology
- · Fully static design
- Wide operating voltage range: 2.5V to 6.0V
- Commercial, Industrial, and Extended temperature ranges
- Low-power consumption:
 - < 2 mA @ 5V, 4 MHz
 - 15 μA typical @ 3V, 32 kHz
 - < 1 μA typical standby current

PIC16C6X Peripheral Features:

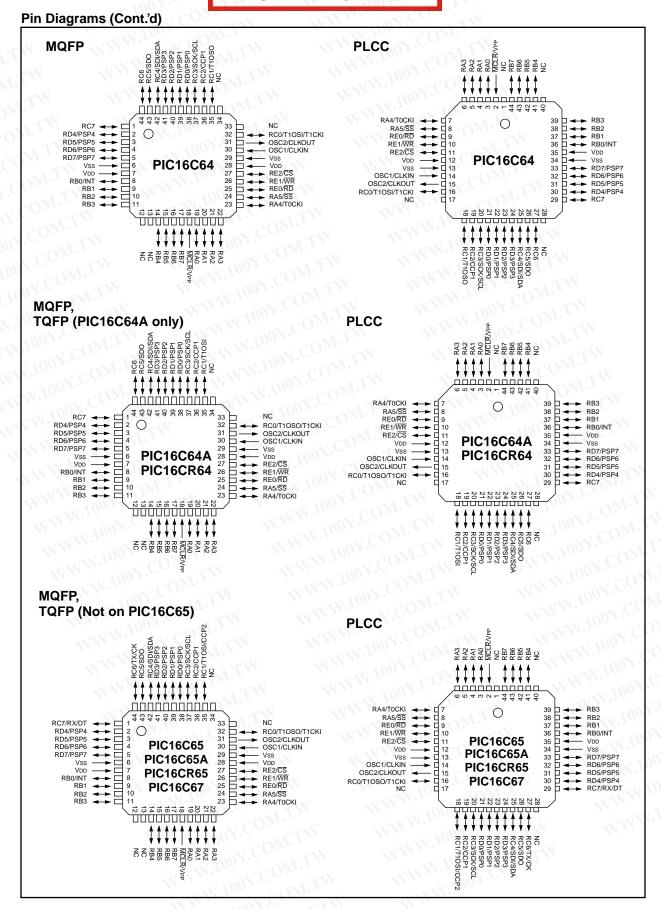
- Timer0: 8-bit timer/counter with 8-bit prescaler
- Timer1: 16-bit timer/counter with prescaler, can be incremented during sleep via external crystal/clock
- Timer2: 8-bit timer/counter with 8-bit period register, prescaler and postscaler
- Capture/Compare/PWM (CCP) module(s)
- Capture is 16-bit, max resolution is 12.5 ns, Compare is 16-bit, max resolution is 200 ns, PWM max resolution is 10-bit.
- Synchronous Serial Port (SSP) with SPI[™] and I²C[™]
- Universal Synchronous Asynchronous Receiver Transmitter (USART/SCI)
- Parallel Slave Port (PSP) 8-bits wide, with external RD, WR and CS controls
- Brown-out detection circuitry for Brown-out Reset (BOR)

PIC16C6X Features	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67
Program Memory (EPROM) x 14	1K	2K	2K	\ <u> </u>	4K	NAM.	2K	2K	O _Ž y	4K	4K	W	8K	8K
(ROM) x 14	=1	GO	17.	2K	_	4K	15		2K	TVT.	_	4K	M	. Const. !
Data Memory (Bytes) x 8	36	128	128	128	192	192	128	128	128	192	192	192	368	368
I/O Pins	13	22	22	22	22	22	33	33	33	33	33	33	22	33
Parallel Slave Port	_	N L C	O _E	-1	_	-1	Yes	Yes	Yes	Yes	Yes	Yes	MAG.	Yes
Capture/Compare/PWM Module(s)	170	00Y.	1	1	2	2	1	1	01.0	2	2	2	2	2
Timer Modules	1	3	3	3	3	3	3	3	3	3	3	3	3	3
Serial Communication	NAN	SPI/ I ² C	SPI/ I ² C	SPI/ I ² C	SPI/I ² C, USART	SPI/I ² C, USART	SPI/ I ² C	SPI/ I ² C	SPI/ I ² C	SPI/I ² C, USART				
In-Circuit Serial Programming	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Brown-out Reset	W.Z.	- 31 1	Yes	Yes	Yes	Yes	_	Yes	Yes	$00\overline{x}$.	Yes	Yes	Yes	Yes
Interrupt Sources	- 3	7	7	7	10	10	8	8	8	11	11	11	10	11
Sink/Source Current (mA)	25/20	25/25	25/25	25/25	25/25	25/25	25/25	25/25	25/25	25/25	25/25	25/25	25/25	25/25

Pin Diagrams



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For register and module descriptions in this data sheet, device legends show which devices apply to those sections. For example, the legend below shows that some features of only the PIC16C62A, PIC16CR62, PIC16C63, PIC16C64A, PIC16CR64, and PIC16C65A are described in this section.

Applicable Devices

61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

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1.0 GENERAL DESCRIPTION

The PIC16CXX is a family of low-cost, high-performance, CMOS, fully-static, 8-bit microcontrollers.

All PIC16/17 microcontrollers employ an advanced RISC architecture. The PIC16CXX microcontroller family has enhanced core features, eight-level deep stack, and multiple internal and external interrupt sources. The separate instruction and data buses of the Harvard architecture allow a 14-bit wide instruction word with separate 8-bit wide data. The two stage instruction pipeline allows all instructions to execute in a single cycle, except for program branches (which require two cycles). A total of 35 instructions (reduced instruction set) are available. Additionally, a large register set gives some of the architectural innovations used to achieve a very high performance.

PIC16CXX microcontrollers typically achieve a 2:1 code compression and a 4:1 speed improvement over other 8-bit microcontrollers in their class.

The **PIC16C61** device has 36 bytes of RAM and 13 I/O pins. In addition a timer/counter is available.

The PIC16C62/62A/R62 devices have 128 bytes of RAM and 22 I/O pins. In addition, several peripheral features are available, including: three timer/counters, one Capture/Compare/PWM module and one serial port. The Synchronous Serial Port can be configured as either a 3-wire Serial Peripheral Interface (SPI™) or the two-wire Inter-Integrated Circuit (I²C) bus.

The PIC16C63/R63 devices have 192 bytes of RAM, while the PIC16C66 has 368 bytes. All three devices have 22 I/O pins. In addition, several peripheral features are available, including: three timer/counters, two Capture/Compare/PWM modules and two serial ports. The Synchronous Serial Port can be configured as either a 3-wire Serial Peripheral Interface (SPI) or the two-wire Inter-Integrated Circuit (I²C) bus. The Universal Synchronous Asynchronous Receiver Transmitter (USART) is also know as a Serial Communications Interface or SCI.

The PIC16C64/64A/R64 devices have 128 bytes of RAM and 33 I/O pins. In addition, several peripheral features are available, including: three timer/counters, one Capture/Compare/PWM module and one serial port. The Synchronous Serial Port can be configured as either a 3-wire Serial Peripheral Interface (SPI) or the two-wire Inter-Integrated Circuit (I²C) bus. An 8-bit Parallel Slave Port is also provided.

The **PIC16C65/65A/R65** devices have 192 bytes of RAM, while the **PIC16C67** has 368 bytes. All four devices have 33 I/O pins. In addition, several peripheral features are available, including: three timer/counters, two Capture/Compare/PWM modules and two serial ports. The Synchronous Serial Port can be configured as either a 3-wire Serial Peripheral Interface (SPI) or the two-wire Inter-Integrated Circuit (I²C) bus. The Universal Synchronous Asynchronous Receiver Transmit-

ter (USART) is also known as a Serial Communications Interface or SCI. An 8-bit Parallel Slave Port is also provided.

The PIC16C6X device family has special features to reduce external components, thus reducing cost, enhancing system reliability and reducing power consumption. There are four oscillator options, of which the single pin RC oscillator provides a low-cost solution, the LP oscillator minimizes power consumption, XT is a standard crystal, and the HS is for High Speed crystals. The SLEEP (power-down) mode offers a power saving mode. The user can wake the chip from SLEEP through several external and internal interrupts, and resets

A highly reliable Watchdog Timer with its own on-chip RC oscillator provides protection against software lock-up.

A UV erasable CERDIP packaged version is ideal for code development, while the cost-effective One-Time-Programmable (OTP) version is suitable for production in any volume.

The PIC16C6X family fits perfectly in applications ranging from high-speed automotive and appliance control to low-power remote sensors, keyboards and telecom processors. The EPROM technology makes customization of application programs (transmitter codes, motor speeds, receiver frequencies, etc.) extremely fast and convenient. The small footprint packages make this microcontroller series perfect for all applications with space limitations. Low-cost, low-power, high performance, ease-of-use, and I/O flexibility make the PIC16C6X very versatile even in areas where no microcontroller use has been considered before (e.g. timer functions, serial communication, capture and compare, PWM functions, and co-processor applications).

1.1 Family and Upward Compatibility

Those users familiar with the PIC16C5X family of microcontrollers will realize that this is an enhanced version of the PIC16C5X architecture. Please refer to Appendix A for a detailed list of enhancements. Code written for PIC16C5X can be easily ported to PIC16CXX family of devices (Appendix B).

1.2 Development Support

PIC16C6X devices are supported by the complete line of Microchip Development tools.

Please refer to Section 15.0 for more details about Microchip's development tools.

TABLE 1-1: PIC16C6X FAMILY OF DEVICES

	PIC16C61	PIC16C62A	PIC16CR62	PIC16C63	PIC16CR63
Maximum Frequency of Operation (MHz)	20	20	20 CO	20	20
EPROM Program Memory (x14 words)	1K	2K	N.100 Y.C.	4K	
ROM Program Memory (x14 words)	CONTIN	_ //	2K	COMITY	4K
Data Memory (bytes)	36	128	128	192	192
Timer Module(s)	TMR0	TMR0, TMR1, TMR2	TMR0, TMR1, TMR2	TMR0, TMR1, TMR2	TMR0, TMR1, TMR2
Capture/Compare/ PWM Module(s)	OAL COM	1	111111111111111111111111111111111111111	2	2
Serial Port(s) (SPI/I ² C, USART)	1 ADY. COM	SPI/I ² C	SPI/I ² C	SPI/I ² C, USART	SPI/I ² C USART
Parallel Slave Port	I TOO	<u></u>	- WWW	· CC	N. A.
Interrupt Sources	3 (00)	7	7	10	10
I/O Pins	13	22	22	22	22
Voltage Range (Volts)	3.0-6.0	2.5-6.0	2.5-6.0	2.5-6.0	2.5-6.0
In-Circuit Serial Programming	Yes	Yes	Yes	Yes	Yes
Brown-out Reset	1007	Yes	Yes	Yes	Yes
Packages	18-pin DIP, SO	28-pin SDIP, SOIC, SSOP	28-pin SDIP, SOIC, SSOP	28-pin SDIP, SOIC	28-pin SDIP, SOIC
	of Operation (MHz) EPROM Program Memory (x14 words) ROM Program Memory (x14 words) Data Memory (bytes) Timer Module(s) Capture/Compare/ PWM Module(s) Serial Port(s) (SPI/I ² C, USART) Parallel Slave Port Interrupt Sources I/O Pins Voltage Range (Volts) In-Circuit Serial Programming Brown-out Reset	Maximum Frequency of Operation (MHz) EPROM Program Memory (x14 words) ROM Program Memory (x14 words) Data Memory (bytes) Timer Module(s) Capture/Compare/ PWM Module(s) Serial Port(s) (SPI/I ² C, USART) Parallel Slave Port Interrupt Sources 3 I/O Pins Voltage Range (Volts) Brown-out Reset 1K TK 1K 1K 1K 1K 1K 1K 1K 1K	Maximum Frequency of Operation (MHz) 20 20 EPROM Program Memory (x14 words) 1K 2K ROM Program Memory (x14 words) — — Data Memory (bytes) 36 128 Timer Module(s) TMR0 TMR0, TMR1, TMR2 Capture/Compare/PWM Module(s) — 1 Serial Port(s) (SPI/I²C, USART) — SPI/I²C Parallel Slave Port — — Interrupt Sources 3 7 I/O Pins 13 22 Voltage Range (Volts) 3.0-6.0 2.5-6.0 In-Circuit Serial Programming Yes Brown-out Reset — Yes Packages 18-pin DIP, SO 28-pin SDIP,	Maximum Frequency of Operation (MHz) 20 20 20 EPROM Program Memory (x14 words) 1K 2K — ROM Program Memory (x14 words) — — 2K Data Memory (bytes) 36 128 128 Timer Module(s) TMR0 TMR0, TMR0, TMR1, TMR1, TMR2 TMR2 Capture/Compare/PWM Module(s) — 1 1 Serial Port(s) (SPI/I²C, USART) — SPI/I²C SPI/I²C Parallel Slave Port — — — Interrupt Sources 3 7 7 I/O Pins 13 22 22 Voltage Range (Volts) 3.0-6.0 2.5-6.0 2.5-6.0 In-Circuit Serial Programming Yes Yes Brown-out Reset — Yes Yes Packages 18-pin DIP, SO 28-pin SDIP, 28-pin SDIP,	Maximum Frequency of Operation (MHz) 20 20 20 20 EPROM Program Memory (x14 words) 1K 2K — 4K ROM Program Memory (x14 words) — — 2K — Data Memory (bytes) 36 128 128 192 Timer Module(s) TMR0 TMR0, TMR0, TMR0, TMR1, TMR1, TMR1, TMR2 TMR2 TMR2 Capture/Compare/PWM Module(s) — 1 1 2 Serial Port(s) (SPI/I²C, USART) — SPI/I²C SPI/I²C SPI/I²C, USART Parallel Slave Port — — — — — Interrupt Sources 3 7 7 10 I/O Pins 13 22 22 22 Voltage Range (Volts) 3.0-6.0 2.5-6.0 2.5-6.0 2.5-6.0 2.5-6.0 In-Circuit Serial Programming Yes Yes Yes Yes Packages 18-pin DIP, SO 28-pin SDIP, 28-pin SDIP, 28-pin SDIP,

		PIC16C64A	PIC16CR64	PIC16C65A	PIC16CR65	PIC16C66	PIC16C67
Clock	Maximum Frequency of Operation (MHz)	20	20	20	20	20	20
	EPROM Program Memory (x14 words)	2K	4.100 X.C	4K	- 1	8K	8K
Memory	ROM Program Memory (x14 words)	- 111	2K	COMITY	4K	NW.	MA'CO
	Data Memory (bytes)	128	128	192	192	368	368
	Timer Module(s)	TMR0, TMR1, TMR2	TMR0, TMR1, TMR2	TMR0, TMR1, TMR2	TMR0, TMR1, TMR2	TMR0, TMR1, TMR2	TMR0, TMR1, TMR2
Peripherals	Capture/Compare/PWM Mod- ule(s)	1	1	2 00 Y.CON	2	2	2
	Serial Port(s) (SPI/I ² C, USART)	SPI/I ² C	SPI/I ² C	SPI/I ² C, USART	SPI/I ² C, USART	SPI/I ² C, USART	SPI/I ² C, USART
	Parallel Slave Port	Yes	Yes	Yes	Yes	_ ~	Yes
	Interrupt Sources	8	8	11	11	10	11
	I/O Pins	33	33	33	33	22	33
	Voltage Range (Volts)	2.5-6.0	2.5-6.0	2.5-6.0	2.5-6.0	2.5-6.0	2.5-6.0
	In-Circuit Serial Programming	Yes	Yes	Yes	Yes	Yes	Yes
Features	Brown-out Reset	Yes	Yes	Yes	Yes	Yes	Yes
	Packages	44-pin PLCC,		40-pin DIP; 44-pin PLCC, MQFP, TQFP	40-pin DIP; 44-pin PLCC, MQFP, TQFP	28-pin SDIP, SOIC	40-pin DIP; 44-pin PLCC, MQFP, TQFP

All PIC16/17 Family devices have Power-on Reset, selectable Watchdog Timer, selectable code protect and high I/O current capability. All PIC16C6X Family devices use serial programming with clock pin RB6 and data pin RB7.

2.0 PIC16C6X DEVICE VARIETIES

A variety of frequency ranges and packaging options are available. Depending on application and production requirements, the proper device option can be selected using the information in the PIC16C6X Product Identification System section at the end of this data sheet. When placing orders, please use that page of the data sheet to specify the correct part number.

For the PIC16C6X family of devices, there are four device "types" as indicated in the device number:

- C, as in PIC16C64. These devices have EPROM type memory and operate over the standard voltage range.
- LC, as in PIC16LC64. These devices have EPROM type memory and operate over an extended voltage range.
- CR, as in PIC16CR64. These devices have ROM program memory and operate over the standard voltage range.
- LCR, as in PIC16LCR64. These devices have ROM program memory and operate over an extended voltage range.

2.1 UV Erasable Devices

The UV erasable version, offered in CERDIP package is optimal for prototype development and pilot programs. This version can be erased and reprogrammed to any of the oscillator modes.

Microchip's PICSTART® Plus and PRO MATE® II programmers both support programming of the PIC16C6X.

2.2 <u>One-Time-Programmable (OTP)</u> Devices

The availability of OTP devices is especially useful for customers who need the flexibility for frequent code updates and small volume applications.

The OTP devices, packaged in plastic packages, permit the user to program them once. In addition to the program memory, the configuration bits must also be programmed.

2.3 Quick-Turnaround-Production (QTP) Devices

Microchip offers a QTP Programming Service for factory production orders. This service is made available for users who choose not to program a medium to high quantity of units and whose code patterns have stabilized. The devices are identical to the OTP devices but with all EPROM locations and configuration options already programmed by the factory. Certain code and prototype verification procedures apply before production shipments are available. Please contact your local Microchip Technology sales office for more details.

2.4 <u>Serialized Quick-Turnaround</u> Production (SQTPSM) Devices

Microchip offers a unique programming service where a few user-defined locations in each device are programmed with different serial numbers. The serial numbers may be random, pseudo-random, or sequential.

Serial programming allows each device to have a unique number which can serve as an entry-code, password, or ID number.

ROM devices do not allow serialization information in the program memory space. The user may have this information programmed in the data memory space.

For information on submitting ROM code, please contact your regional sales office.

2.5 Read Only Memory (ROM) Devices

Microchip offers masked ROM versions of several of the highest volume parts, thus giving customers a low cost option for high volume, mature products.

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3.0 ARCHITECTURAL OVERVIEW

The high performance of the PIC16CXX family can be attributed to a number of architectural features commonly found in RISC microprocessors. To begin with, the PIC16CXX uses a Harvard architecture, in which, program and data are accessed from separate memories using separate buses. This improves bandwidth over traditional von Neumann architecture where program and data may be fetched from the same memory using the same bus. Separating program and data busses further allows instructions to be sized differently than 8-bit wide data words. Instruction opcodes are 14-bits wide making it possible to have all single word instructions. A 14-bit wide program memory access bus fetches a 14-bit instruction in a single cycle. A twostage pipeline overlaps fetch and execution of instructions (Example 3-1). Consequently, all instructions execute in a single cycle (200 ns @ 20 MHz) except for program branches.

The PIC16C61 addresses 1K x 14 of program memory. The PIC16C62/62A/R62/64/64A/R64 address 2K x 14 of program memory, and the PIC16C63/R63/65/65A/R65 devices address 4K x 14 of program memory. The PIC16C66/67 address 8K x 14 program memory. All program memory is internal.

The PIC16CXX can directly or indirectly address its register files or data memory. All special function registers including the program counter are mapped in the data memory. The PIC16CXX has an orthogonal (symmetrical) instruction set that makes it possible to carry out any operation on any register using any addressing mode. This symmetrical nature and lack of "special optimal situations" makes programming with the PIC16CXX simple yet efficient, thus significantly reducing the learning curve.

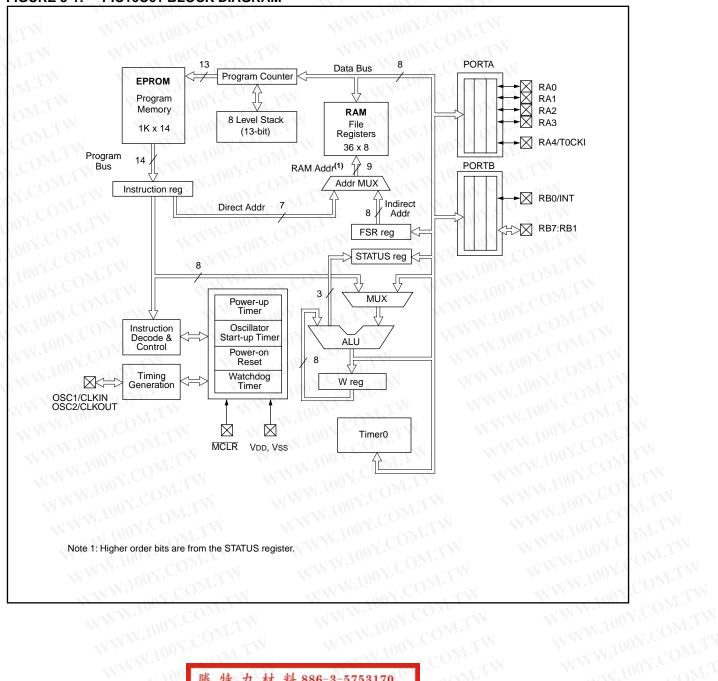
The PIC16CXX device contains an 8-bit ALU and working register (W). The ALU is a general purpose arithmetic unit. It performs arithmetic and Boolean functions between data in the working register and any register file.

The ALU is 8-bits wide and capable of addition, subtraction, shift, and logical operations. Unless otherwise mentioned, arithmetic operations are two's complement in nature. In two-operand instructions, typically one operand is the working register (W register), the other operand is a file register or an immediate constant. In single operand instructions, the operand is either the W register or a file register.

The W register is an 8-bit working register used for ALU operations. It is not an addressable register.

Depending upon the instruction executed, the ALU may affect the values of the Carry (C), Digit Carry (DC), and Zero (Z) bits in the STATUS register. Bits C and DC operate as a $\overline{\text{borrow}}$ and $\overline{\text{digit}}$ $\overline{\text{borrow}}$ out bit, respectively, in subtraction. See the SUBLW and SUBWF instructions for examples.

FIGURE 3-1: PIC16C61 BLOCK DIAGRAM



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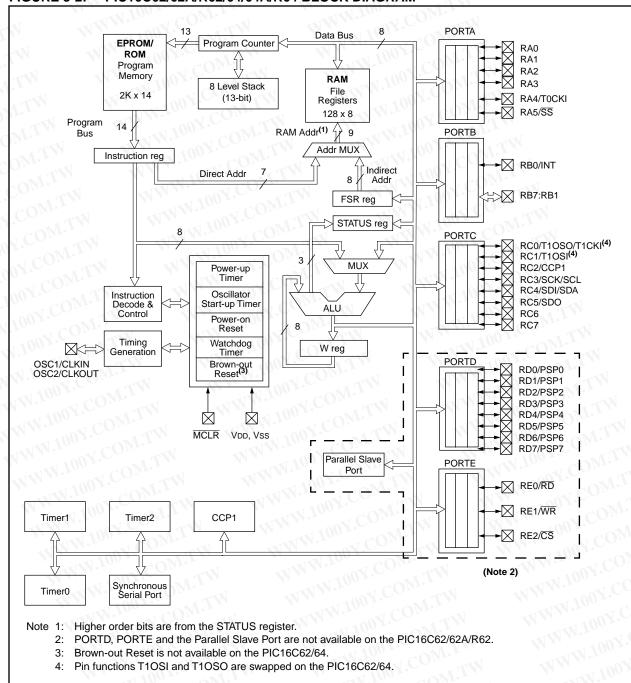


FIGURE 3-2: PIC16C62/62A/R62/64/64A/R64 BLOCK DIAGRAM

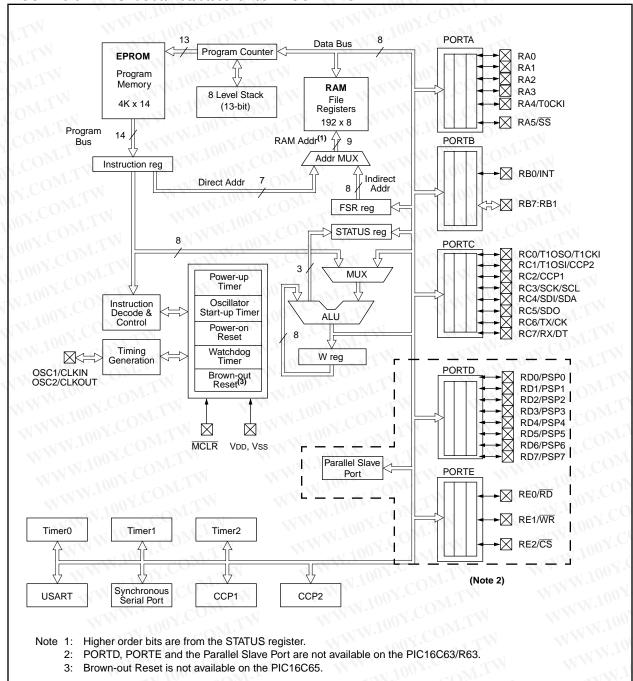


FIGURE 3-3: PIC16C63/R63/65/65A/R65 BLOCK DIAGRAM

13 **PORTA** Data Bus **Program Counter EPROM** RA0 RA1 Program RA2 Memory RAM RA3 8 Level Stack File RA4/T0CKI 8K x 14 (13-bit) Registers RA5/SS 368 x 8 Program 14 RAM Addr⁽¹⁾ 9 Bus **PORTB** Addr MUX Instruction reg RB0/INT Indirect Direct Addr 8 Addr RB7:RB1 FSR reg STATUS reg **PORTC** RC0/T1OSO/T1CKI RC1/T1OSI/CCP2 3 MUX RC2/CCP1 Power-up Timer RC3/SCK/SCL RC4/SDI/SDA Oscillator Instruction RC5/SDO Start-up Timer Decode & Control ALU RC6/TX/CK Power-on RC7/RX/DT 8 Reset Timing Generation Watchdog W reg Timer OSC1/CLKIN OSC2/CLKOUT PORTD Brown-out RD0/PSP0 Reset RD1/PSP1 RD2/PSP2 RD3/PSP3 RD4/PSP4 × 囟 RD5/PSP5 RD6/PSP6 MCLR VDD, VSS RD7/PSP7 Parallel Slave **PORTE** Port ► RE0/RD RE1/WR Timer0 Timer1 Timer2 RE2/CS (Note 2) Synchronous Serial Port USART CCP1 CCP2 Note 1: Higher order bits are from the STATUS register. PORTD, PORTE and the Parallel Slave Port are not available on the PIC16C66.

FIGURE 3-4: PIC16C66/67 BLOCK DIAGRAM

PIC16C61 PINOUT DESCRIPTION **TABLE 3-1:**

Pin Name	DIP Pin#	SOIC Pin#	Pin Type	Buffer Type	Description
OSC1/CLKIN	16	16		ST/CMOS ⁽¹⁾	Oscillator crystal input/external clock source input.
OSC2/CLKOUT	15	15	N.O OY.CO	M.TW	Oscillator crystal output. Connects to crystal or resonator in crystal oscillator mode. In RC mode, the pin outputs CLKOUT which has 1/4 the frequency of OSC1, and denotes the instruction cycle rate.
MCLR/VPP	4	4	I/P	ST	Master clear reset input or programming voltage input. This pin is an active low reset to the device.
COLUMN	1	NA	1007.	TILLE	PORTA is a bi-directional I/O port.
RA0	17	17	I/O	COTTL	N WWW. any. Com. TW
RA1	18	18	I/O	TTL	COM.
RA2	1	1	I/O	TTL	M. 100x. ON 11
RA3	2	2	I/O	TTL	TW WWW. OOY.CO. TW
RA4/T0CKI	3	3	I/O	ST	RA4 can also be the clock input to the Timer0 timer/counter. Output is open drain type.
TOON COM	TW		MAN	OOX.CO	PORTB is a bi-directional I/O port. PORTB can be software programmed for internal weak pull-up on all inputs.
RB0/INT	6	6	I/O	TTL/ST ⁽²⁾	RB0 can also be the external interrupt pin.
RB1	7	7	I/O	TTL	DM. TAN M. TO COM.
RB2	8	8	I/O	TTL	WILL M. TOW. COMILLY
RB3	9	9	I/O	TTL	WWW. 100X.CONTR
RB4	10	10	I/O	TTL	Interrupt on change pin.
RB5	11	11	I/O	TTLOU	Interrupt on change pin.
RB6	12	12	I/O	TTL/ST ⁽³⁾	Interrupt on change pin. Serial programming clock.
RB7	13	13	I/O	TTL/ST ⁽³⁾	Interrupt on change pin. Serial programming data.
Vss	5	5	Р	- 	Ground reference for logic and I/O pins.
VDD	14	14	Р	MAG	Positive supply for logic and I/O pins.

Legend: I = input

O = output

I/O = input/output

P = power

- = Not used

TTL = TTL input

ST = Schmitt Trigger input

WWW.100Y.COM.TW Note 1: This buffer is a Schmitt Trigger input when configured in RC oscillator mode and a CMOS input otherwise.

W.100Y.COM

2: This buffer is a Schmitt Trigger input when configured as the external interrupt.

3: This buffer is a Schmitt Trigger input when used in serial programming mode.

TABLE 3-2: PIC16C62/62A/R62/63/R63/66 PINOUT DESCRIPTION

Pin Name	Pin#	Pin Type	Buffer Type	Description
OSC1/CLKIN	9	TIMO	ST/CMOS ⁽³⁾	Oscillator crystal input/external clock source input.
OSC2/CLKOUT	10	COM.	TAN —	Oscillator crystal output. Connects to crystal or resonator in crystal oscillator mode. In RC mode, the pin outputs CLKOUT which has 1/4 the frequency of OSC1, and denotes the instruction cycle rate.
MCLR/VPP	110	I/P	ST	Master clear reset input or programming voltage input. This pin is an active low reset to the device.
OM-	TOWN.	-7 CC	NA.	PORTA is a bi-directional I/O port.
RA0	2	I/O	TTL	M. TN TOO I. COM! I.
RA1	3	1/0	TTL	WWW. 100X.CO. TW
RA2	4	I/O	OTTL	COM.
RA3	5	1/0	TIL	M. 1001. OM. 1.
RA4/T0CKI	6	I/O	ST	RA4 can also be the clock input to the Timer0 timer/counter. Output is open drain type.
RA5/SS	7	1/0	TILM	RA5 can also be the slave select for the synchronous serial port.
ON COM.		WW.I	ON.COM	PORTB is a bi-directional I/O port. PORTB can be software programmed for internal weak pull-up on all inputs.
RB0/INT	21	1/0	TTL/ST(4)	RB0 can also be the external interrupt pin.
RB1	22	I/O	100 TTL	MILL COM.
RB2	23	I/O	TTL	WW. TIOOY.CONT.TW
RB3	24	I/O	TTL	DM. THE WAY COME
RB4	25	I/O	1TL	Interrupt on change pin.
RB5	26	I/O	TTL	Interrupt on change pin.
RB6	27	I/O	TTL/ST ⁽⁵⁾	Interrupt on change pin. Serial programming clock.
RB7	28	I/O	TTL/ST ⁽⁵⁾	Interrupt on change pin. Serial programming data.
NAME OF COMMENTAL OF THE PROPERTY OF THE PROPE	TW	1	1100	PORTC is a bi-directional I/O port.
RC0/T10SO ⁽¹⁾ /T1CKI	11	I/O	ST	RC0 can also be the Timer1 oscillator output ⁽¹⁾ or Timer1 clock input.
RC1/T1OSI ⁽¹⁾ /CCP2 ⁽²⁾	12	I/O	ST	RC1 can also be the Timer1 oscillator input ⁽¹⁾ or Capture2 input/Compare2 output/PWM2 output ⁽²⁾ .
RC2/CCP1	13	I/O	ST	RC2 can also be the Capture1 input/Compare1 out-put/PWM1 output.
RC3/SCK/SCL	14	I/O	ST	RC3 can also be the synchronous serial clock input/output for both SPI and I ² C modes.
RC4/SDI/SDA	15	I/O	ST	RC4 can also be the SPI Data In (SPI mode) or data I/O (I ² C mode).
RC5/SDO	16	I/O	ST	RC5 can also be the SPI Data Out (SPI mode).
RC6/TX/CK ⁽²⁾	17	I/O	ST	RC6 can also be the USART Asynchronous Transmit ⁽²⁾ or Synchronous Clock ⁽²⁾ .
RC7/RX/DT ⁽²⁾	18	I/O	ST	RC7 can also be the USART Asynchronous Receive ⁽²⁾ or Synchronous Data ⁽²⁾ .
Vss	8,19	Р	W _	Ground reference for logic and I/O pins.
VDD	20	P		Positive supply for logic and I/O pins.

Legend: I = input O =

O = output

— = Not used

I/O = input/output TTL = TTL input P = power

-- = Not used TTL = TTL input ST = Schmitt Trigger input Note 1: Pin functions T1OSO and T1OSI are reversed on the PIC16C62.

- 2: The USART and CCP2 are not available on the PIC16C62/62A/R62.
- 3: This buffer is a Schmitt Trigger input when configured in RC oscillator mode and a CMOS input otherwise.
- 4: This buffer is a Schmitt Trigger input when configured as the external interrupt.
- 5: This buffer is a Schmitt Trigger input when used in serial programming mode.

TABLE 3-3: PIC16C64/64A/R64/65/65A/R65/67 PINOUT DESCRIPTION

Pin Name	DIP Pin#	PLCC Pin#	TQFP MQFP Pin#	Pin Type	Buffer Type	Description
OSC1/CLKIN	13	14	30	M.T.Y	ST/CMOS ⁽³⁾	Oscillator crystal input/external clock source input.
OSC2/CLKOUT	14	15	31	OM.		Oscillator crystal output. Connects to crystal or resonator in crystal oscillator mode. In RC mode, the pin outputs CLK-OUT which has 1/4 the frequency of OSC1, and denotes the instruction cycle rate.
MCLR/VPP	1	2	18	I/P	ST	Master clear reset input or programming voltage input. This pin is an active low reset to the device.
COMP			700	100	- 1	PORTA is a bi-directional I/O port.
RA0	2	3	19	I/O	TTL	M. 21 1001.
RA1 CONTRACT	3	4	20	1/0	TTL	WWW. CON.CO.
RA2	4	5	21	I/O	TTL	M. To COM.
RA3	5	6	22	1/0	TTL	M. MINTONIA
RA4/T0CKI	6	7	23	1/0	ST	RA4 can also be the clock input to the Timer0 timer/counter. Output is open drain type.
RA5/SS	7	8	24	I/O	TILL.T	RA5 can also be the slave select for the synchronous serial port.
AN.100X.COM	TW		WW	N.100	N.COM	PORTB is a bi-directional I/O port. PORTB can be software programmed for internal weak pull-up on all inputs.
RB0/INT	33	36	8	1/0	TTL/ST ⁽⁴⁾	RB0 can also be the external interrupt pin.
RB1	34	37	9	I/O	TTL	1.11, W. 100 . COW. 1.
RB2	35	38	10	I/O	TTL	TTW WW. TIOOY.C. WITH
RB3	36	39	11	1/0	TTLC	MAN TANK TANK
RB4	37	41	14	I/O	10TTL	Interrupt on change pin.
RB5	38	42	15	I/O	TTL	Interrupt on change pin.
RB6	39	43	16	I/O	TTL/ST ⁽⁵⁾	Interrupt on change pin. Serial programming clock.
RB7	40	44	17	I/O	TTL/ST ⁽⁵⁾	Interrupt on change pin. Serial programming data.
MAN	C	TTV		11/1	1003	PORTC is a bi-directional I/O port.
RC0/T10SO ⁽¹⁾ /T1CKI	15	16	32	I/O	ST	RC0 can also be the Timer1 oscillator output ⁽¹⁾ or Timer1 clock input.
RC1/T1OSI ⁽¹⁾ /CCP2 ⁽²⁾	16	18	35	I/O	ST	RC1 can also be the Timer1 oscillator input ⁽¹⁾ or Capture2 input/Compare2 output/PWM2 output ⁽²⁾ .
RC2/CCP1	17	19	36	I/O	ST	RC2 can also be the Capture1 input/Compare1 out- put/PWM1 output.
RC3/SCK/SCL	18	20	37	I/O	ST	RC3 can also be the synchronous serial clock input/out- put for both SPI and I ² C modes.
RC4/SDI/SDA	23	25	42	N/O	ST	RC4 can also be the SPI Data In (SPI mode) or data I/O (I ² C mode).
RC5/SDO	24	26	43	1/0	ST	RC5 can also be the SPI Data Out (SPI mode).
RC6/TX/CK ⁽²⁾	25	27	44	I/O	ST	RC6 can also be the USART Asynchronous Transmit ⁽²⁾ or Synchronous Clock ⁽²⁾ .
RC7/RX/DT ⁽²⁾	26	29	CON	I/O	ST	RC7 can also be the USART Asynchronous Receive ⁽²⁾ or Synchronous Data ⁽²⁾ .

Legend: I = input

O = output

I/O = input/output

P = power

— = Not used TTL = TTL input ST = Schmitt Trigger input

- Note 1: Pin functions T1OSO and T1OSI are reversed on the PIC16C64.
 - 2: CCP2 and the USART are not available on the PIC16C64/64A/R64.
 - 3: This buffer is a Schmitt Trigger input when configured in RC oscillator mode and a CMOS input otherwise.
 - 4: This buffer is a Schmitt Trigger input when configured as the external interrupt.
 - 5: This buffer is a Schmitt Trigger input when used in serial programming mode.
 - 6: This buffer is a Schmitt Trigger input when configured as general purpose I/O and a TTL input when used in the Parallel Slave Port mode (for interfacing to a microprocessor bus).

PIC16C64/64A/R64/65/65A/R65/67 PINOUT DESCRIPTION (Cont.'d) **TABLE 3-3:**

Pin Name		DIP Pin#	PLCC Pin#	TQFP MQFP Pin#	Pin Type	Buffer Type	Description
TW	WV	W.F	007.C	OMI	W	MM	PORTD can be a bi-directional I/O port or parallel slave por for interfacing to a microprocessor bus.
RD0/PSP0		19	21	38	I/O	ST/TTL ⁽⁶⁾	1100Y.COTW
RD1/PSP1		20	22	39	I/O	ST/TTL ⁽⁶⁾	MN. CON. COM
RD2/PSP2		21	23	40	I/O	ST/TTL ⁽⁶⁾	M. 100 COM. I
RD3/PSP3		22	24	41	I/O	ST/TTL ⁽⁶⁾	100Y. SM.TW
RD4/PSP4		27	30	2	I/O	ST/TTL ⁽⁶⁾	NWW. ON COM TW
RD5/PSP5		28	31	3	I/O	ST/TTL ⁽⁶⁾	COM.
RD6/PSP6		29	32	4	I/O	ST/TTL ⁽⁶⁾	WW. 1007.
RD7/PSP7		30	33	5	I/O	ST/TTL ⁽⁶⁾	WWW. ON. CO. TW
RE0/RD RE1/WR RE2/CS	TW	8 9 10	9 10 11	25 26 27	I/O I/O I/O	ST/TTL ⁽⁶⁾ ST/TTL ⁽⁶⁾ ST/TTL ⁽⁶⁾	PORTE is a bi-directional I/O port. RE0 can also be read control for the parallel slave por RE1 can also be write control for the parallel slave por RE2 can also be select control for the parallel slave por
Vss	WILL	12,31	13,34	6,29	Р	MIT IN	Ground reference for logic and I/O pins.
VDD	TI	11,32	12,35	7,28	P.C	-rW	Positive supply for logic and I/O pins.
NC C	OM.	N —	1,17, 28,40	12,13, 33,34	100X.	ON L	These pins are not internally connected. These pins should be left unconnected.

Note 1: Pin functions T1OSO and T1OSI are reversed on the PIC16C64.

- 2: CCP2 and the USART are not available on the PIC16C64/64A/R64.
- 3: This buffer is a Schmitt Trigger input when configured in RC oscillator mode and a CMOS input otherwise.
- 4: This buffer is a Schmitt Trigger input when configured as the external interrupt.
- 5: This buffer is a Schmitt Trigger input when used in serial programming mode.
- 6: This buffer is a Schmitt Trigger input when configured as general purpose I/O and a TTL input when used in the Parallel Slave Port mode (for interfacing to a microprocessor bus).

3.1 Clocking Scheme/Instruction Cycle

The clock input (from OSC1) is internally divided by four to generate four non-overlapping quadrature clocks namely Q1, Q2, Q3, and Q4. Internally, the program counter (PC) is incremented every Q1, the instruction is fetched from the program memory and latched into the instruction register in Q4. The instruction is decoded and executed during the following Q1 through Q4. The clock and instruction execution flow is shown in Figure 3-5.

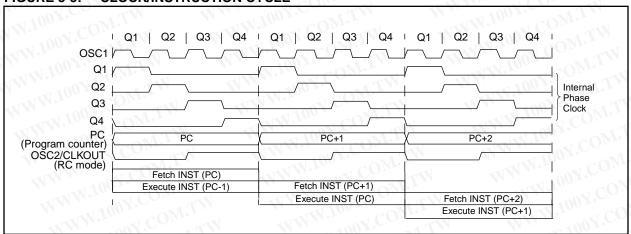
3.2 <u>Instruction Flow/Pipelining</u>

An "Instruction Cycle" consists of four Q cycles (Q1, Q2, Q3, and Q4). The instruction fetch and execute are pipelined such that fetch takes one instruction cycle while decode and execute takes another instruction cycle. However, due to the pipelining, each instruction effectively executes in one cycle. If an instruction causes the program counter to change (e.g. GOTO) then two cycles are required to complete the instruction (Example 3-1).

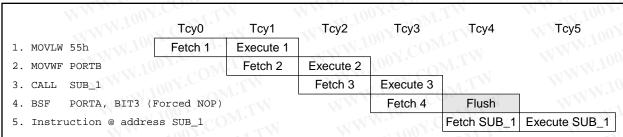
A fetch cycle begins with the program counter (PC) incrementing in Q1.

In the execution cycle, the fetched instruction is latched into the "Instruction Register (IR)" in cycle Q1. This instruction is then decoded and executed during the Q2, Q3, and Q4 cycles. Data memory is read during Q2 (operand read) and written during Q4 (destination write).





EXAMPLE 3-1: INSTRUCTION PIPELINE FLOW



All instructions are single cycle, except for any program branches. These take two cycles since the fetch instruction is "flushed" from the pipeline while the new instruction is being fetched and then executed.

4.0 MEMORY ORGANIZATION

Applicable Devices
61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

4.1 <u>Program Memory Organization</u>

The PIC16C6X family has a 13-bit program counter capable of addressing an 8K x 14 program memory space. The amount of program memory available to each device is listed below:

Device	Program Memory	Address Range
PIC16C61	1K x 14	0000h-03FFh
PIC16C62	2K x 14	0000h-07FFh
PIC16C62A	2K x 14	0000h-07FFh
PIC16CR62	2K x 14	0000h-07FFh
PIC16C63	4K x 14	0000h-0FFFh
PIC16CR63	4K x 14	0000h-0FFFh
PIC16C64	2K x 14	0000h-07FFh
PIC16C64A	2K x 14	0000h-07FFh
PIC16CR64	2K x 14	0000h-07FFh
PIC16C65	4K x 14	0000h-0FFFh
PIC16C65A	4K x 14	0000h-0FFFh
PIC16CR65	4K x 14	0000h-0FFFh
PIC16C66	8K x 14	0000h-1FFFh
PIC16C67	8K x 14	0000h-1FFFh

For those devices with less than 8K program memory, accessing a location above the physically implemented address will cause a wraparound.

The reset vector is at 0000h and the interrupt vector is at 0004h.

FIGURE 4-1: PIC16C61 PROGRAM
MEMORY MAP AND STACK

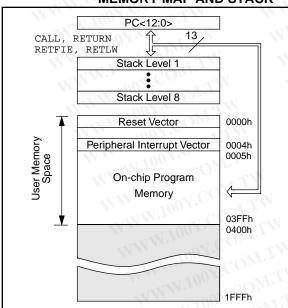


FIGURE 4-2: PIC16C62/62A/R62/64/64A/ R64 PROGRAM MEMORY MAP AND STACK

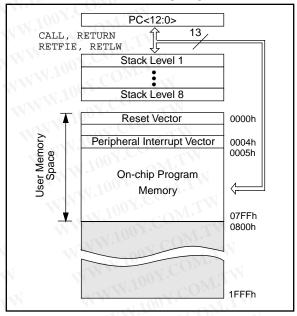


FIGURE 4-3: PIC16C63/R63/65/65A/R65 PROGRAM MEMORY MAP AND STACK

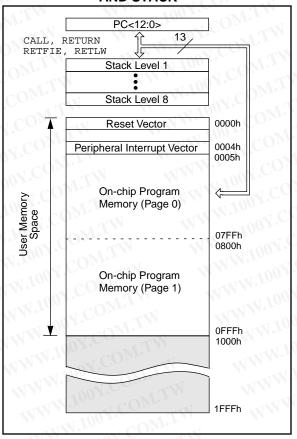
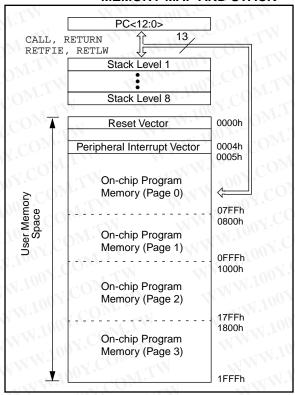


FIGURE 4-4: PIC16C66/67 PROGRAM MEMORY MAP AND STACK



4.2 Data Memory Organization

 Applicable Devices

 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

The data memory is partitioned into multiple banks which contain the General Purpose Registers and the Special Function Registers. Bits RP1 and RP0 are the bank select bits.

RP1:RP0 (STATUS<6:5>)

- $= 00 \rightarrow Bank0$
- = $01 \rightarrow Bank1$
- = $10 \rightarrow Bank2$
- = $11 \rightarrow Bank3$

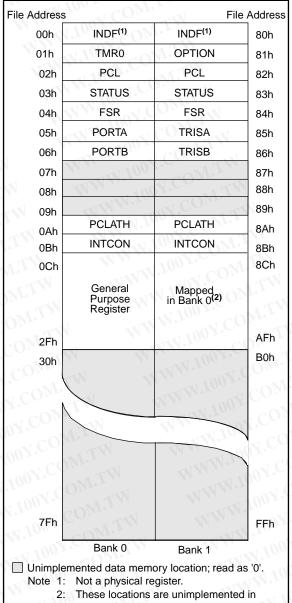
Each bank extends up to 7Fh (128 bytes). The lower locations of each bank are reserved for the Special Function Registers. Above the Special Function Registers are General Purpose Registers, implemented as static RAM. All implemented banks contain special function registers. Some "high use" special function registers from one bank may be mirrored in another bank for code reduction and quicker access.

4.2.1 GENERAL PURPOSE REGISTERS

These registers are accessed either directly or indirectly through the File Select Register (FSR) (Section 4.5).

For the PIC16C61, general purpose register locations 8Ch-AFh of Bank 1 are not physically implemented. These locations are mapped into 0Ch-2Fh of Bank 0.

FIGURE 4-5: PIC16C61 REGISTER FILE MAP



 These locations are unimplemented in Bank 1. Any access to these locations will access the corresponding Bank 0 register.

FIGURE 4-6: PIC16C62/62A/R62/64/64A/ R64 REGISTER FILE MAP

File Addre	ess		File Address
00h	INDF ⁽¹⁾	INDF ⁽¹⁾	80h
01h	TMR0	OPTION	81h
02h	PCL	PCL	82h
03h	STATUS	STATUS	83h
04h	FSR	FSR	84h
05h	PORTA	TRISA	85h
06h	PORTB	TRISB	86h
07h	PORTC	TRISC	87h
08h	PORTD ⁽²⁾	TRISD ⁽²⁾	88h
09h	PORTE ⁽²⁾	TRISE ⁽²⁾	89h
0Ah	PCLATH	PCLATH	8Ah
0Bh	INTCON	INTCON	8Bh
0Ch	PIR1	PIE1	8Ch
0Dh	ON	MMM.	8Dh
0Eh	TMR1L	PCON	8Eh
0Fh	TMR1H	WW	8Fh
10h	T1CON	WA	90h
11h	TMR2	N N	91h
12h	T2CON	PR2	92h
13h	SSPBUF	SSPADD	93h
14h	SSPCON	SSPSTAT	94h
15h	CCPR1L	TW	95h
16h	CCPR1H	M. TW	96h
17h	CCP1CON	DIA.	97h
18h	MMM.100X	COM.TW	98h
1Fh	WWW.10	oy.COM.T	9Fh
20h	General	General Purpose Register	A0h BFh
7Fh	Purpose Register	M.100X.CC	C0h
/Ln		- ×1 100 1.	FFh

FIGURE 4-7: PIC16C63/R63/65/65A/R65 REGISTER FILE MAP

Addre	ss		File Address
00h	INDF ⁽¹⁾	INDF ⁽¹⁾	80h
01h	TMR0	OPTION	81h
02h	PCL	PCL	82h
03h	STATUS	STATUS	83h
04h	FSR	FSR	84h
05h	PORTA	TRISA	85h
06h	PORTB	TRISB	86h
07h	PORTC	TRISC	87h
08h	PORTD ⁽²⁾	TRISD ⁽²⁾	88h
09h	PORTE ⁽²⁾	TRISE ⁽²⁾	89h
0Ah	PCLATH	PCLATH	8Ah
0Bh	INTCON	INTCON	8Bh
0Ch	PIR1	PIE1	8Ch
DDh	PIR2	PIE2	8Dh
)Eh	TMR1L	PCON	8Eh
)Fh	TMR1H	100 X . CO.	8Fh
10h	T1CON	1 100 Y.Co.	90h
11h	TMR2	100Y.CO	91h
12h	T2CON	PR2	92h
13h	SSPBUF	SSPADD	93h
14h	SSPCON V	SSPSTAT	94h
15h	CCPR1L	1100	95h
16h	CCPR1H	WW 100	96h
17h	CCP1CON	WWW 10	97h
18h	RCSTA	TXSTA	98h
19h	TXREG	SPBRG	99h
1Ah	RCREG	MMA	9Ah
1Bh	CCPR2L	WW	9Bh
1Ch	CCPR2H	MA	9Ch
1Dh	CCP2CON	M.	9Dh
Eh	OY.CO	W A	9Eh
1Fh	OON.CON	LAI .	9Fh
20h	General	General	A0h
JWW	Purpose	Purpose	WWW
7Fh	Register	Register	FFh
MAA	Bank 0	Bank 1 emory location; re	

PORTD and PORTE are not available on the PIC16C63/R63.

TWW 100Y.COM

FIGURE 4-8: PIC16C66/67 DATA MEMORY MAP

Indirect addr.(*)	00h	Indirect addr.(*)	.80h	Indirect addr.(*)	100h	Indirect addr.(*)
TMR0	01h	OPTION	81h	TMR0	101h	OPTION
PCL	02h	PCL	82h	PCL	102h	PCL
STATUS	03h	STATUS	83h	STATUS	103h	STATUS
FSR	04h	FSR	84h	FSR	104h	FSR
PORTA	05h	TRISA	85h	MM.	105h	WILL
PORTB	06h	TRISB	86h	PORTB	106h	TRISB
PORTC	07h	TRISC	87h	- 1	107h	COM.
PORTD (1)	08h	TRISD (1)	88h	11/11/11	108h	Y. CONTIN
PORTE (1)	09h	TRISE (1)	89h	VV	109h	V.Cor
PCLATH	0Ah	PCLATH	8Ah	PCLATH	10Ah	PCLATH
INTCON	0Bh	INTCON	8Bh	INTCON	10Bh	INTCON
C PIR1	0Ch	PIE1	8Ch	W. V	10Ch	MY.CO
PIR2	0Dh	PIE2	8Dh	10	10Dh	COM
TMR1L	0Eh	PCON	8Eh	T.I.	10Eh	100 x 20M
TMR1H	0Fh	MAL	8Fh	TW	10Fh	1100X.
T1CON	10h	-11N N . 10	90h		110h	M. CO
TMR2	11h	W	91h	OWITH	111h	W.100 F CO
T2CON	12h	PR2	92h	WIL	112h	1007.0
SSPBUF	13h	SSPADD	93h	COM.	113h	MM. OUN.C.
SSPCON	14h	SSPSTAT	94h	COM.	114h	WW.100
CCPR1L	15h		95h	. M.TW	115h	N., 100 x.
CCPR1H	16h	N	96h	Y.COM TW	116h	WWW. 100X
CCP1CON	17h		97h	General	117h	General
RCSTA	18h	TXSTA	98h	Purpose Register	118h	Purpose Register
TXREG	19h	SPBRG N	99h	16 Bytes	119h	16 Bytes
RCREG	1Ah		9Ah	COM	11Ah	WWW.r
CCPR2L	1Bh	1	9Bh	Jon r. COW.	11Bh	L.WW.1
CCPR2H	1Ch	TW	9Ch	1100Y.	11Ch	N W
CCP2CON	1Dh	N. C.	9Dh	M. COM	11Dh	MMIN
VI 10	1Eh	OW:	9Eh	W.100 - CO	11Eh	TIVIV
MAN	1Fh	WI.IV	9Fh	1007.	11Fh	N T
WWW	20h	CONTRACT OF THE PARTY OF THE PA	A0h	V TOON CO	120h	1 MA
	Ing -	COM.	7.011	MAN. TOO C		VID VI
Al Al	11007	· TIM	N.	1001.		
General Purpose	100	General Purpose	4	General Purpose		General Purpose
Register	M.To.	Register		Register		Register
96 Bytes	TXN.10	80 Bytes		80 Bytes	$\sim 10^{M}$	80 Bytes
an pales	N 11	3000000	EFh	accesses	16Fh	accesses
	MM·7	accesses 70h-7Fh	F0h	70h-7Fh	170h	70h-7Fh
	7Fh	in Bank 0	FFh	in Bank 0	17Fh	in Bank 0

Unimplemented data memory locations, read as '0'.

Not a physical register.

These registers are not implemented on the PIC16C66.

Note: The upper 16 bytes of data memory in banks 1, 2, and 3 are mapped in Bank 0. This may require relocation of data memory usage in the user application code if upgrading to the PIC16C66/67.

4.2.2 SPECIAL FUNCTION REGISTERS:

The Special Function Registers are registers used by the CPU and peripheral modules for controlling the desired operation of the device. These registers are implemented as static RAM. The special function registers can be classified into two sets (core and peripheral). The registers associated with the "core" functions are described in this section and those related to the operation of the peripheral features are described in the section of that peripheral feature.

TABLE 4-1: SPECIAL FUNCTION REGISTERS FOR THE PIC16C61

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR	Value on all other resets ⁽³⁾
Bank 0	TV	N.	MM	ov.CC	M. TW		WWW	ann Y.	Com	TW	
00h ⁽¹⁾	INDF	Addressing	this location	uses conte	nts of FSR to	address data	a memory (n	ot a physica	l register)	0000 0000	0000 0000
01h	TMR0	Timer0 mod	dule's register	.00 -	COM	- 1	- 177	M.Inc	A COL	xxxx xxxx	uuuu uuuu
02h ⁽¹⁾	PCL	Program Co	ounter's (PC)	Least Sign	ificant Byte					0000 0000	0000 0000
03h ⁽¹⁾	STATUS	IRP ⁽⁴⁾	RP1 ⁽⁴⁾	RP0	TO	PD	z	DC	С	0001 1xxx	000q quuu
04h ⁽¹⁾	FSR	Indirect dat	a memory ad	dress point	ter	TW	V	1	007.	xxxx xxxx	uuuu uuuu
05h	PORTA	- W	4VV	44.5	PORTA Dat	a Latch whe	n written: PC	RTA pins wh	nen read	x xxxx	u uuuu
06h	PORTB	PORTB Da	ta Latch wher	n written: P	ORTB pins wl	nen read		MMM	You	xxxx xxxx	uuuu uuuu
07h	COM	Unimpleme	nted							$C_{G_{I_{I_{I_{I_{I_{I_{I_{I_{I_{I_{I_{I_{I_$	cVI—
08h	<u>-01</u>	Unimpleme	nted	WW	100 1	OW.	-31	-111	W.Inc	' CONT.	N N
09h	07.5	Unimpleme	nted		A.100 x.	COM.		44	NW.10	CON	<u> </u>
0Ah ^(1,2)	PCLATH	TY	_	M. J.	Counter	0 0000	0 0000				
0Bh ⁽¹⁾	INTCON	GIE	N _	RBIF	0-00 000x	0-00 000u					
Bank 1	· vol.	CO	TV	MA	1007.	MIN					
80h ⁽¹⁾	INDF	Addressing	this location	l register)	0000 0000	0000 0000					
81h	OPTION	RBPU	INTEDG	T0CS	TOSE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
82h ⁽¹⁾	PCL	Program Co	ounter's (PC)	Least Sign	ificant Byte	100 -	OM.	× N	TAT V	0000 0000	0000 0000
83h ⁽¹⁾	STATUS	IRP ⁽⁴⁾	RP1 ⁽⁴⁾	RP0	TO	PD	_ Z	DC	С	0001 1xxx	000q quuu
84h ⁽¹⁾	FSR	Indirect dat	a memory ad	dress point	ter	N.100 Y	Mos	In		xxxx xxxx	uuuu uuuu
85h	TRISA	ON LOS	π	N _	PORTA Dat	a Direction F	Register	LTW.		1 1111	1 1111
86h	TRISB	PORTB Da	ta Direction C	ontrol Reg	ister	100	M.Co.	WTI		1111 1111	1111 1111
87h	W.	Unimplemented								MAN.	100 1.C
88h	- Tank	Unimpleme	nted	TAN	<1	MW.I	OV.C	DIAT	N	WALL AND A	<u></u>
89h	7	Unimpleme	nted	U.I.		WW.	100	OM.	·XXI	TW W	1.100
8Ah ^(1,2)	PCLATH	VIV.10	07.0	$W.\overline{I}_{AA}$	Write Buffer	for the uppe	er 5 bits of th	e Program C	Counter	0 0000	0 0000
8Bh ⁽¹⁾	INTCON	GIE	007:00	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0-00 000x	0-00 000u

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented locations read as '0'. Shaded locations are unimplemented and read as '0'

Note 1: These registers can be addressed from either bank.

- 2: The upper byte of the Program Counter (PC) is not directly accessible. PCLATH is a holding register for the PC whose contents are transferred to the upper byte of the program counter. (PC<12:8>)
- 3: Other (non power-up) resets include external reset through MCLR and the Watchdog Timer Reset.
- 4: The IRP and RP1 bits are reserved on the PIC16C61, always maintain these bits clear.

TABLE 4-2: SPECIAL FUNCTION REGISTERS FOR THE PIC16C62/62A/R62

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets ⁽³⁾
Bank 0		VV T	N.100 x	COM.	1	1	WW.10	<1 CC	Mir	J	
00h ⁽¹⁾	INDF	Addressing	this location	uses conter	nts of FSR to	address data	a memory (n	ot a physica	register)	0000 0000	0000 0000
01h	TMR0	Timer0 mo	dule's registe	r	MIL		NA	100 x.	TMO	xxxx xxxx	uuuu uuuu
02h ⁽¹⁾	PCL	Program C	ounter's (PC)	Least Signit	ficant Byte		MM	11001		0000 0000	0000 0000
03h ⁽¹⁾	STATUS	IRP ⁽⁵⁾	RP1 ⁽⁵⁾	RP0	TO	PD	Z	DC	С	0001 1xxx	000q quuu
04h ⁽¹⁾	FSR	Indirect da	ta memory ac	ddress pointe	er	W	WW	M. in	V.CON	xxxx xxxx	uuuu uuuu
05h	PORTA	_	TO W	PORTA Dat	a Latch whe	n written: PO	RTA pins wh	en read	ov.CO	xx xxxx	uu uuuu
06h	PORTB	PORTB Da	ata Latch whe	n written: PC	ORTB pins w	hen read	44	WW.II	-1 CC	xxxx xxxx	uuuu uuuu
07h	PORTC	PORTC Da	ata Latch whe	n written: PC	ORTC pins w	hen read		-TXV.1	001.	xxxx xxxx	uuuu uuuu
08h	OF T	Unimpleme	ented	100	M.Co.	WILL	4	MAN	100 Y.C	77.77	_
09h	CG_{N_I}	Unimpleme	ented	MM	VA'CO	W		WWW	YOUY.	COF	W -
0Ah ^(1,2)	PCLATH	<u>-</u>	-	ounter	0 0000	0 0000					
0Bh ⁽¹⁾	INTCON	GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	(6)	(6)	<u> </u>	700x.	SSPIF	CCP1IF	TMR2IF	TMR1IF	00 0000	00 0000
0Dh	UO X-CO	Unimpleme	ented	MM	1100Y		LM	111	11 km	07.5	1.77
0Eh	TMR1L	Holding re	gister for the I	_east Signific	cant Byte of t	the 16-bit TM	R1 register	V	M M	xxxx xxxx	uuuu uuuu
0Fh	TMR1H	Holding re	gister for the I	Most Signific	ant Byte of the	ne 16-bit TMF	R1 register	4	NWW	xxxx xxxx	uuuu uuuu
10h	T1CON	COM!		T1CKPS1	T1CKPS0	T10SCEN	T1SYNC	TMR1CS	TMR10N	00 0000	uu uuuu
11h	TMR2	Timer2 mo	dule's registe	r	- XX 10	00 x .	MITW		-311	0000 0000	0000 0000
12h	T2CON	Y.Co.,	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	-000 0000
13h	SSPBUF	Synchrono	us Serial Por	t Receive Bu	ıffer/Transmit	Register	UH	W	WW	xxxx xxxx	uuuu uuuu
14h	SSPCON	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000	0000 0000
15h	CCPR1L	Capture/Co	ompare/PWM	1 (LSB)	VI CALL	N.100	COM	1		xxxx xxxx	uuuu uuuu
16h	CCPR1H	Capture/Co	ompare/PWM	1 (MSB)	MA	100		1.71	N.	xxxx xxxx	uuuu uuuu
17h	CCP1CON	ATTY!		CCP1X	CCP1Y	CCP1M3	CCP1M2	CCP1M1	CCP1M0	00 0000	00 0000
18h-1Fh	TVV	Unimpleme	ented	-CVV	N.	MM	VY.CO	TW		MAIN.	400 N.C

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented location read as '0'.

Shaded locations are unimplemented, read as '0'.

- Note 1: These registers can be addressed from either bank.
 - 2: The upper byte of the Program Counter (PC) is not directly accessible. PCLATH is a holding register for the PC whose contents are transferred to the upper byte of the program counter. (PC<12:8>)
 - 3: Other (non power-up) resets include external reset through MCLR and the Watchdog Timer reset.
 - 4: The BOR bit is reserved on the PIC16C62, always maintain this bit set.
 - 5: The IRP and RP1 bits are reserved on the PIC16C62/62A/R62, always maintain these bits clear.
 - 6: PIE1<7:6> and PIR1<7:6> are reserved on the PIC16C62/62A/R62, always maintain these bits clear.

TABLE 4-2: SPECIAL FUNCTION REGISTERS FOR THE PIC16C62/62A/R62 (Cont.'d)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets ⁽³⁾
Bank 1	4	- W.1	007	Mil	-1		N.100 .	COM	-31	-	
80h ⁽¹⁾	INDF	Addressing	this location	uses conte	ents of FSR to	address dat	a memory (r	ot a physica	l register)	0000 0000	0000 0000
81h	OPTION	RBPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
82h ⁽¹⁾	PCL	Program C	ounter's (PC)	Least Sig	nificant Byte	W	MAN	OY.Co	VIIV	0000 0000	0000 0000
83h ⁽¹⁾	STATUS	IRP ⁽⁵⁾	RP1 ⁽⁵⁾	RP0	TO	PD	Z	DC	С	0001 1xxx	000q quuu
84h ⁽¹⁾	FSR	Indirect da	ta memory ac	ldress poin	ter		NWW.	OOY.C	OM	xxxx xxxx	uuuu uuuu
85h	TRISA		W/4.10	PORTA Da	ata Direction F	Register	WW	In	$CO_{M_{I^{*}}}$	11 1111	11 1111
86h	TRISB	PORTB Da	ata Direction F	Register	OWITH	-7	1	N.100 x	COM	1111 1111	1111 1111
87h	TRISC	PORTC Da	ata Direction I	Register	TIM	N	M.	100		1111 1111	1111 1111
88h	WT	Unimpleme	ented	ANY.	COR	W	WW	100	N.Co	TTAN	_
89h	Wr-	Unimpleme	ented	VY.CO	WT	_					
8Ah ^(1,2)	PCLATH	<u> </u>	-	V.700.	Write Buffe	for the uppe	er 5 bits of th	e Program C	ounter	0 0000	0 0000
8Bh ⁽¹⁾	INTCON	GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000 000x	0000 000u
8Ch	PIE1	(6)	(6)	-xx110	07.7	SSPIE	CCP1IE	TMR2IE	TMR1IE	00 0000	00 0000
8Dh	CO	Unimpleme	ented	11	ON.Co	VIII	1	MM	1 100 X	-M.1	W -
8Eh	PCON	TV	- <	Man	Toot.C	- T	N —	POR	BOR ⁽⁴⁾	qq	uu
8Fh	√ C O	Unimpleme	ented	WWW	.Ju	OM	W	WW	111.2	V.COm	TY !
90h	03.	Unimpleme	ented	- TXXI Y	N.100	COM		-31	MM.In	~√€ON	N. T.
91h	00.7.0	Unimpleme	ented	111	W.100 Y	MOD	LA	77	-xW.1	-CO	W. F.
92h	PR2	Timer2 Per	riod Register	MA	100	Y.CO	TW	1	N N N	1111 1111	1111 1111
93h	SSPADD	Synchrono	us Serial Por	t (I ² C mode) Address Re	gister	WILL	4	MM	0000 0000	0000 0000
94h	SSPSTAT	CG_{M_I}	CV.	D/Ā	P	S	R/W	UA	BF	00 0000	00 0000
95h-9Fh	100°	Unimpleme	ented	4	L.VV.	00 -	UM	-4	-31	1.10	$CO\overline{M}_{I}$.

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented location read as '0'.

Shaded locations are unimplemented, read as '0'.

- Note 1: These registers can be addressed from either bank.
 - 2: The upper byte of the Program Counter (PC) is not directly accessible. PCLATH is a holding register for the PC whose contents are transferred to the upper byte of the program counter. (PC<12:8>)
 - 3: Other (non power-up) resets include external reset through MCLR and the Watchdog Timer reset.
 - 4: The $\overline{\text{BOR}}$ bit is reserved on the PIC16C62, always maintain this bit set.
 - 5: The IRP and RP1 bits are reserved on the PIC16C62/62A/R62, always maintain these bits clear.
 - 6: PIE1<7:6> and PIR1<7:6> are reserved on the PIC16C62/62A/R62, always maintain these bits clear.

TABLE 4-3: SPECIAL FUNCTION REGISTERS FOR THE PIC16C63/R63

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets ⁽³⁾
Bank 0	4	- 1V.1	do X	M.T.	-T	TANK	1.100	COM		'	
00h ⁽¹⁾	INDF	Addressing	this location	uses conte	nts of FSR to	address data	a memory (n	ot a physica	l register)	0000 0000	0000 0000
01h	TMR0	Timer0 mo	dule's registe	er		MAN	100	7.0	M.I.M	xxxx xxxx	uuuu uuuu
02h ⁽¹⁾	PCL	Program C	ounter's (PC)) Least Sign	ficant Byte	W	7110	OY.Co	WILL	0000 0000	0000 0000
03h ⁽¹⁾	STATUS	IRP ⁽⁴⁾	RP1 ⁽⁴⁾	RP0	TO	PD	z	DC	С	0001 1xxx	000q quuu
04h ⁽¹⁾	FSR	Indirect dat	ta memory a	ddress point	er		NWW	OOY.C	ON	xxxx xxxx	uuuu uuuu
05h	PORTA	_	V/1/10	PORTA Da	ta Latch whe	n written: PO	RTA pins wh	en read	COMP.	xx xxxx	uu uuuu
06h	PORTB	PORTB Da	ta Latch whe	en written: P	ORTB pins w	hen read	77	N.100	COM	xxxx xxxx	uuuu uuuu
07h	PORTC	PORTC Da	ata Latch whe	en written: P	ORTC pins w	hen read	MA	100		xxxx xxxx	uuuu uuuu
08h	WT	Unimpleme	ented	. cony.		W	MA	1100	M.Co.	TIN I	_
09h	Mr.	Unimpleme	ented	N. I.O.	COhr	TW	W	MAN	WY.CO	WT	_
0Ah ^(1,2)	PCLATH	«1 —	-	W.700.	Write Buffer	for the uppe	r 5 bits of the	e Program C	ounter	0 0000	0 0000
0Bh ⁽¹⁾	INTCON	GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	(5)	(5)	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
0Dh	PIR2	IM	-1/	-51 1	007	MIL	_		CCP2IF	0	0
0Eh	TMR1L	Holding reg	gister for the	Least Signifi	cant Byte of	the 16-bit TM	R1 register	MA	100	xxxx xxxx	uuuu uuuu
0Fh	TMR1H	Holding reg	gister for the	Most Signific	ant Byte of the	he 16-bit TMF	R1 register	WW	700	xxxx xxxx	uuuu uuuu
10h	T1CON	M-F	_	T1CKPS1	T1CKPS0	T10SCEN	T1SYNC	TMR1CS	TMR10N	00 0000	uu uuuu
11h	TMR2	Timer2 mo	dule's registe	er	W.100 .	COM	-31		TNW.Y	0000 0000	0000 0000
12h	T2CON	T.M	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	-000 0000
13h	SSPBUF	Synchrono	us Serial Por	t Receive B	uffer/Transmit	Register	MILIN	4	MAL	xxxx xxxx	uuuu uuuu
14h	SSPCON	WCOL	SSPOV	SSPEN	СКР	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000	0000 0000
15h	CCPR1L	Capture/Co	ompare/PWM	11 (LSB)	TWW.	as C	DIAI.	N	WW	xxxx xxxx	uuuu uuuu
16h	CCPR1H	Capture/Co	ompare/PWM	11 (MSB)		100 .	$O_{M,T}$		111	xxxx xxxx	uuuu uuuu
17h	CCP1CON	115	W.IN	CCP1X	CCP1Y	CCP1M3	CCP1M2	CCP1M1	CCP1M0	00 0000	00 0000
18h 🔨	RCSTA	SPEN	RX9	SREN	CREN	1107	FERR	OERR	RX9D	0000 -00x	0000 -00x
19h	TXREG	USART Tra	nsmit Data F	Register	WW	100	Y.Co.	WIN	V	0000 0000	0000 0000
1Ah	RCREG	USART Re	ceive Data R	Register	VV	M.To	V.COP	WT		0000 0000	0000 0000
1Bh	CCPR2L	Capture/Co	ompare/PWM	12 (LSB)		MM Ja	N CO	M		xxxx xxxx	uuuu uuuu
1Ch	CCPR2H	Capture/Co	ompare/PWM	12 (MSB)		WW.I	90 1	OWIT	<u> </u>	xxxx xxxx	uuuu uuuu
1Dh	CCP2CON	-XI-100	O	CCP2X	CCP2Y	CCP2M3	CCP2M2	CCP2M1	CCP2M0	00 0000	00 0000
1Eh-1Fh	70/7	Unimpleme	ented	WIIN		N. V.	7007.	COM.		-	W 700;
l edend:		4111.2	nchanged o		Ú			Description of the		101	10

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented location read as '0'. Shaded locations are unimplemented, read as '0'.

- Note 1: These registers can be addressed from either bank.
 - 2: The upper byte of the Program Counter (PC) is not directly accessible. PCLATH is a holding register for the PC whose contents are transferred to the upper byte of the program counter. (PC<12:8>)
 - 3: Other (non power-up) resets include external reset through MCLR and the Watchdog Timer reset.
 - 4: The IRP and RP1 bits are reserved on the PIC16C63/R63, always maintain these bits clear.
 - 5: PIE1<7:6> and PIR1<7:6> are reserved on the PIC16C63/R63, always maintain these bits clear.

TABLE 4-3: SPECIAL FUNCTION REGISTERS FOR THE PIC16C63/R63 (Cont.'d)

									-	•		
Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets ⁽³⁾	
Bank 1	A	- TXV.1	uv -	MIL		N T	N.100	COM	-11			
80h ⁽¹⁾	INDF	Addressing	this location	uses conte	ents of FSR to	address dat	ta memory (r	ot a physica	l register)	0000 0000	0000 0000	
81h	OPTION	RBPU	INTEDG	TOCS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111	
82h ⁽¹⁾	PCL	Program C	ounter's (PC)) Least Siç	gnificant Byte	W	W 44.	10 Y.Co	VIIV	0000 0000	0000 0000	
83h ⁽¹⁾	STATUS	IRP ⁽⁴⁾	RP1 ⁽⁴⁾	RP0	TO	PD	Z	DC	С	0001 1xxx	000q quuu	
84h ⁽¹⁾	FSR	Indirect dat	ta memory a	ddress poin	ter		WW.	OV.C	OM	xxxx xxxx	uuuu uuuu	
85h	TRISA		VIV-10	PORTA Da	ata Direction F	Register	TAN V	100 1	$CO_{M_{1}}$	11 1111	11 1111	
86h	TRISB	PORTB Da	ata Direction	Register	OMITH		11	N.100 X	MOD	1111 1111	1111 1111	
87h	TRISC	PORTC Da	ata Direction	Register	TIME	N	MAN	100	-01	1111 1111	1111 1111	
88h	WT	Unimpleme	ented	TOUX:	Con	W	WW	1100	M.Co.	TT	_	
89h	W	Unimpleme	ented	1.10	COMP.	TW	W	MM	NY.CO	WT.	_	
8Ah ^(1,2)	PCLATH	<u> </u>		N.100	Write Buffer	for the uppe	er 5 bits of th	e Program C	ounter	0 0000	0 0000	
8Bh ⁽¹⁾	INTCON	GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000 000x	0000 000u	
8Ch	PIE1	(5)	(5)	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000	
8Dh	PIE2	TIL	-1/1	=11	007	W.T.V	_	1/1	CCP2IE	0	0	
8Eh	PCON	(T Y)	- <	11/7	100¥.C	- \ - T	N _	POR	BOR	qq	uu	
8Fh	~√.€O	Unimpleme	ented	WWW	. NOV.	ON	W	WV	100	N.Co.	TH	
90h	27 CC	Unimpleme	ented	-XIXIV	N.Ing	COM	-CVV	VN"	MMira	N.€OD	- 17N	
91h	00 =	Unimpleme	ented	1	W.100 x	COM	. 1		WW.T	- 7 CO	Nr	
92h	PR2	Timer2 Per	riod Register	W.	100	1.0	LTW			1111 1111	1111 1111	
93h	SSPADD	Synchrono	us Serial Por	t (I ² C mode	e) Address Re	gister				0000 0000	0000 0000	
94h	SSPSTAT	$CO_{M_{p}}$	TV I	D/Ā	Р	S	R/W	UA	BF	00 0000	00 0000	
95h	11.700	Unimpleme	ented		WW.I	NZ.C	OMr.	N	WW	N. E	COA	
96h	101.±00	Unimpleme	ented		W.	100 -	-OM.1			41.700	CGM.	
97h	T 10	Unimpleme	ented		N V	1700 x	COM	. N.		WH100	COM	
98h ⁽²⁾	TXSTA	CSRC	TX9	TXEN	SYNC	100X	BRGH	TRMT	TX9D	0000 -010	0000 -010	
99h ⁽²⁾	SPBRG	Baud Rate	Generator R	egister	MM	100	A.Co.	WIL		0000 0000	0000 0000	
9Ah	N W	Unimpleme	ented	rsN	WV	1111-7	M.COr	W		MATA	T.C.	
9Bh	- ANY	Unimplemented								WAN.	N.C	
9Ch	M.	Unimpleme	ented	<u> </u>	TANY	100						
9Dh	AN	Unimpleme	implemented									
9Eh	307	Unimpleme	ented	WT		MANA	100Y.	7		4111	TOOY	
9Fh		Unimpleme	ented	Mr.	N	WWW	Vie		TW	-11	700	

 $\label{eq:location} \textbf{Legend:} \quad \textbf{x} = \textbf{unknown}, \ \textbf{u} = \textbf{unchanged}, \ \textbf{q} = \textbf{value} \ \textbf{depends} \ \textbf{on condition}, \ \textbf{-} = \textbf{unimplemented location read as '0'}.$

Shaded locations are unimplemented, read as '0'.

- Note 1: These registers can be addressed from either bank.
 - 2: The upper byte of the Program Counter (PC) is not directly accessible. PCLATH is a holding register for the PC whose contents are transferred to the upper byte of the program counter. (PC<12:8>)
 - 3: Other (non power-up) resets include external reset through MCLR and the Watchdog Timer reset.
 - 4: The IRP and RP1 bits are reserved on the PIC16C63/R63, always maintain these bits clear.
 - 5: PIE1<7:6> and PIR1<7:6> are reserved on the PIC16C63/R63, always maintain these bits clear.

TABLE 4-4: SPECIAL FUNCTION REGISTERS FOR THE PIC16C64/64A/R64

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets ⁽³⁾
Bank 0		W	N.100 x	COM	1	-1	M.10	<1 CC	M	J	
00h ⁽¹⁾	INDF	Addressing	this location	uses conter	nts of FSR to	address data	a memory (n	ot a physica	l register)	0000 0000	0000 0000
01h	TMR0	Timer0 mo	dule's registe	r	MIL		NA	100 X.	TMOT	xxxx xxxx	uuuu uuuu
02h ⁽¹⁾	PCL	Program C	ounter's (PC)	Least Signi	ficant Byte		MM	1100Y		0000 0000	0000 0000
03h ⁽¹⁾	STATUS	IRP ⁽⁵⁾	RP1 ⁽⁵⁾	RP0	TO	PD	Z	DC	С	0001 1xxx	000q quuu
04h(1)	FSR	Indirect da	ta memory ac	dress pointe	er	11	WW	M. in	V.COM	xxxx xxxx	uuuu uuuu
05h	PORTA	_	- WW	PORTA Dat	a Latch whe	n written: PO	RTA pins wh	en read	ON CO	xx xxxx	uu uuuu
06h	PORTB	PORTB Da	ata Latch whe	n written: PC	ORTB pins w	hen read	14	11.W.X	7 CC	xxxx xxxx	uuuu uuuu
07h	PORTC	PORTC Da	ata Latch whe	n written: PO	ORTC pins w	hen read		-TXN.1	001.	xxxx xxxx	uuuu uuuu
08h	PORTD	PORTD Da	ata Latch whe	n written: PO	ORTD pins w	hen read	1	MAN	100 Y.C	xxxx xxxx	uuuu uuuu
09h	PORTE	rV I	-01	N.A.	W.Co.	WE	RE2	RE1	RE0	xxx	uuu
0Ah ^(1,2)	PCLATH	- TN	- 3	1171.7	Write Buffer	for the uppe	r 5 bits of the	e Program C	ounter	0 0000	0 0000
0Bh ⁽¹⁾	INTCON	GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	PSPIF	(6)	VV	100,	SSPIF	CCP1IF	TMR2IF	TMR1IF	00 0000	00 0000
0Dh	00.7	Unimpleme	ented	11	N.100 X	COM.	1		MW.M	-TO	W
0Eh	TMR1L	Holding reg	gister for the I	_east Signific	cant Byte of t	he 16-bit TM	R1 register		- TAN .	xxxx xxxx	uuuu uuuu
0Fh	TMR1H	Holding reg	gister for the I	Most Signific	ant Byte of th	ne 16-bit TMF	R1 register	4	MM	xxxx xxxx	uuuu uuuu
10h	T1CON	$CG_{Z_{I_{I}}}$	CVI	T1CKPS1	T1CKPS0	T10SCEN	T1SYNC	TMR1CS	TMR10N	00 0000	uu uuuu
11h	TMR2	Timer2 mo	dule's registe	r	TWW.I	of CC	Mr	KJ	WIN	0000 0000	0000 0000
12h	T2CON		TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	-000 0000
13h	SSPBUF	Synchrono	us Serial Por	t Receive Bu	ıffer/Transmit	Register	.oM.T		111	xxxx xxxx	uuuu uuuu
14h	SSPCON	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000	0000 0000
15h	CCPR1L	Capture/Co	ompare/PWM	1 (LSB)	TIM	N. I.	COM.		11	xxxx xxxx	uuuu uuuu
16h	CCPR1H	Capture/Co	ompare/PWM	1 (MSB)	TXX	W.100	CON	1.1		xxxx xxxx	uuuu uuuu
17h	CCP1CON	100,	<u>-1.1</u>	CCP1X	CCP1Y	CCP1M3	CCP1M2	CCP1M1	CCP1M0	00 0000	00 0000
18h-1Fh	MAN	Unimpleme	ented	TW	W	1110	OY.Co	WILLE		11 7	1000

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented location read as '0'. Shaded locations are unimplemented, read as '0'.

- Note 1: These registers can be addressed from either bank.
 - 2: The upper byte of the Program Counter (PC) is not directly accessible. PCLATH is a holding register for the PC whose WWW.100Y.COM.T contents are transferred to the upper byte of the program counter. (PC<12:8>)
 - Other (non power-up) resets include external reset through MCLR and the Watchdog Timer reset.
 - The BOR bit is reserved on the PIC16C64, always maintain this bit set.
 - The IRP and RP1 bits are reserved on the PIC16C64/64A/R64, always maintain these bits clear.
 - PIE1<6> and PIR1<6> are reserved on the PIC16C64/64A/R64, always maintain these bits clear.

TABLE 4-4: SPECIAL FUNCTION REGISTERS FOR THE PIC16C64/64A/R64 (Cont.'d)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets ⁽³⁾
Bank 1	A	TW.1	003	M.I.			N.100	COM	- 1	•	
80h ⁽¹⁾	INDF	Addressing	g this location	uses conte	ents of FSR to a	address da	ta memory (n	ot a physica	l register)	0000 0000	0000 0000
81h	OPTION	RBPU	INTEDG	TOCS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
82h ⁽¹⁾	PCL	Program C	ounter's (PC) Least Sig	gnificant Byte	W	111	10Y.Co	VIIV	0000 0000	0000 0000
83h ⁽¹⁾	STATUS	IRP ⁽⁵⁾	RP1 ⁽⁵⁾	RP0	TO	PD	Z	DC	С	0001 1xxx	000q quuu
84h ⁽¹⁾	FSR	Indirect da	ta memory a	ddress poin	ter		NWW.	OOY.C	OM	xxxx xxxx	uuuu uuuu
85h	TRISA		W/4.10	PORTA Da	ata Direction Re	egister	WW	In	$CO_{M_{I^{*}}}$	11 1111	11 1111
86h	TRISB	PORTB Da	ata Direction	Register	OWITH	7		N.100	COM	1111 1111	1111 1111
87h	TRISC	PORTC Da	ata Direction	Register	MIN		11111	WI 100	100	1111 1111	1111 1111
88h	TRISD	PORTD Da	ata Direction	Register	COTT	W	N.Co	1111 1111	1111 1111		
89h	TRISE	IBF	OBF	IBOV	PSPMODE	rvi-	PORTE Da	ta Direction	Bits	0000 -111	0000 -111
8Ah ^(1,2)	PCLATH	- N	N To	11.700	Write Buffer f	for the upp	er 5 bits of the	e Program C	ounter	0 0000	0 0000
8Bh ⁽¹⁾	INTCON	GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000 000x	0000 000u
8Ch	PIE1	PSPIE	(6)	W.14.10	7.0	SSPIE	CCP1IE	TMR2IE	TMR1IE	00 0000	00 0000
8Dh	- <u>-</u> M	Unimpleme	ented	- TXN .1	1003.	MIL	-7	77	N.100,	CGM.	
8Eh	PCON	TIN	- 1	111	1007.	ON+T	_	POR	BOR ⁽⁴⁾	qq	uu
8Fh	W.Co.	Unimpleme	ented	MAN	1100 Y.C	- N 1	IN	MA	10	7	TY
90h	~-CC	Unimpleme	ented	WW	N. M.	$CO_{M_{\bullet}}$	TW	W	M. A.	ON CO.	PETT
91h	00 = C	Unimpleme	ented	- 11/	W.Inc	$^{\circ}CO_{D_{i}}$. TAN	*1	MAN	CO	WE
92h	PR2	Timer2 Per	riod Register	N.	M.100,	COL	TINN.	1111 1111	1111 1111		
93h	SSPADD	Synchrono	ous Serial Por	t (I ² C mode	e) Address Reg	ister	11	0000 0000	0000 0000		
94h	SSPSTAT	CO	TIL	D/Ā	Р	S	R/W	UA	BF	00 0000	00 0000
95h-9Fh	41.5	Unimpleme	ented		MM	ON.C	On.	N	WW	Your	U 1

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented location read as '0'. Shaded locations are unimplemented, read as '0'.

- Note 1: These registers can be addressed from either bank.
 - 2: The upper byte of the Program Counter (PC) is not directly accessible. PCLATH is a holding register for the PC whose contents are transferred to the upper byte of the program counter. (PC<12:8>)
 - 3: Other (non power-up) resets include external reset through MCLR and the Watchdog Timer reset.
 - 4: The BOR bit is reserved on the PIC16C64, always maintain this bit set.
 - 5: The IRP and RP1 bits are reserved on the PIC16C64/64A/R64, always maintain these bits clear.
 - 6: PIE1<6> and PIR1<6> are reserved on the PIC16C64/64A/R64, always maintain these bits clear.

TABLE 4-5: SPECIAL FUNCTION REGISTERS FOR THE PIC16C65/65A/R65

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets ⁽³⁾
_1		N.100.	COM		- 1	WW.I	ow CC	Mr.	V	
INDF	Addressing	this location	n uses conte	nts of FSR to	address data	a memory (n	ot a physica	register)	0000 0000	0000 0000
TMR0	Timer0 mod	dule's registe	er	MIIM		N	1007.	T.MO	xxxx xxxx	uuuu uuuu
PCL	Program C	ounter's (PC) Least Sign	ificant Byte		MM	1100X	Mo	0000 0000	0000 0000
STATUS	IRP ⁽⁵⁾	RP1 ⁽⁵⁾	RP0	TO	PD	z	DC	С	0001 1xxx	000q quuu
FSR	Indirect dat	a memory a	ddress point	er	W	WW	44.	Y.CO	xxxx xxxx	uuuu uuuu
PORTA	_		PORTA Da	ta Latch whe	n written: PO	RTA pins wh	en read	V.CO	xx xxxx	uu uuuu
PORTB	PORTB Da	ta Latch whe	en written: P	ORTB pins w	hen read		WW.I	*1 CC	xxxx xxxx	uuuu uuuu
PORTC	PORTC Da	ita Latch who	en written: P	ORTC pins w	hen read	The state of the s	TIN.	003.	xxxx xxxx	uuuu uuuu
PORTD	PORTD Da	ita Latch who	en written: P	ORTD pins w	hen read		NA	100 X.C	xxxx xxxx	uuuu uuuu
PORTE	TVI	-W	W	WI CO	WFIL	RE2	RE1	RE0	xxx	uuu
PCLATH	~~~\	- <	M.	Write Buffer	r for the uppe	r 5 bits of the	e Program C	ounter	0 0000	0 0000
INTCON	GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000 000x	0000 000u
PIR1	PSPIF	(6)	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
PIR2	MIL			N.100	COM.	-	_	CCP2IF	0	0
TMR1L	Holding reg	jister for the	Least Signifi	icant Byte of	the 16-bit TM	R1 register			xxxx xxxx	uuuu uuuu
TMR1H	Holding reg	gister for the	Most Signific	cant Byte of the	he 16-bit TMI	R1 register		N N	xxxx xxxx	uuuu uuuu
T1CON	CO_{N}	TV +	T1CKPS1	T1CKPS0	T10SCEN	T1SYNC	TMR1CS	TMR10N	00 0000	uu uuuu
TMR2	Timer2 mo	dule's registe	er	MM	ov.C)W.	N	WW	0000 0000	0000 0000
T2CON	01	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	-000 0000
SSPBUF	Synchrono	us Serial Po	rt Receive B	uffer/Transmit	t Register	COM		- 1	xxxx xxxx	uuuu uuuu
SSPCON	WCOL	SSPOV	SSPEN	СКР	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000	0000 0000
CCPR1L	Capture/Co	mpare/PWN	//1 (LSB)	WW	1007	I.Co.	WT	V	xxxx xxxx	uuuu uuuu
CCPR1H	Capture/Co	mpare/PWN	И1 (MSB)	WV	M.r.	A'CON	TW	4	xxxx xxxx	uuuu uuuu
CCP1CON	700	COM.	CCP1X	CCP1Y	CCP1M3	CCP1M2	CCP1M1	CCP1M0	00 0000	00 0000
RCSTA	SPEN	RX9	SREN	CREN	W.10	FERR	OERR	RX9D	0000 -00x	0000 -00x
TXREG	USART Tra	nsmit Data F	Register	V	-111	1001	TIMO	N	0000 0000	0000 0000
RCREG	USART Re	ceive Data F	Register	4	MW	1007.	-OM.T		0000 0000	0000 0000
CCPR2L	Capture/Co	mpare/PWN	//2 (LSB)		MMA	TOOY	Con	TW	xxxx xxxx	uuuu uuuu
CCPR2H	Capture/Co	ompare/PWN	//2 (MSB)	W	WW	N. P	Y.COM	WT	xxxx xxxx	uuuu uuuu
CCP2CON	or N	100 F	CCP2X	CCP2Y	CCP2M3	CCP2M2	CCP2M1	CCP2M0	00 0000	00 0000
_	Unimpleme	ented	COM			WW.10	SI CO	M.	_	NIVIN.
	TMR0 PCL STATUS FSR PORTA PORTB PORTC PORTD PORTE PCLATH INTCON PIR1 PIR2 TMR1L TMR1H T1CON SSPBUF SSPCON CCPR1L CCPR1H CCP1CON RCSTA TXREG RCREG CCPR2L	INDF Addressing TMR0 Timer0 mo PCL Program C STATUS IRP(5) FSR Indirect dat PORTA — PORTB PORTB Da PORTC PORTC Da PORTD PORTD Da PORTE — PCLATH — INTCON GIE PIR1 PSPIF PIR2 — TMR1L Holding reg TMR1H Holding reg TMR2 Timer2 mo T2CON — SSPBUF Synchrono SSPCON WCOL CCPR1L Capture/Cc CCPR1L Capture/Cc CCP1CON — RCSTA SPEN TXREG USART Tra RCREG USART Re CCPR2L Capture/Cc CCPR2H Capture/Cc CCPR2CON —	INDF Addressing this location TMR0 Timer0 module's registre PCL Program Counter's (PC) STATUS IRP(5) RP1(5) FSR Indirect data memory a PORTA — — PORTB PORTB Data Latch who PORTC PORTC Data Latch who PORTD PORTD Data Latch who PORTE — — PCLATH — — INTCON GIE PEIE PIR1 PSPIF (6) PIR2 — — TMR1L Holding register for the T1CON — — TMR2 Timer2 module's registre T2CON — TOUTPS3 SSPBUF Synchronous Serial Po SSPCON WCOL SSPOV CCPR1L Capture/Compare/PWN CCP1CON — — RCSTA SPEN RX9 TXREG USART Transmit Data I RCREG USART Receive Data F CCPR2L Capture/Compare/PWN CCPR2H Capture/Compare/PWN CCCPR2H Capture/Compare/PWN CCPR2H Capture/Compare/PWN	INDF Addressing this location uses content of the test of the Least Signification and the Least Signif	INDF Addressing this location uses contents of FSR to TMR0 Timer0 module's register PCL Program Counter's (PC) Least Significant Byte STATUS IRP(5) RP1(5) RP0 TO FSR Indirect data memory address pointer PORTA — PORTA Data Latch when PORTB PORTB PORTB Data Latch when written: PORTB pins when PORTD PORTC Data Latch when written: PORTC pins when PORTD PORTD Data Latch when written: PORTD pins when PORTD PORTD Data Latch when written: PORTD pins when PORTD PORTD Data Latch when written: PORTD pins when PORTD PORTD Data Latch when written: PORTD pins when PORTD PORTD Data Latch when written: PORTD pins when PORTD PORTD Data Latch when written: PORTD pins when PORTD PORTD Data Latch when written: PORTD pins when PORTD P	INDF Addressing this location uses contents of FSR to address dated TMR0 Timer0 module's register PCL Program Counter's (PC) Least Significant Byte STATUS IRP(5) RP1(5) RP0 TO PD FSR Indirect data memory address pointer PORTA — PORTA Data Latch when written: PORTB pins when read PORTC PORTB Data Latch when written: PORTB pins when read PORTC PORTD Data Latch when written: PORTD pins when read PORTD PORTD Data Latch when written: PORTD pins when read PORTD PORTD Data Latch when written: PORTD pins when read PORTE — — — — — — — — — — — — — — — — — — —	INDF Addressing this location uses contents of FSR to address data memory (notes) Timero module's register PCL Program Counter's (PC) Least Significant Byte STATUS IRP(5) RP1(5) RP0 TO PD Z FSR Indirect data memory address pointer PORTA — PORTA Data Latch when written: PORTA pins when PORTB PORTB Data Latch when written: PORTB pins when read PORTD PORTD Data Latch when written: PORTC pins when read PORTD PORTD Data Latch when written: PORTD pins when read PORTD PORTD Data Latch when written: PORTD pins when read PORTE — — — RE2 PCLATH — Write Buffer for the upper 5 bits of the INTCON GIE PEIE TOIE INTE RBIE TOIF PIR1 PSPIF (6) RCIF TXIF SSPIF CCP1IF PIR2 — — — — — — — — — — — — — — — — — — —	INDF Addressing this location uses contents of FSR to address data memory (not a physica TMR0 Timer0 module's register PCL Program Counter's (PC) Least Significant Byte STATUS IRP(5) RP1(5) RP0 TO PD Z DC FSR Indirect data memory address pointer PORTA — PORTA Data Latch when written: PORTA pins when read PORTB PORTB Data Latch when written: PORTB pins when read PORTC PORTC Data Latch when written: PORTC pins when read PORTD PORTD Data Latch when written: PORTD pins when read PORTD PORTD Data Latch when written: PORTD pins when read PORTE — — — Write Buffer for the upper 5 bits of the Program C INTCON GIE PEIE TOIE INTE RBIE TOIF INTF INTF INTF INTF INTF INTF INTF IN	INDF Addressing this location uses contents of FSR to address data memory (not a physical register) TMR0 Timer0 module's register PCL Program Counter's (PC) Least Significant Byte STATUS IRP(9) RP19 RP0 TO PD Z DC C FSR Indirect data memory address pointer PORTA — PORTA Data Latch when written: PORTA pins when read PORTB PORTB Data Latch when written: PORTB pins when read PORTD PORTD PORTD Data Latch when written: PORTD pins when read PORTD PORTD PORTD Data Latch when written: PORTD pins when read PORTD PORTD Data Latch when written: PORTD pins when read PORTD PORTD Data Latch when written: PORTD pins when read PORTD PORTD PORTD Data Latch when written: PORTD pins when read PORTD PORTD PORTD Data Latch when written: PORTD pins when read PORTD PORTD PORTD DATA LATCH WRITTEN PORTD PINS WHEN PROWN PROWN PORTD PINS WHEN PROWN	Name

 $\label{eq:condition} \textbf{Legend:} \quad \textbf{x} = \textbf{unknown}, \ \textbf{u} = \textbf{unchanged}, \ \textbf{q} = \textbf{value} \ \textbf{depends} \ \textbf{on condition}, \ \textbf{-} = \textbf{unimplemented location read as '0'}.$

Shaded locations are unimplemented, read as '0'.

- Note 1: These registers can be addressed from either bank.
 - 2: The upper byte of the Program Counter (PC) is not directly accessible. PCLATH is a holding register for the PC whose contents are transferred to the upper byte of the program counter. (PC<12:8>)
 - 3: Other (non power-up) resets include external reset through MCLR and the Watchdog Timer reset.
 - 4: The BOR bit is reserved on the PIC16C65, always maintain this bit set.
 - 5: The IRP and RP1 bits are reserved on the PIC16C65/65A/R65, always maintain these bits clear.
 - 6: PIE1<6> and PIR1<6> are reserved on the PIC16C65/65A/R65, always maintain these bits clear.

TABLE 4-5: SPECIAL FUNCTION REGISTERS FOR THE PIC16C65/65A/R65 (Cont.'d)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets ⁽³⁾
Bank 1	4	- 1V.1	007	MI	-1		N.100 x	COM			
80h ⁽¹⁾	INDF	Addressing	this location	uses conte	ents of FSR to a	address da	ta memory (r	ot a physica	l register)	0000 0000	0000 0000
81h	OPTION	RBPU	INTEDG	TOCS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
82h ⁽¹⁾	PCL	Program C	ounter's (PC)) Least Sig	gnificant Byte	W	1111	OY.Co	TIV	0000 0000	0000 0000
83h ⁽¹⁾	STATUS	IRP ⁽⁵⁾	RP1 ⁽⁵⁾	RP0	₹Ō	PD	Z	DC	С	0001 1xxx	000q quuu
84h ⁽¹⁾	FSR	Indirect dat	a memory a	ddress poin	ter		WW.	ON C	ON	xxxx xxxx	uuuu uuuu
85h	TRISA		XX 1 .10	PORTA Da	ata Direction R	egister	VIVI	100	COMP.	11 1111	11 1111
86h	TRISB	PORTB Da	ta Direction	Register	OWITH		N V	N.100 x	COM	1111 1111	1111 1111
87h	TRISC	PORTC Da	ta Direction	Register	MIN		MAG	100°		1111 1111	1111 1111
88h	TRISD	PORTD Da	ta Direction	Register	COPT	W	MM	100	JY.Co	1111 1111	1111 1111
89h	TRISE	IBF	OBF	IBOV	PSPMODE	rvi-	PORTE Da	ta Direction	Bits	0000 -111	0000 -111
8Ah ^(1,2)	PCLATH	N -	-WW	N.700	Write Buffer	for the upp	er 5 bits of th	e Program C	ounter	0 0000	0 0000
8Bh ⁽¹⁾	INTCON	GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000 000x	0000 000u
8Ch	PIE1	PSPIE	(6)	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
8Dh	PIE2	T.	- 4	- 1 1 1 1	1003	WILL	_		CCP2IE		0
8Eh	PCON	TY	_ 1		1007.	ONA.T	_	POR	BOR ⁽⁴⁾	qq	uu
8Fh	W.Co.	Unimpleme	ented	MANA	1100 Y.C		T.M.	MA	10	77	(III)
90h	CC C	Unimpleme	ented	WW	N. P	$C_{O_{2k,1}}$	TW	W	W. Aur	ON CO.	TEN
91h	- <u>₹</u> 1 C	Unimpleme	ented	TATE OF	W. In	$^{\prime}CO_{D_{2}}$	TV	1	MM	ONT.CO	WE
92h	PR2	Timer2 Per	iod Register	N. C.	M.100,		Vir		TWW.	1111 1111	1111 1111
93h	SSPADD	Synchrono	us Serial Por	t (I ² C mode	e) Address Reg	ister				0000 0000	0000 0000
94h	SSPSTAT	CO	TIV	D/Ā	Р	S	R/W	UA	BF	00 0000	00 0000
95h	$M \cdot \overline{\overline{z}}$	Unimpleme	ented		MM	ONY.C	" 1 T	N	MM	T 107	<u> </u>
96h	MITO	Unimpleme	ented		WW.		COMP	W	WV	111.5	COn
97h	10 N	Unimpleme	ented	1	TANK	100	COM	<u> </u>		MATIO	A COM
98h	TXSTA	CSRC	TX9	TXEN	SYNC	$^{N.7}\overline{\sigma}_{0.2}$	BRGH	TRMT	TX9D	0000 -010	0000 -010
99h	SPBRG	Baud Rate	Generator R	egister						0000 0000	0000 0000
9Ah	MAIN	Unimpleme	ented		WW	10	OXICO	MIN		<u> </u>	100 T.
9Bh	WALLEY OF	Unimpleme	ented	TW	W	MAN	ONY.CO	WT		M. Tallan	1005Y.C
9Ch		Unimpleme	ented	- XXI	N	WWW	- - 0 V.				
9Dh	W.	Unimpleme	ented	V.J.	- 51	=	N.100				
9Eh	411	Unimpleme	ented	MILM		N	1.100 X.	OM	LAA	7	W. HOU?
9Fh	- 41	Unimpleme	ented		N	MM	1007	.00	TW	-1/1/	100

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented location read as '0'. Shaded locations are unimplemented, read as '0'.

- Note 1: These registers can be addressed from either bank.
 - The upper byte of the Program Counter (PC) is not directly accessible. PCLATH is a holding register for the PC whose WWW.100Y.COM contents are transferred to the upper byte of the program counter. (PC<12:8>)
 - 3: Other (non power-up) resets include external reset through MCLR and the Watchdog Timer reset.
 - 4: The BOR bit is reserved on the PIC16C65, always maintain this bit set.
 - 5: The IRP and RP1 bits are reserved on the PIC16C65/65A/R65, always maintain these bits clear.
 - 6: PIE1<6> and PIR1<6> are reserved on the PIC16C65/65A/R65, always maintain these bits clear.

TABLE 4-6: SPECIAL FUNCTION REGISTERS FOR THE PIC16C66/67

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets ⁽³⁾
Bank 0	- 7	NA TATA	N. 100.	COM	1	- 1	MN.In	T CC	Mir	J	•
00h ⁽¹⁾	INDF	Addressing	this location	uses conte	nts of FSR to	address data	a memory (n	ot a physical	l register)	0000 0000	0000 0000
01h	TMR0	Timer0 mod	dule's registe	er	MIW		NAV	100 A.	T.MOD	xxxx xxxx	uuuu uuuu
02h ⁽¹⁾	PCL	Program Co	ounter's (PC) Least Sign	ificant Byte		MM	1100Y.		0000 0000	0000 0000
03h ⁽¹⁾	STATUS	IRP	RP1	RP0	TO	PD	Z	DC	С	0001 1xxx	000q quuu
04h(1)	FSR	Indirect data	a memory a	ddress point	er	W	WW	11:30	V.COM	xxxx xxxx	uuuu uuuu
05h	PORTA	_		PORTA Da	ta Latch whe	n written: PO	RTA pins wh	en read	N CO	xx xxxx	uu uuuu
06h	PORTB	PORTB Dat	ta Latch whe	en written: Po	ORTB pins w	hen read		MW.10	, C	xxxx xxxx	uuuu uuuu
07h	PORTC	PORTC Dat	ta Latch whe	en written: P	ORTC pins w	hen read	V	-TXXI.3	001.	xxxx xxxx	uuuu uuuu
08h ⁽⁵⁾	PORTD	PORTD Dat	ta Latch whe	en written: P	ORTD pins w	hen read	4	MM	100 Y.C	xxxx xxxx	uuuu uuuu
09h ⁽⁵⁾	PORTE	~V+	-01	N.J.	W-CO	WE	RE2	RE1	RE0	xxx	4uuu
0Ah ^(1,2)	PCLATH			MAN	Write Buffer	for the uppe	r 5 bits of the	e Program C	ounter	0 0000	0 0000
0Bh ⁽¹⁾	INTCON	GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	PSPIF ⁽⁶⁾	(4)	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
0Dh	PIR2	MITTY	_		N.100 ×	COM.	<u>=</u>	_	CCP2IF	0	0
0Eh	TMR1L	Holding reg	ister for the	Least Signifi	icant Byte of	the 16-bit TM	R1 register		- XIVI.1	xxxx xxxx	uuuu uuuu
0Fh	TMR1H	Holding reg	ister for the	Most Signific	cant Byte of the	he 16-bit TMF	R1 register		MAA	xxxx xxxx	uuuu uuuu
10h	T1CON	$CO_{D_{2}}$	rV I	T1CKPS1	T1CKPS0	T10SCEN	T1SYNC	TMR1CS	TMR10N	00 0000	uu uuuu
11h	TMR2	Timer2 mod	dule's registe	er	MW.L	ov.CC)Mr.	V	WW	0000 0000	0000 0000
12h	T2CON	- 01	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	-000 0000
13h	SSPBUF	Synchronou	ıs Serial Por	t Receive B	uffer/Transmit	Register	T.Mor	77	- 14	xxxx xxxx	uuuu uuuu
14h 🔨	SSPCON	WCOL	SSPOV	SSPEN	СКР	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000	0000 0000
15h	CCPR1L	Capture/Co	mpare/PWN	11 (LSB)	WW	W	CO P	WT	V	xxxx xxxx	uuuu uuuu
16h	CCPR1H	Capture/Co	mpare/PWN	11 (MSB)		M. Inc	A CON	T. T.	4	xxxx xxxx	uuuu uuuu
17h	CCP1CON	700 x.	COTAL!	CCP1X	CCP1Y	CCP1M3	CCP1M2	CCP1M1	CCP1M0	00 0000	00 0000
18h	RCSTA	SPEN	RX9	SREN	CREN	<u></u>	FERR	OERR	RX9D	0000 -00x	0000 -00x
19h	TXREG	USART Tran	nsmit Data F	Register						0000 0000	0000 0000
1Ah	RCREG	USART Red	ceive Data F	Register		MM	100 Y.C	Time	N	0000 0000	0000 0000
1Bh	CCPR2L	Capture/Co	mpare/PWN	12 (LSB)	Ĭ.	MMM	· rooy	COR	TWI	xxxx xxxx	uuuu uuuu
1Ch	CCPR2H	Capture/Co	mpare/PWN	12 (MSB)	N	WW	N.To.	I.COM	WT	xxxx xxxx	uuuu uuuu
1Dh	CCP2CON	W.	100	CCP2X	CCP2Y	CCP2M3	CCP2M2	CCP2M1	CCP2M0	00 0000	00 0000
1Eh-1Fh	_	Unimpleme	nted	COM:	1	-	MW.10	=1 CO	Mir	_	TO THE STATE OF TH

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented location read as '0'. Shaded locations are unimplemented, read as '0'.

- Note 1: These registers can be addressed from any bank.
 - 2: The upper byte of the Program Counter (PC) is not directly accessible. PCLATH is a holding register for the PC whose contents are transferred to the upper byte of the program counter. (PC<12:8>)
 - 3: Other (non power-up) resets include external reset through MCLR and the Watchdog Timer reset.
 - 4: PIE1<6> and PIR1<6> are reserved on the PIC16C66/67, always maintain these bits clear.
 - 5: PORTD, PORTE, TRISD, and TRISE are not implemented on the PIC16C66, read as '0'.
 - 6: PSPIF (PIR1<7>) and PSPIE (PIE1<7>) are reserved on the PIC16C66, maintain these bits clear.

TABLE 4-6: SPECIAL FUNCTION REGISTERS FOR THE PIC16C66/67 (Cont.'d)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets ⁽³⁾		
Bank 1	A	-XW.1	10 7	MIT	-1	TXXI'	N.100 x	COM	1				
80h ⁽¹⁾	INDF	Addressing	this location	uses conte	ents of FSR to	address da	ta memory (r	ot a physica	l register)	0000 0000	0000 0000		
81h	OPTION	RBPU	INTEDG	TOCS	TOSE	PSA	PS2	PS1	PS0	1111 1111	1111 1111		
82h ⁽¹⁾	PCL	Program Co	ounter's (PC)	Least Sig	gnificant Byte	W	1111	OY.Co	TIV	0000 0000	0000 0000		
83h ⁽¹⁾	STATUS	IRP	RP1	RP0	TO	PD	Z	DC	С	0001 1xxx	000q quuu		
84h ⁽¹⁾	FSR	Indirect data	a memory a	ddress poin	ter		WW.	any.C	OM	xxxx xxxx	uuuu uuuu		
85h	TRISA		114.10	PORTA Da	ata Direction R	egister	VIVI	100	COMP	11 1111	11 1111		
86h	TRISB	PORTB Dat	ta Direction I	Register	OWITH		11	N.100	MOD	1111 1111	1111 1111		
87h	TRISC	PORTC Da	ta Direction	Register	MIT	Ň.	MAN	100	7.00	1111 1111	1111 1111		
88h ⁽⁵⁾	TRISD	PORTD Da	ta Direction I	Register	Con	V	WW	100	M.Co.	1111 1111	1111 1111		
89h ⁽⁵⁾	TRISE	IBF	OBF	IBOV	PSPMODE	rv i	PORTE Da	ta Direction	Bits	0000 -111	0000 -111		
8Ah ^(1,2)	PCLATH	si –	- T W	11:100	Write Buffer	for the upp	er 5 bits of th	e Program C	ounter	0 0000	0 0000		
8Bh ⁽¹⁾	INTCON	GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000 000x	0000 000u		
8Ch	PIE1	PSPIE ⁽⁶⁾	(4)	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000		
8Dh	PIE2	777	_ 1/1	- 1.1	100 -	MITTY	_	-	CCP2IE		0		
8Eh	PCON	LIN	_ ~	1 N	1007.	ONA.T	_	POR	BOR	qq	uu		
8Fh	W.Co.	Unimpleme	nted	MM	1100Y.C		W	MA	-x 10	77.			
90h	CC C	Unimpleme	nted	WW	N. P	$C_{O_{2,2}}$	TW	W	W. Aur	ON CO.	(ET)		
91h	100 = C	Unimpleme	nted	Wire	M. Jac	1 CO $_{D_{1}}$	- TN	1	MM	ONT.CO	W		
92h	PR2	Timer2 Peri	od Register	71	MN.100	-1 CO	1.1		TINN.	1111 1111	1111 1111		
93h	SSPADD	Synchronou	ıs Serial Por	t (I ² C mode	e) Address Reg	ister	M.I.M	,	VV - XVV	0000 0000	0000 0000		
94h	SSPSTAT	SMP	CKE	D/Ā	Р	S	R/W	UA	BF	0000 0000	0000 0000		
95h	$M \cdot \overline{\overline{z}}$	Unimpleme	nted	4	MMM	MY.C	OF T	N	MM	TON	=11		
96h	11/1/200	Unimpleme	nted			N.	CO_{Mr} .	W	WV	M.= 004			
97h	- 11 H	Unimpleme	nted	Т	TANW	100	COM			MATTO	4 COM		
98h	TXSTA	CSRC	TX9	TXEN	SYNC	$^{N.7\overline{\sigma}_{0.3}}$	BRGH	TRMT	TX9D	0000 -010	0000 -010		
99h	SPBRG	Baud Rate	Generator R	egister	Mari	N 100	Y.0	LTW		0000 0000	0000 0000		
9Ah	MAN	Unimplemented								MNT.	1007.		
9Bh	TATE OF THE STATE	Unimpleme	Unimplemented							MAIN	Ind I.C		
9Ch	- TXX	Unimpleme	nted	N	WW	- - 0 V							
9Dh	11.	Unimpleme	nimplemented										
9Eh	-1/1	Unimpleme	nted	MIL		M A.	1.100 X.	OM!	LAA	71	W. 100		
9Fh	- 48	Unimpleme	nted		N	WW	Your	·CO	TW	-41/4	100		

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented location read as '0'. Shaded locations are unimplemented, read as '0'.

- Note 1: These registers can be addressed from any bank.
 - 2: The upper byte of the Program Counter (PC) is not directly accessible. PCLATH is a holding register for the PC whose contents are transferred to the upper byte of the program counter. (PC<12:8>)
 - 3: Other (non power-up) resets include external reset through MCLR and the Watchdog Timer reset.
 - 4: PIE1<6> and PIR1<6> are reserved on the PIC16C66/67, always maintain these bits clear.
 - 5: PORTD, PORTE, TRISD, and TRISE are not implemented on the PIC16C66, read as '0'.
 - 6: PSPIF (PIR1<7>) and PSPIE (PIE1<7>) are reserved on the PIC16C66, maintain these bits clear.

TABLE 4-6: SPECIAL FUNCTION REGISTERS FOR THE PIC16C66/67 (Cont.'d)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets ⁽³⁾
Bank 2		-41	N.100 x	COM		-1	WW.10	=1 CC	$M_{1,1}$	*1	
100h ⁽¹⁾	INDF	Addressing	this location	uses conte	ents of FSR to	address data	a memory (n	ot a physica	l register)	0000 0000	0000 0000
101h	TMR0	Timer0 mo	dule's registe	r	NITN		NA	1007.	-0M. ⁷	xxxx xxxx	uuuu uuuu
102h ⁽¹⁾	PCL	Program C	ounter's (PC)	Least Sign	ificant Byte					0000 0000	0000 0000
103h ⁽¹⁾	STATUS	IRP	RP1	RP0	TO	PD	Z	DC	С	0001 1xxx	000q quuu
104h ⁽¹⁾	FSR	Indirect da	ta memory ac	ldress point	ter	N.	WW	M.r.	N.COP	xxxx xxxx	uuuu uuuu
105h	$W.T_{\perp}$	Unimpleme	ented	100	COM.	. 1	-313	NW.To.	ST CO		_
106h	PORTB	PORTB Da	ata Latch whe	n written: P	ORTB pins w	hen read		W.M)U - C (xxxx xxxx	uuuu uuuu
107h	- 1 T	Unimpleme	ented	100	Y.C.	(TW	1/	753	100 x.	-ONETW	_
108h	OF	Unimpleme	ented	11	W.Cor	TW	4	MM	100 X.	7.7	_
109h	$C_{OD/I}$.	Unimpleme	ented	NN.IO	CO	NI.		WWW	You	COF	W -
10Ah ^(1,2)	PCLATH			W 41.1	Write Buffer	for the uppe	r 5 bits of the	e Program C	Counter	0 0000	0 0000
10Bh ⁽¹⁾	INTCON	GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000 000x	0000 000u
10Ch- 10Fh	7. CC	Unimpleme	ented		NW.10	ON.EON	W				
Bank 3	00 x	$O_{M^{*}T}$	×1	TWW.	V.CO	W					
180h ⁽¹⁾	INDF	Addressing	this location	uses conte	ents of FSR to	address data	a memory (n	ot a physica	l register)	0000 0000	0000 0000
181h	OPTION	RBPU	INTEDG	T0CS	TOSE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
182h ⁽¹⁾	PCL	Program C	ounter's (PC)	Least Sig	nificant Byte					0000 0000	0000 0000
183h ⁽¹⁾	STATUS	IRP	RP1	RP0	ТО	PD	Z	DC	С	0001 1xxx	000q quuu
184h ⁽¹⁾	FSR	Indirect da	ta memory ac	ldress point	ter	ON C	Oh	W	WV	xxxx xxxx	uuuu uuuu
185h	W/#.10	Unimpleme	ented		WW	Too	$CO_{Mr.}$	TXN	TN.	M.M.	A'CON
186h	TRISB	PORTB Da	ata Direction F	Register		N.100	COM	-31		1111 1111	1111 1111
187h	/ / · ·	Unimpleme	ented	N	M.	W.100	CON	1.1.4		TANIL	
188h	WA W	Unimpleme	ented	W	MM	1100	N.Co.	MTN		M	007
189h	TV TV	Unimpleme	ented	TW	W	MM.	W.Co	WT		M. Jan.	100 2 1.C
18Ah ^(1,2)	PCLATH	W.700	a COM		Write Buffer	for the uppe	r 5 bits of the	e Program C	Counter	0 0000	0 0000
18Bh ⁽¹⁾	INTCON	GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000 000x	0000 000u
18Ch- 19Fh	- 44	Unimpleme	ented	TW	WA	41.100					

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented location read as '0'. Shaded locations are unimplemented, read as '0'.

- Note 1: These registers can be addressed from any bank.
 - 2: The upper byte of the Program Counter (PC) is not directly accessible. PCLATH is a holding register for the PC whose contents are transferred to the upper byte of the program counter. (PC<12:8>)
 - 3: Other (non power-up) resets include external reset through MCLR and the Watchdog Timer reset.
 - 4: PIE1<6> and PIR1<6> are reserved on the PIC16C66/67, always maintain these bits clear.
 - 5: PORTD, PORTE, TRISD, and TRISE are not implemented on the PIC16C66, read as '0'.
 - 6: PSPIF (PIR1<7>) and PSPIE (PIE1<7>) are reserved on the PIC16C66, maintain these bits clear.

4.2.2.1 STATUS REGISTER

Applicable Devices

61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

The STATUS register, shown in Figure 4-9, contains the arithmetic status of the ALU, the RESET status and the bank select bits for data memory.

The STATUS register can be the destination for any instruction, as with any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the $\overline{\text{TO}}$ and $\overline{\text{PD}}$ bits are not writable. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.

For example, CLRF STATUS will clear the upper-three bits and set the Z bit. This leaves the STATUS register as 000u uluu (where u = unchanged).

It is recommended, therefore, that only BCF, BSF, SWAPF and MOVWF instructions are used to alter the STATUS register because these instructions do not affect the Z, C or DC bits from the STATUS register. For other instructions, not affecting any status bits, see the "Instruction Set Summary."

- **Note 1:** For those devices that do not use bits IRP and RP1 (STATUS<7:6>), maintain these bits clear to ensure upward compatibility with future products.
- Note 2: The C and DC bits operate as a borrow and digit borrow bit, respectively, in subtraction. See the SUBLW and SUBWF instructions for examples.

FIGURE 4-9: STATUS REGISTER (ADDRESS 03h, 83h, 103h, 183h)

R/W-0 IRP	R/W-0 RP1	R/W-0 RP0	R-1 TO	R-1 PD	R/W-x	R/W-x DC	R/W-x	R = Readable bit				
bit7	I.COM	TW	W	WW.100	oy.CO	M.TW	bit0	W = Writable bit - n = Value at POR reset x = unknown				
bit 7:	IRP: RegIster Bank Select bit (used for indirect addressing) 1 = Bank 2, 3 (100h - 1FFh) 0 = Bank 0, 1 (00h - FFh)											
bit 6-5:	11 = Bank 10 = Bank 01 = Bank 00 = Bank Each bank	Register Ba 3 (180h - 18 2 (100h - 17 1 (80h - FFI 0 (00h - 7FI is 128 byte	FFh) 7Fh) n) n)	性特力电子	材 料 886-3-5753170 (上海) 86-21-54151736 (深圳) 86-755-83298787							
bit 4:		out bit ower-up, CL time-out oc		uction, or S		Http://www.100y.com.tw						
bit 3:		-down bit ower-up or b cution of the			tion							
bit 2:	Z: Zero bit 1 = The result of an arithmetic or logic operation is zero 0 = The result of an arithmetic or logic operation is not zero											
bit 1:	DC : Digit carry/borrow bit (for ADDWF, ADDLW, SUBLW, and SUBWF instructions) (For borrow the polarity is reversed 1 = A carry-out from the 4th low order bit of the result occurred 0 = No carry-out from the 4th low order bit of the result											
bit 0:	C: Carry/borrow bit (for ADDWF, ADDLW, SUBLW, and SUBWF instructions) (For borrow the polarity is reversed). 1 = A carry-out from the most significant bit of the result occurred 0 = No carry-out from the most significant bit of the result Note: a subtraction is executed by adding the two's complement of the second operand. For rotate (RRF, RLF) instructions, this bit is loaded with either the high or low order bit of the source register.											

4.2.2.2 **OPTION REGISTER**

Applicable Devices

61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

The OPTION register is a readable and writable register which contains various control bits to configure the TMR0/WDT prescaler, the external INT interrupt, TMR0, and the weak pull-ups on PORTB.

Note: To achieve a 1:1 prescaler assignment for TMR0 register, assign the prescaler to the Watchdog Timer.

FIGURE 4-10: OPTION REGISTER (ADDRESS 81h, 181h)

R/W-1	R/W-1	R/W-1 R	/W-1	R/W-1	R/W-1	R/W-1	R/W-1	OOY.COM.TW					
RBPU	INTEDG	- 4 1 1 1	0SE	PSA	PS2	PS1	PS0	R = Readable bit					
bit7	M.TW M.TW	W	MM	W = Writable bit U = Unimplemented bit, read as '0' - n = Value at POR reset									
bit 7:	RBPU: PORTB Pull-up Enable bit 1 = PORTB pull-ups are disabled 0 = PORTB pull-ups are enabled by individual port latch values												
bit 6:	INTEDG: Interrupt Edge Select bit 1 = Interrupt on rising edge of RB0/INT pin 0 = Interrupt on falling edge of RB0/INT pin												
bit 5:	TOCS: TMR0 Clock Source Select bit 1 = Transition on RA4/T0CKI pin 0 = Internal instruction cycle clock (CLKOUT)												
bit 4:	T0SE: TMR0 Source Edge Select bit 1 = Increment on high-to-low transition on RA4/T0CKI pin 0 = Increment on low-to-high transition on RA4/T0CKI pin												
bit 3:	PSA: Prescaler Assignment bit 1 = Prescaler is assigned to the WDT 0 = Prescaler is assigned to the Timer0 module												
bit 2-0:	PS2:PS0 : P	rescaler Rate	Select	MWW.Inc. COM									
	Bit Value	TMR0 Rate	WDT	Rate				WW.100 CO					
	000 001 010 011 100 101 110	1:2 1:4 1:8 1:16 1:32 1:64 1:128 1:256	1: 1:	2 4				M.T.M. M.M.Y.100.Y.C.C.C.C.C.C.C.C.C.C.C.C.C.C.C.C.C.C					
								WY WY TOO					

4.2.2.3 INTCON REGISTER

Applicable Devices

61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

The INTCON Register is a readable and writable register which contains the various enable and flag bits for the TMR0 register overflow, RB port change and external RB0/INT pin interrupts.

Note: Interrupt flag bits get set when an interrupt condition occurs regardless of the state of its corresponding enable bit or the global enable bit, GIE (INTCON<7>).

FIGURE 4-11: INTCON REGISTER (ADDRESS 0Bh, 8Bh, 10Bh 18Bh)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-x	
GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	R = Readable bit
oit7	TW LTW M.TW	W	NWW.10	100 ^X ·CO	M.TW OM.TW	7	bitO	W = Writable bit U = Unimplemented bit, read as '0' - n = Value at POR reset x = unknown
bit 7:		s all un-ma	ipt Enable b asked interr rupts					
bit 6:	1 = Enable	s all un-ma	nterrupt Ena asked perip heral interru	neral interru	ipts O		WW	W.100Y.COM.TW
bit 5:	1 = Enable	s the TMR	v Interrupt E 0 overflow i 0 overflow	nterrupt			胜华	特 力 材 料 886-3-5753170 寺力电子(上海) 86-21-5415173 寺力电子(深圳) 86-755-832987
bit 4:	1 = Enable	s the RB0	nal Interrup /INT externa)/INT extern	al interrupt			N M	Http://www.100y.com.tw
bit 3:	1 = Enable	s the RB p	ge Interrupt oort change port change	interrupt				
bit 2:	1 = TMR0	register ov	v Interrupt F erflowed (m d not overflo	ust be clea	red in softwa	re)		
bit 1:	1 = The RE	30/INT exte	nal Interrup ernal interru ernal interru	pt occurred	(must be cle	eared in soft	ware)	
bit 0:	1 = At leas	t one of th	ge Interrupt e RB7:RB4 :RB4 pins ha	pins chang	ed state (see d state	e Section 5.2	to clear the	e interrupt)
Note 1:		led by the						red, the GIE bit may unintentionally Refer to Section 13.5 for a detailed

global enable bit, GIE (INTCON<7>). User software should ensure the appropriate interrupt flag bits are clear prior to

enabling an interrupt.

PIC16C6X

4.2.2.4 PIE1 REGISTER

Applicable Devices

61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

This register contains the individual enable bits for the peripheral interrupts.

Note: Bit PEIE (INTCON<6>) must be set to enable any peripheral interrupt.

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FIGURE 4-12: PIE1 REGISTER FOR PIC16C62/62A/R62 (ADDRESS 8Ch)

RW-0	R/W-0	U-0 —	U-0 —	R/W-0 SSPIE	R/W-0 CCP1IE	R/W-0 TMR2IE	R/W-0 TMR1IE	R = Readable bit
bit7	M.TW	V	NWW.1	100 ^{Y.CC}	OM.TW	V	bit0	W = Writable bit U = Unimplemented bit, read as '0' - n = Value at POR reset
bit 7-6:	Reserved:	Always ma	aintain these	e bits clear.				W.100 F. COM: 1
bit 5-4:	Unimplem	ented: Rea	ad as '0'					
bit 3:	SSPIE: Syr 1 = Enables 0 = Disable	s the SSP	interrupt	Interrupt Er	nable bit			
bit 2:	CCP1IE: Control of the control of th	s the CCP	1 interrupt	bit				
bit 1:	TMR2IE: TI 1 = Enables 0 = Disable	s the TMR2	2 to PR2 ma	atch interru	ot 100 X			
bit 0:	TMR1IE: TI 1 = Enables 0 = Disable	s the TMR	1 overflow in	nterrupt	NN.100			

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FIGURE 4-13: PIE1 REGISTER FOR PIC16C63/R63/66 (ADDRESS 8Ch)

R/W-0 R/W-0 R/W-0 R/W-0 R/W-0 R/W-0 R/W-0 R/W-0 **RCIE SSPIE** CCP1IE TMR2IE TMR1IE TXIE = Readable bit = Writable bit W bit7 bit0 = Unimplemented bit, read as '0' = Value at POR reset bit 7-6: Reserved: Always maintain these bits clear. RCIE: USART Receive Interrupt Enable bit 1 = Enables the USART receive interrupt 勝 特 力 材 料 886-3-5753170 0 = Disables the USART receive interrupt 胜特力电子(上海) 86-21-54151736 bit 4: TXIE: USART Transmit Interrupt Enable bit 1 = Enables the USART transmit interrupt 胜特力电子(深圳) 86-755-83298787 0 = Disables the USART transmit interrupt Http://www. 100y. com. tw bit 3: SSPIE: Synchronous Serial Port Interrupt Enable bit 1 = Enables the SSP interrupt 0 = Disables the SSP interrupt CCP1IE: CCP1 Interrupt Enable bit bit 2: 1 = Enables the CCP1 interrupt 0 = Disables the CCP1 interrupt bit 1: TMR2IE: TMR2 to PR2 Match Interrupt Enable bit 1 = Enables the TMR2 to PR2 match interrupt 0 = Disables the TMR2 to PR2 match interrupt bit 0: TMR1IE: TMR1 Overflow Interrupt Enable bit 1 = Enables the TMR1 overflow interrupt 0 = Disables the TMR1 overflow interrupt

FIGURE 4-14: PIE1 REGISTER FOR PIC16C64/64A/R64 (ADDRESS 8Ch)

R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	1007
PSPIE	700	OM.,		SSPIE	CCP1IE	TMR2IE	TMR1IE	R = Readable bit
oit7							bit0	W = Writable bit U = Unimplemented bit, read as '0' - n = Value at POR reset
oit 7:	PSPIE: Para 1 = Enables 0 = Disables	the PSP r	ead/write i	nterrupt	rupt Enable b	oit C		WWW.100Y.C
oit 6:	Reserved:	Always ma	intain this	bit clear.				
oit 5-4:	Unimpleme	ented: Rea	d as '0'					
oit 3:	SSPIE : Syn 1 = Enables 0 = Disables	the SSP is	nterrupt	Interrupt Er	nable bit			
oit 2:	CCP1IE: CO 1 = Enables 0 = Disables	the CCP1	interrupt	bit				
oit 1:	TMR2IE: TM 1 = Enables 0 = Disables	the TMR2	to PR2 m	atch interru	ot			
bit 0:	TMR1IE: TM 1 = Enables 0 = Disables	the TMR1	overflow i	nterrupt	TW			

FIGURE 4-15: PIE1 REGISTER FOR PIC16C65/65A/R65/67 (ADDRESS 8Ch)

PSPIE bit7		RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE bit0	R = Readable bit W = Writable bit U = Unimplemented bit, read as '0' - n = Value at POR reset
bit 7:	PSPIE: Par 1 = Enables 0 = Disable	s the PSP	read/write i	nterrupt	upt Enable t	oit		Y.COM.TW
bit 6:	Reserved:	Always ma	aintain this	bit clear.				00Y.CO
bit 5:	RCIE: USA 1 = Enables 0 = Disable	s the USAF	RT receive	interrupt				100Y.COM.TW
bit 4:	TXIE: USA 1 = Enables 0 = Disable	s the USAF	RT transmit	interrupt				W.100Y.COM.TW
bit 3:	SSPIE: Syr 1 = Enables 0 = Disable	s the SSP	interrupt	Interrupt Er	able bit			WW.100Y.COM.TW
bit 2:	CCP1IE: Control of the control of th	s the CCP	1 interrupt	bit				MMM.100X.COW.TM
bit 1:	TMR2IE: TI 1 = Enables 0 = Disable	s the TMR2	2 to PR2 m	atch interru	ot .			WWW.100Y.COM.TW
bit 0:	TMR1IE: TI 1 = Enable:	s the TMR		nterrupt	W.100X			MMM.100X.COW.1

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4.2.2.5 PIR1 REGISTER

Applicable Devices

61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

This register contains the individual flag bits for the peripheral interrupts.

Interrupt flag bits get set when an interrupt condition occurs regardless of the state of its corresponding enable bit or the global enable bit, GIE (INTCON<7>). User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

FIGURE 4-16: PIR1 REGISTER FOR PIC16C62/62A/R62 (ADDRESS 0Ch)

R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	
WITH A	_	11/4	4 100 X	SSPIF	CCP1IF	TMR2IF	TMR1IF	R = Readable bit
bit7	N	MM	W.100	Y.COM	TW	WV	bit0	W = Writable bit U = Unimplemented bit,
								read as '0' - n = Value at POR reset

Note:

- bit 7-6: Reserved: Always maintain these bits clear.
- bit 5-4: Unimplemented: Read as '0'
- bit 3: SSPIF: Synchronous Serial Port Interrupt Flag bit
 - 1 = The transmission/reception is complete (must be cleared in software)
 - 0 = Waiting to transmit/receive
- bit 2: CCP1IF: CCP1 Interrupt Flag bit

Capture Mode

- 1 = A TMR1 register capture occurred (must be cleared in software)
- 0 = No TMR1 register capture occurred

Compare Mode

- 1 = A TMR1 register compare match occurred (must be cleared in software)
- 0 = No TMR1 register compare match occurred

PWM Mode

Unused in this mode

- bit 1: TMR2IF: TMR2 to PR2 Match Interrupt Flag bit
 - 1 = TMR2 to PR2 match occurred (must be cleared in software)
 - 0 = No TMR2 to PR2 match occurred
- bit 0: TMR1IF: TMR1 Overflow Interrupt Flag bit
 - 1 = TMR1 register overflow occurred (must be cleared in software)
 - 0 = No TMR1 register overflow occurred

Interrupt flag bits get set when an interrupt condition occurs regardless of the state of its corresponding enable bit or the global enable bit, GIE (INTCON<7>). User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

FIGURE 4-17: PIR1 REGISTER FOR PIC16C63/R63/66 (ADDRESS 0Ch)

R/W-0 R/W-0 R/W-0 R-0 R-0 R/W-0 R/W-0 R/W-0 **RCIF TXIF** SSPIF CCP1IF TMR2IF TMR1IF bit7 bit0

= Readable bit

V = Writable bit

U = Unimplemented bit, read as '0'

n = Value at POR reset

bit 7-6: Reserved: Always maintain these bits clear.

bit 5: RCIF: USART Receive Interrupt Flag bit

1 = The USART receive buffer is full (cleared by reading RCREG)

0 = The USART receive buffer is empty

bit 4: TXIF: USART Transmit Interrupt Flag bit

1 = The USART transmit buffer is empty (cleared by writing to TXREG)

0 = The USART transmit buffer is full

bit 3: SSPIF: Synchronous Serial Port Interrupt Flag bit

1 = The transmission/reception is complete (must be cleared in software)

0 = Waiting to transmit/receive

bit 2: CCP1IF: CCP1 Interrupt Flag bit

Capture Mode

1 = A TMR1 register capture occurred (must be cleared in software)

0 = No TMR1 register capture occurred

Compare Mode

1 = A TMR1 register compare match occurred (must be cleared in software)

0 = No TMR1 register compare match occurred

PWM Mode

Unused in this mode

bit 1: TMR2IF: TMR2 to PR2 Match Interrupt Flag bit

1 = TMR2 to PR2 match occurred (must be cleared in software)

0 = No TMR2 to PR2 match occurred

bit 0: TMR1IF: TMR1 Overflow Interrupt Flag bit

1 = TMR1 register overflow occurred (must be cleared in software)

0 = No TMR1 register overflow occurred

Interrupt flag bits get set when an interrupt condition occurs regardless of the state of its corresponding enable bit or the global enable bit, GIE (INTCON<7>). User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

FIGURE 4-18: PIR1 REGISTER FOR PIC16C64/64A/R64 (ADDRESS 0Ch)

 R/W-0
 R/W-0
 U-0
 U-0
 R/W-0
 R/W-0
 R/W-0
 R/W-0

 PSPIF
 —
 —
 —
 SSPIF
 CCP1IF
 TMR2IF
 TMR1IF

 bit7
 bit0

R = Readable bit W = Writable bit

U = Unimplemented bit, read as '0' - n = Value at POR reset

bit 7: **PSPIF:** Parallel Slave Port Interrupt Flag bit

1 = A read or a write operation has taken place (must be cleared in software)

0 = No read or write operation has taken place

bit 6: Reserved: Always maintain this bit clear.

bit 5-4: Unimplemented: Read as '0'

bit 3: SSPIF: Synchronous Serial Port Interrupt Flag bit

1 = The transmission/reception is complete (must be cleared in software)

0 = Waiting to transmit/receive

bit 2: CCP1IF: CCP1 Interrupt Flag bit

Capture Mode

1 = A TMR1 register capture occurred (must be cleared in software)

0 = No TMR1 register capture occurred

Compare Mode

1 = A TMR1 register compare match occurred (must be cleared in software)

0 = No TMR1 register compare match occurred

PWM Mode

Unused in this mode

bit 1: TMR2IF: TMR2 to PR2 Match Interrupt Flag bit

1 = TMR2 to PR2 match occurred (must be cleared in software)

0 = No TMR2 to PR2 match occurred

bit 0: TMR1IF: TMR1 Overflow Interrupt Flag bit

1 = TMR1 register overflow occurred (must be cleared in software)

0 = No TMR1 register occurred

Interrupt flag bits get set when an interrupt condition occurs regardless of the state of its corresponding enable bit or the global enable bit, GIE (INTCON<7>). User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

FIGURE 4-19: PIR1 REGISTER FOR PIC16C65/65A/R65/67 (ADDRESS 0Ch)

R/W-0 R-0 R/W-0 R/W-0 R-0 R/W-0 R/W-0 R/W-0 **PSPIF RCIF TXIF** SSPIF CCP1IF TMR2IF TMR1IF bit7 bit0 PSPIF: Parallel Slave Port Interrupt Flag bit bit 7: 1 = A read or a write operation has taken place (must be cleared in software) 0 = No read or write operation has taken place bit 6: Reserved: Always maintain this bit clear. bit 5: RCIF: USART Receive Interrupt Flag bit 1 = The USART receive buffer is full (cleared by reading RCREG) 0 = The USART receive buffer is empty bit 4: TXIF: USART Transmit Interrupt Flag bit 1 = The USART transmit buffer is empty (cleared by writing to TXREG) 0 = The USART transmit buffer is full bit 3: SSPIF: Synchronous Serial Port Interrupt Flag bit 1 = The transmission/reception is complete (must be cleared in software) 0 = Waiting to transmit/receive bit 2: CCP1IF: CCP1 Interrupt Flag bit Capture Mode 1 = A TMR1 register capture occurred (must be cleared in software) 0 = No TMR1 register capture occurred Compare Mode 1 = A TMR1 register compare match occurred (must be cleared in software) 0 = No TMR1 register compare match occurred **PWM Mode** Unused in this mode TMR2IF: TMR2 to PR2 Match Interrupt Flag bit bit 1: 1 = TMR2 to PR2 match occurred (must be cleared in software) 0 = No TMR2 to PR2 match occurred bit 0: TMR1IF: TMR1 Overflow Interrupt Flag bit 1 = TMR1 register overflow occurred (must be cleared in software)

0 = No TMR1 register overflow occurred

Interrupt flag bits get set when an interrupt condition occurs regardless of the state of its corresponding enable bit or the global enable bit, GIE (INTCON<7>). User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

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= Readable bit= Writable bit

J = Unimplemented bit, read as '0'n = Value at POR reset

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4.2.2.6 PIE2 REGISTER

Applicable Devices

61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

FIGURE 4-20: PIE2 REGISTER (ADDRESS 8Dh)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	
(F)	_		10 0 7.6	TI	N _	ALT.	CCP2IE	R = Readable bit
bit 7-1:	Unimplem	ented: Rea	ad as '0'					- n = Value at POR res
bit 0:	CCP2IE: C 1 = Enable 0 = Disable	s the CCP2	2 interrupt	bit CO				

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4.2.2.7 PIR2 REGISTER

Applicable Devices

61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

This register contains the CCP2 interrupt flag bit.

Interrupt flag bits get set when an interrupt condition occurs regardless of the state of its corresponding enable bit or the global enable bit, GIE (INTCON<7>). User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

FIGURE 4-21: PIR2 REGISTER (ADDRESS 0Dh)

			11010				DAMO
U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
T.C.	TY	- 11		00 7.	TIM	_	CCP2IF
bit7			TWW.		Oh		bit0

2 N

Note:

= Readable bit

W = Writable bitU = Unimplemented bit, read as '0'

n = Value at POR reset

bit 7-1: Unimplemented: Read as '0'

bit 0: CCP2IF: CCP2 Interrupt Flag bit

Capture Mode

1 = A TMR1 register capture occurred (must be cleared in software)

0 = No TMR1 register capture occurred

Compare Mode

1 = A TMR1 register compare match occurred (must be cleared in software)

0 = No TMR1 register compare match occurred

PWM Mode

Unused in this mode

Interrupt flag bits get set when an interrupt condition occurs regardless of the state of its corresponding enable bit or the global enable bit, GIE (INTCON<7>). User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

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4.2.2.8 PCON REGISTER

Applicable Devices

61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

The Power Control register (PCON) contains a flag bit to allow differentiation between a Power-on Reset to an external MCLR reset or WDT reset. Those devices with brown-out detection circuitry contain an additional bit to differentiate a Brown-out Reset condition from a Power-on Reset condition.

BOR is unknown on Power-on Reset. It must then be set by the user and checked on subsequent resets to see if BOR is clear, indicating a brown-out has occurred. The BOR status bit is a "don't care" and is not necessarily predictable if the brown-out circuit is disabled (by clearing the BODEN bit in the Configuration word).

FIGURE 4-22: PCON REGISTER FOR PIC16C62/64/65 (ADDRESS 8Eh)

U-0 U-0 U-0 U-0 U-0 U-0 R/W-0 R/W-q **POR** = Readable bit W = Writable bit bit7 bit0 = Unimplemented bit, read as '0' n = Value at POR reset = value depends on conditions bit 7-2: Unimplemented: Read as '0 bit 1: POR: Power-on Reset Status bit 1 = No Power-on Reset occurred 0 = A Power-on Reset occurred (must be set in software after a Power-on Reset occurs) bit 0: Reserved This bit should be set upon a Power-on Reset by user software and maintained as set. Use of this bit as a general purpose read/write bit is not recommended, since this may affect upward compatibility with future products.

Note:

FIGURE 4-23: PCON REGISTER FOR PIC16C62A/R62/63/R63/64A/R64/65A/R65/66/67 (ADDRESS 8Eh)

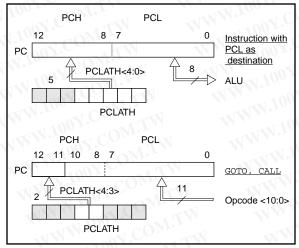
U-0 U-0 U-0 U-0 R/W-0 R/W-q U-0 U-0 **POR BOR** = Readable bit W = Writable bit bit0 = Unimplemented bit, read as '0' n = Value at POR reset = value depends on conditions bit 7-2: Unimplemented: Read as '0' bit 1: POR: Power-on Reset Status bit 1 = No Power-on Reset occurred 0 = A Power-on Reset occurred (must be set in software after a Power-on Reset occurs) bit 0: BOR: Brown-out Reset Status bit 1 = No Brown-out Reset occurred 0 = A Brown-out Reset occurred (must be set in software after a Brown-out Reset occurs)

4.3 PCL and PCLATH

Applicable Devices 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

The program counter (PC) is 13-bits wide. The low byte comes from the PCL register, which is a readable and writable register. The upper bits (PC<12:8>) are not readable, but are indirectly writable through the PCLATH register. On any reset, the upper bits of the PC will be cleared. Figure 4-24 shows the two situations for the loading of the PC. The upper example in the figure shows how the PC is loaded on a write to PCL (PCLATH<4:0> \rightarrow PCH). The lower example in the figure shows how the PC is loaded during a CALL or GOTO instruction (PCLATH<4:3> \rightarrow PCH).

FIGURE 4-24: LOADING OF PC IN DIFFERENT SITUATIONS



4.3.1 COMPUTED GOTO

A computed GOTO is accomplished by adding an offset to the program counter (ADDWF PCL). When doing a table read using a computed GOTO method, care should be exercised if the table location crosses a PCL memory boundary (each 256 word block). Refer to the application note "Implementing a Table Read" (AN556).

4.3.2 STACK

The PIC16CXX family has an 8 deep x 13-bit wide hardware stack. The stack space is not part of either program or data space and the stack pointer is not readable or writable. The PC is PUSHed onto the stack when a CALL instruction is executed or an interrupt causes a branch. The stack is POPed in the event of a RETURN, RETLW or a RETFIE instruction execution. PCLATH is not affected by a PUSH or a POP operation.

The stack operates as a circular buffer. This means that after the stack has been PUSHed eight times, the ninth push overwrites the value that was stored from the first push. The tenth push overwrites the second push (and so on).

Note 1: There are no status bits to indicate stack overflows or stack underflow conditions.

Note 2: There are no instructions mnemonics called PUSH or POP. These are actions that occur from the execution of the CALL, RETURN, RETLW, and RETFIE instructions, or the vectoring to an interrupt address

4.4 Program Memory Paging

Applicable Devices
61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

PIC16C6X devices are capable of addressing a continuous 8K word block of program memory. The CALL and GOTO instructions provide only 11 bits of address to allow branching within any 2K program memory page. When doing a CALL or GOTO instruction the upper two bits of the address are provided by PCLATH<4:3>. When doing a CALL or GOTO instruction, the user must ensure that the page select bits are programmed so that the desired program memory page is addressed. If a return from a CALL instruction (or interrupt) is executed, the entire 13-bit PC is pushed onto the stack. Therefore, manipulation of the PCLATH<4:3> bits are not required for the return instructions (which POPs the address from the stack).

Note: PIC16C6X devices with 4K or less of program memory ignore paging bit PCLATH<4>. The use of PCLATH<4> as a general purpose read/write bit is not recommended since this may affect upward compatibility with future products.

Example 4-1 shows the calling of a subroutine in page 1 of the program memory. This example assumes that the PCLATH is saved and restored by the interrupt service routine (if interrupts are used).

EXAMPLE 4-1: CALL OF A SUBROUTINE IN PAGE 1 FROM PAGE 0

```
ORG 0x500
BSF
       PCLATH. 3
                  ;Select page 1 (800h-FFFh)
BCF
       PCLATH, 4
                  ;Only on >4K devices
                  ;Call subroutine in
CALL
       SUB1_P1
                  ; page 1 (800h-FFFh)
ORG 0x900
SUB1_P1:
                  ; called subroutine
                  ;page 1 (800h-FFFh)
RETURN
                  return to Call subroutine
                  ;in page 0 (000h-7FFh)
```

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4.5 <u>Indirect Addressing, INDF and FSR</u> <u>Registers</u>

Applicable Devices

61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

The INDF register is not a physical register. Addressing the INDF register will cause indirect addressing.

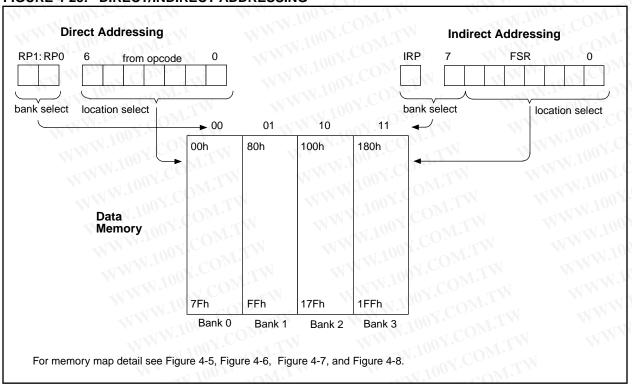
Indirect addressing is possible by using the INDF register. Any instruction using the INDF register actually accesses the register pointed to by the File Select Register, FSR. Reading the INDF register itself indirectly (FSR = '0') will produce 00h. Writing to the INDF register indirectly results in a no-operation (although status bits may be affected). An effective 9-bit address is obtained by concatenating the 8-bit FSR register and the IRP bit (STATUS<7>), as shown in Figure 4-25.

A simple program to clear RAM location 20h-2Fh using indirect addressing is shown in Example 4-2.

EXAMPLE 4-2: INDIRECT ADDRESSING

	movlw	0x20	;initialize pointer
	movwf	FSR	; to RAM
NEXT	clrf	INDF	clear INDF register;
	incf	FSR,F	;inc pointer
	btfss	FSR,4	;all done?
	goto	NEXT	;NO, clear next
CONTINUE			
	:		;YES, continue

FIGURE 4-25: DIRECT/INDIRECT ADDRESSING



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5.0 I/O PORTS

Applicable Devices 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

Some pins for these I/O ports are multiplexed with an alternate function(s) for the peripheral features on the device. In general, when a peripheral is enabled, that pin may not be used as a general purpose I/O pin.

5.1 PORTA and TRISA Register

Applicable Devices 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

All devices have a 6-bit wide PORTA, except for the PIC16C61 which has a 5-bit wide PORTA.

Pin RA4/T0CKI is a Schmitt Trigger input and an open drain output. All other RA port pins have TTL input levels and full CMOS output drivers. All pins have data direction bits (TRIS registers) which can configure these pins as output or input.

Setting a bit in the TRISA register puts the corresponding output driver in a hi-impedance mode. Clearing a bit in the TRISA register puts the contents of the output latch on the selected pin.

Reading PORTA register reads the status of the pins whereas writing to it will write to the port latch. All write operations are read-modify-write operations. Therefore, a write to a port implies that the port pins are read, this value is modified, and then written to the port data latch.

Pin RA4 is multiplexed with Timer0 module clock input to become the RA4/T0CKI pin.

EXAMPLE 5-1: INITIALIZING PORTA

```
BCF
       STATUS, RP0
BCF
       STATUS, RP1 ; PIC16C66/67 only
       PORTA
CLRF
                    ; Initialize PORTA by
                    ; clearing output
                    ; data latches
                    ; Select Bank 1
BSF
       STATUS, RPO
MOVLW
       OxCF
                     ; Value used to
                      initialize data
                      direction
                      Set RA<3:0> as inputs
                      RA<5:4> as outputs
                      TRISA<7:6> are always
                      read as 'O'
```

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FIGURE 5-1: BLOCK DIAGRAM OF THE RA3:RA0 PINS AND THE RA5 PIN

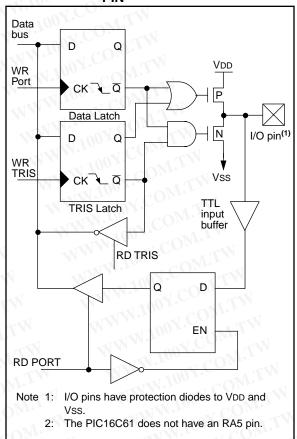
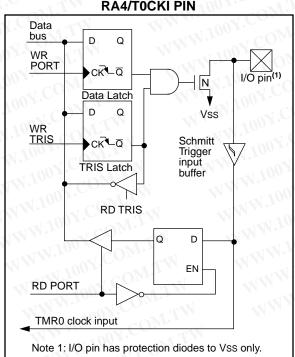


FIGURE 5-2: BLOCK DIAGRAM OF THE RA4/T0CKI PIN



PIC16C6X

PORTA FUNCTIONS TABLE 5-1:

Name	Bit#	Buffer Type	Function
RA0	bit0	TICON	Input/output
RA1	bit1	W.JUNTIL CON	Input/output
RA2	bit2	1 (TTL	Input/output
RA3	bit3	TILY	Input/output
RA4/T0CKI	bit4	ST C	Input/output or external clock input for Timer0. Output is open drain type.
RA5/SS (1)	bit5	TTLOOK	Input/output or slave select input for synchronous serial port.

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TABLE 5-2: REGISTERS/BITS ASSOCIATED WITH PORTA

Note 1:	The PIC1	16C61	does r	ot have PC)RTA<5>	or TRISA	<5>, read	as '0'.			
TABLE 5	5-2: F	REGIS	TERS	S/BITS AS	SOCIAT	ED WIT	H PORT	AWW			
Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets
05h	PORTA		_	RA5 ⁽¹⁾	RA4	RA3	RA2	RA1	RA0	xx xxxx	uu uuuu
85h	TRISA		_	PORTA Data	Direction Re	egister ⁽¹⁾	TW		WWW	11 1111	11 1111

WWW.100Y.COM.TW Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by PORTA.

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Note 1: PORTA<5> and TRISA<5> are not implemented on the PIC16C61, read as '0'.

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5.2 **PORTB and TRISB Register**

Applicable Devices

61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

PORTB is an 8-bit wide bi-directional port. The corresponding data direction register is TRISB. Setting a bit in the TRISB register puts the corresponding output driver in a hi-impedance mode. Clearing a bit in the TRISB register puts the contents of the output latch on the selected pin(s).

EXAMPLE 5-2: INITIALIZING PORTB

```
BCF
       STATUS, RP0
CLRF
       PORTB
                     ; Initialize PORTB by
                     ; clearing output
                     ; data latches
BSE
       STATUS. RPO
                    ; Select Bank 1
MOVLW
      0xCF
                     ; Value used to
                     ; initialize data
                     ; direction
MOVWF
      TRISB
                     ; Set RB<3:0> as inputs
                     ; RB<5:4> as outputs
                     ; RB<7:6> as inputs
```

Each of the PORTB pins has a weak internal pull-up. A single control bit can turn on all the pull-ups. This is performed by clearing bit RBPU (OPTION<7>). The weak pull-up is automatically turned off when the port pin is configured as an output. The pull-ups are also disabled on a Power-on Reset.

Four of PORTB's pins, RB7:RB4, have an interrupt on change feature. Only pins configured as inputs can cause this interrupt to occur (i.e., any RB7:RB4 pin configured as an output is excluded from the interrupt on change comparison). The input pins (of RB7:RB4) are compared with the old value latched on the last read of PORTB. The "mismatch" outputs of RB7:RB4 are OR'ed together to generate the RB port change interrupt with flag bit RBIF (INTCON<0>).

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This interrupt can wake the device from SLEEP. The user, in the interrupt service routine, can clear the interrupt in the following manner:

- Any read or write of PORTB. This will end the mismatch condition.
- Clear flag bit RBIF. b)

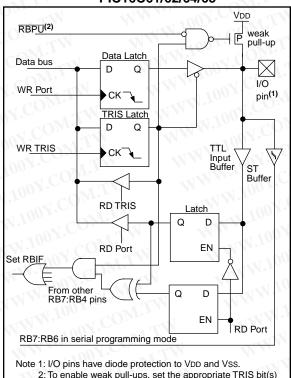
A mismatch condition will continue to set flag bit RBIF. Reading PORTB will end the mismatch condition, and allow flag bit RBIF to be cleared.

This interrupt on mismatch feature, together with software configurable pull-ups on these four pins allow easy interface to a keypad and make it possible for wake-up on key-depression. Refer to the Embedded Control Handbook, Application Note, "Implementing Wake-up on Key Stroke" (AN552).

Note: For PIC16C61/62/64/65, if a change on the I/O pin should occur when a read operation is being executed (start of the Q2 cycle), then interrupt flag bit RBIF may not get set.

The interrupt on change feature is recommended for wake-up on key depression operation and operations where PORTB is only used for the interrupt on change feature. Polling of PORTB is not recommended while using the interrupt on change feature.

FIGURE 5-3: **BLOCK DIAGRAM OF THE RB7:RB4 PINS FOR** PIC16C61/62/64/65



2: To enable weak pull-ups, set the appropriate TRIS bit(s) and clear the RPBU bit (OPTION<7>).

BLOCK DIAGRAM OF THE FIGURE 5-4: **RB7:RB4 PINS FOR** PIC16C62A/63/R63/64A/65A/

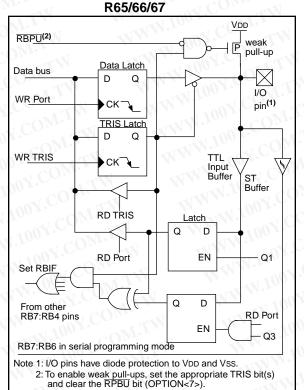


FIGURE 5-5: **BLOCK DIAGRAM OF THE RB3:RB0 PINS**

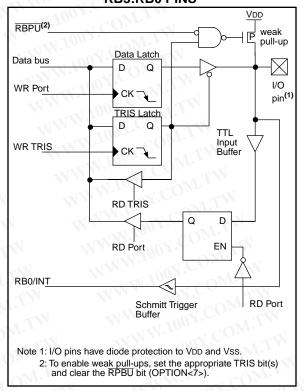


TABLE 5-3: PORTB FUNCTIONS

and oldar	the Ri Bo i	oit (OPTION<75).	TAIN TO THE WAY TO THE
TABLE 5-3:	POR	TB FUNCTION	IS CONTRACTON THE TANK TO NOT
Name	Bit#	Buffer Type	Function
RB0/INT	bit0	TTL/ST ⁽¹⁾	Input/output pin or external interrupt input. Internal software programmable weak pull-up.
RB1	bit1	COLLE	Input/output pin. Internal software programmable weak pull-up.
RB2	bit2	TTL	Input/output pin. Internal software programmable weak pull-up.
RB3	bit3	OY. TTL T	Input/output pin. Internal software programmable weak pull-up.
RB4	bit4	OOY.TTL	Input/output pin (with interrupt on change). Internal software programmable weak pull-up.
RB5	bit5	100XLL	Input/output pin (with interrupt on change). Internal software programmable weak pull-up.
RB6	bit6	TTL/ST ⁽²⁾	Input/output pin (with interrupt on change). Internal software programmable weak pull-up. Serial programming clock.
RB7	bit7	TTL/ST ⁽²⁾	Input/output pin (with interrupt on change). Internal software programmable weak pull-up. Serial programming data.

Legend: TTL = TTL input, ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.

2: This buffer is a Schmitt Trigger input when used in serial programming mode.

TABLE 5-4: SUMMARY OF REGISTERS ASSOCIATED WITH PORTB

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets
06h, 106h	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx xxxx	uuuu uuuuu
86h, 186h	TRISB	PORTB D	ata Direction	1111 1111	1111 1111						
81h, 181h	OPTION	RBPU	INTEDG	T0CS	TOSE	PSA	PS2	PS1	PS0	1111 1111	1111 1111

Legend: x = unknown, u = unchanged. Shaded cells are not used by PORTB.

5.3 PORTC and TRISC Register

Applicable Devices
61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

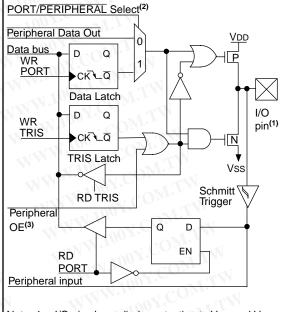
PORTC is an 8-bit wide bi-directional port. Each pin is individually configurable as an input or output through the TRISC register. PORTC is multiplexed with several peripheral functions (Table 5-5). PORTC pins have Schmitt Trigger input buffers.

When enabling peripheral functions, care should be taken in defining TRIS bits for each PORTC pin. Some peripherals override the TRIS bit to make a pin an output, while other peripherals override the TRIS bit to make a pin an input. Since the TRIS bit override is in effect while the peripheral is enabled, read-modify-write instructions (BSF, BCF, XORWF) with TRISC as destination should be avoided. The user should refer to the corresponding peripheral section for the correct TRIS bit settings.

EXAMPLE 5-3: INITIALIZING PORTC

BCF STATUS, RPO STATUS, RP1 BCF ; PIC16C66/67 only CLRF PORTC ; Initialize PORTC by clearing output ; data latches BSF STATUS, RPO ; Select Bank 1 MOVLW 0xCF ; Value used to initialize data direction Set RC<3:0> as inputs MOVWF ; RC<5:4> as outputs ; RC<7:6> as inputs

FIGURE 5-6: PORTC BLOCK DIAGRAM



- Note 1: I/O pins have diode protection to VDD and Vss.
 - 2: Port/Peripheral select signal selects between port data and peripheral output.
 - Peripheral OE (output enable) is only activated if peripheral select is active.

TABLE 5-5: PORTC FUNCTIONS FOR PIC16C62/64

Name	Bit#	Buffer Type	Function
RC0/T1OSI/T1CKI	bit0	ST	Input/output port pin or Timer1 oscillator input or Timer1 clock input
RC1/T1OSO	bit1	ST	Input/output port pin or Timer1 oscillator output
RC2/CCP1	bit2	ST	Input/output port pin or Capture1 input/Compare1 output/PWM1 output
RC3/SCK/SCL	bit3	ST	RC3 can also be the synchronous serial clock for both SPI and PC modes.
RC4/SDI/SDA	bit4	COST	RC4 can also be the SPI Data In (SPI mode) or data I/O (PC mode).
RC5/SDO	bit5	ST	Input/output port pin or synchronous serial port data output
RC6	bit6	ST	Input/output port pin
RC7	bit7	ST	Input/output port pin

Legend: ST = Schmitt Trigger input

PORTC FUNCTIONS FOR PIC16C62A/R62/64A/R64 **TABLE 5-6:**

Name	Bit#	Buffer Type	Function
RC0/T1OSO/T1CKI	bit0	ST	Input/output port pin or Timer1 oscillator output or Timer1 clock input
RC1/T1OSI	bit1	ST	Input/output port pin or Timer1 oscillator input
RC2/CCP1	bit2	ST	Input/output port pin or Capture input/Compare output/PWM1 output
RC3/SCK/SCL	bit3	ST	RC3 can also be the synchronous serial clock for both SPI and PC modes
RC4/SDI/SDA	bit4	ST	RC4 can also be the SPI Data In (SPI mode) or data I/O (PC mode).
RC5/SDO	bit5	ST	Input/output port pin or synchronous serial port data output
RC6	bit6	ST	Input/output port pin
RC7	bit7	ST	Input/output port pin

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TABLE 5-7: PORTC FUNCTIONS FOR PIC16C63/R63/65/65A/R65/66/67

Name	Bit#	Buffer Type	Function
RC0/T1OSO/T1CKI	bit0	ST	Input/output port pin or Timer1 oscillator output or Timer1 clock input
RC1/T1OSI/CCP2	bit1	ST	Input/output port pin or Timer1 oscillator input or Capture2 input/Compare2 output/PWM2 output
RC2/CCP1	bit2	ST	Input/output port pin or Capture1 input/Compare1 output/PWM1 output
RC3/SCK/SCL	bit3	ST	RC3 can also be the synchronous serial clock for both SPI and I ² C modes.
RC4/SDI/SDA	bit4	ST	RC4 can also be the SPI Data In (SPI mode) or data I/O (PC mode).
RC5/SDO	bit5	√√ ST	Input/output port pin or synchronous serial port data output
RC6/TX/CK	bit6	ST	Input/output port pin or USART Asynchronous Transmit, or USART Synchronous Clock
RC7/RX/DT	bit7	ST	Input/output port pin or USART Asynchronous Receive, or USART Synchronous Data
Legend: ST = Schmi	tt Trigg	ger input	COM. TOWN TOWN TOWN TOWN TOWN
1/1/1/	Y.C.	WTI	SISTERS ASSOCIATED WITH PORTC
IABLE 5-8: 5U	IVIIVIA	KT OF REG	ISTERS ASSOCIATED WITH PORTC

TABLE 5-8: SUMMARY OF REGISTERS ASSOCIATED WITH PORTC

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets
07h	PORTC	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	xxxx xxxx	uuuu uuuu
87h	TRISC	PORTC I	Data Direc	tion Regist	ter	-431	N.100	COM		1111 1111	1111 1111

Legend: x = unknown, u = unchanged. WWW.100Y.COM.TW

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5.4 PORTD and TRISD Register

Applicable Devices
61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

PORTD is an 8-bit port with Schmitt Trigger input buffers. Each pin is individually configurable as input or output.

PORTD can be configured as an 8-bit wide microprocessor port (parallel slave port) by setting control bit PSPMODE (TRISE<4>). In this mode, the input buffers are TTL.

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FIGURE 5-7: PORTD BLOCK DIAGRAM (IN I/O PORT MODE)

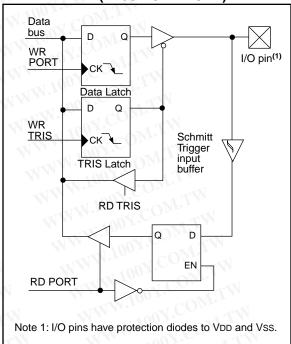


TABLE 5-9: PORTD FUNCTIONS

Name	Bit#	Buffer Type	Function
RD0/PSP0	bit0	ST/TTL ⁽¹⁾	Input/output port pin or parallel slave port bit0
RD1/PSP1	bit1	ST/TTL ⁽¹⁾	Input/output port pin or parallel slave port bit1
RD2/PSP2	bit2	ST/TTL ⁽¹⁾	Input/output port pin or parallel slave port bit2
RD3/PSP3	bit3	ST/TTL ⁽¹⁾	Input/output port pin or parallel slave port bit3
RD4/PSP4	bit4	ST/TTL ⁽¹⁾	Input/output port pin or parallel slave port bit4
RD5/PSP5	bit5	ST/TTL ⁽¹⁾	Input/output port pin or parallel slave port bit5
RD6/PSP6	bit6	ST/TTL ⁽¹⁾	Input/output port pin or parallel slave port bit6
RD7/PSP7	bit7	ST/TTL ⁽¹⁾	Input/output port pin or parallel slave port bit7

Legend: ST = Schmitt Trigger input, TTL = TTL input

Note 1: Buffer is a Schmitt Trigger when in I/O mode, and a TTL buffer when in Parallel Slave Port mode.

TABLE 5-10: SUMMARY OF REGISTERS ASSOCIATED WITH PORTD

Address	Name	Bit 7	Bit 6	Bit 5	W Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets
08h	PORTD	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	xxxx xxxx	uuuu uuuu
88h	TRISD	PORTD	Data Direc	tion Regi	ster		WW.	00-	OM	1111 1111	1111 1111
89h	TRISE	IBF	OBF	IBOV	PSPMODE	_	PORTE D	ata Directio	n Bits	0000 -111	0000 -111

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by PORTD.

5.5 PORTE and TRISE Register

Applicable Devices 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

PORTE has three pins, RE2/CS, RE1/WR, and RE0/RD which are individually configurable as inputs or outputs. These pins have Schmitt Trigger input buffers

I/O PORTE becomes control inputs for the microprocessor port when bit PSPMODE (TRISE<4>) is set. In this mode, the user must make sure that the TRISE<2:0> bits are set (pins are configured as digital inputs). In this mode the input buffers are TTL.

Figure 5-9 shows the TRISE register, which controls the parallel slave port operation and also controls the direction of the PORTE pins.

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FIGURE 5-8: PORTE BLOCK DIAGRAM (IN I/O PORT MODE)

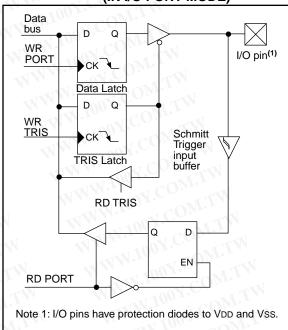


FIGURE 5-9: TRISE REGISTER (ADDRESS 89h)

R-0	R-0	R/W-0	R/W-0	U-0	R/W-1	R/W-1	R/W-1	MAN A. TOON CO.
IBF	OBF	IBOV	PSPMODE		bit2	bit1	bit0	R = Readable bit W = Writable bit
oit7							bit0	U = Unimplemented bit, read as '0'
		CO.	N					- n = Value at POR reset
bit 7 :	IBF : Input I 1 = A word 0 = No wor	has been	received and is	s waiting t	to be read by	the CPU		
			OM: 1					
bit 6:	1 = The ou	tput buffer	Full Status bit still holds a pro has been read		vritten word			
bit 5:	IBOV: Inpu	t Buffer O	verflow Detect I	bit (in mic	roprocessor i	mode)		
J. 0.	1 = A write $0 = No$ ove			isly input	word has not	been read (must be cle	eared in software)
bit 4:	0 = No ove	rflow occu : Parallel I slave por	ırred Slave Port Mod rt mode			been read (i	must be cle	eared in software)
	0 = No ove PSPMODE 1 = Paralle	rflow occu : Parallel I slave pou al purpose	urred Slave Port Mod rt mode I/O mode			been read (I	must be cle	eared in software)
bit 4:	0 = No ove PSPMODE 1 = Paralle 0 = Genera Unimplem	rflow occu : Parallel I slave pou al purpose ented: Re	urred Slave Port Mod rt mode I/O mode			been read (i	must be cle	eared in software)
bit 4:	0 = No ove PSPMODE 1 = Paralle 0 = Genera Unimplem PORTE D Bit2: Direct 1 = Input	rflow occur E: Parallel I slave por al purpose ented: Re Pata Dire tion Contr	irred Slave Port Mod rt mode I/O mode ead as '0'	le Select t		been read (i	must be cle	eared in software)
bit 4: bit 3:	0 = No ove PSPMODE 1 = Paralle 0 = Genera Unimplem PORTE D Bit2: Direct	rflow occur E: Parallel I slave por al purpose ented: Re Pata Dire tion Contr	arred Slave Port Mod rt mode I/O mode ead as '0' ction Bits	le Select t		been read (I	must be cle	eared in software)
bit 4: bit 3:	0 = No ove PSPMODE 1 = Paralle 0 = Genera Unimplem PORTE D Bit2: Direct 1 = Input 0 = Output Bit1: Direct 1 = Input	rflow occu E: Parallel I slave por al purpose ented: Re Pata Dire tion Contr	arred Slave Port Mod rt mode I/O mode ead as '0' ction Bits	le Select t		been read (I	must be cle	eared in software)
bit 4: bit 3: bit 2:	0 = No ove PSPMODE 1 = Paralle 0 = Genera Unimplem PORTE D Bit2: Direct 1 = Input 0 = Output Bit1: Direct 1 = Input 0 = Output	rflow occu E: Parallel I slave por al purpose ented: Re Pata Dire tion Contr	arred Slave Port Mod rt mode I/O mode ead as '0' ction Bits ol bit for pin RE	e Select b		been read (I	must be cle	eared in software)

TABLE 5-11: PORTE FUNCTIONS

Name	WW	Bit#	Buffer Type	Function
RE0/RD	W	bit0	ST/TTL ⁽¹⁾	Input/output port pin or Read control input in parallel slave port mode. RD 1 = Not a read operation
		WW.	100X.COM	1 = Not a read operation0 = Read operation. The system reads the PORTD register (if chip selected)
RE1/WR	sī.	bit1	ST/TTL ⁽¹⁾	Input/output port pin or Write control input in parallel slave port mode. WR 1 = Not a write operation 0 = Write operation. The system writes to the PORTD register (if chip selected)
RE2/CS	TW TW	bit2	ST/TTL ⁽¹⁾	Input/output port pin or Chip select control input in parallel slave port mode. CS 1 = Device is not selected 0 = Device is selected

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Legend: ST = Schmitt Trigger input, TTL = TTL input

Note 1: Buffer is a Schmitt Trigger when in I/O mode, and a TTL buffer when in Parallel Slave Port (PSP) mode.

SUMMARY OF REGISTERS ASSOCIATED WITH PORTE

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Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets
09h	PORTE	11-2	<u> </u>		MATION	v.€C	RE2	RE1	RE0	xxx	uuu
89h	TRISE	IBF	OBF	IBOV	PSPMODE	, <u> </u>	PORTE Da	ta Direction	Bits	0000 -111	0000 -111

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells not used by PORTE. WWW.100Y.COM.TW WWW.100Y.C

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5.6 **I/O Programming Considerations**

Applicable Devices
61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

5.6.1 BI-DIRECTIONAL I/O PORTS

Any instruction which writes, operates internally as a read followed by a write operation. The BCF and BSF instructions, for example, read the register into the CPU, execute the bit operation and write the result back to the register. Caution must be used when these instructions are applied to a port with both inputs and outputs defined. For example, a BSF operation on bit5 of PORTB will cause all eight bits of PORTB to be read into the CPU. Then the BSF operation takes place on bit5 and PORTB is written to the output latches. If another bit of PORTB is used as a bi-directional I/O pin (e.g., bit0) and it is defined as an input at this time, the input signal present on the pin itself would be read into the CPU and rewritten to the data latch of this particular pin, overwriting the previous content. As long as the pin stays in the input mode, no problem occurs. However, if bit0 is switched into output mode later on, the content of the data latch may now be unknown.

Reading the port register, reads the values of the port pins. Writing to the port register writes the value to the port latch. When using read-modify-write instructions (ex. BCF, BSF, etc.) on a port, the value of the port pins is read, the desired operation is done to this value, and this value is then written to the port latch.

Example 5-4 shows the effect of two sequential read-modify-write instructions on an I/O port.

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EXAMPLE 5-4: READ-MODIFY-WRITE INSTRUCTIONS ON AN I/O PORT

```
;Initial PORT settings: PORTB<7:4> Inputs
                        PORTB<3:0> Outputs
;PORTB<7:6> have external pull-ups and are
;not connected to other circuitry
                     PORT latch PORT pins
 BCF PORTB, 7
                     01pp pppp
                                 11pp pppp
 BCF PORTB, 6
                     10pp pppp
                                  11pp pppp
 BSF STATUS, RPO
 BCF TRISB, 7
                   ; 10pp pppp
                                 11pp pppp
 BCF TRISB, 6
                   ; 10pp pppp
                                  10pp pppp
; Note that the user may have expected the
;pin values to be 00pp pppp. The 2nd BCF
; caused RB7 to be latched as the pin value
```

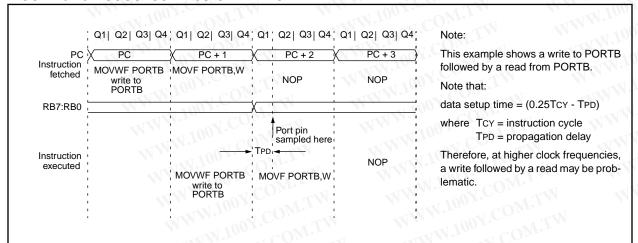
A pin actively outputting a Low or High should not be driven from external devices at the same time in order to change the level on this pin ("wired-or", "wired-and"). The resulting high output currents may damage the chip.

; (high).

5.6.2 SUCCESSIVE OPERATIONS ON I/O PORTS

The actual write to an I/O port happens at the end of an instruction cycle, whereas for reading, the data must be valid at the beginning of the instruction cycle (Figure 5-10). Therefore, care must be exercised if a write followed by a read operation is carried out on the same I/O port. The sequence of instructions should be such to allow the pin voltage to stabilize (load dependent) before the next instruction which causes that file to be read into the CPU is executed. Otherwise, the previous state of that pin may be read into the CPU rather than the new state. When in doubt, it is better to separate these instructions with a NOP or another instruction not accessing this I/O port.





5.7 Parallel Slave Port

Applicable Devices
61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

PORTD operates as an 8-bit wide parallel slave port (microprocessor port) when control bit PSPMODE (TRISE<4>) is set. In slave mode it is asynchronously readable and writable by the external world through \overline{RD} control input (RE0/ \overline{RD}) and \overline{WR} control input pin (RE1/ \overline{WR}).

It can directly interface to an 8-bit microprocessor data bus. The external microprocessor can read or write the PORTD latch as an 8-bit latch. Setting PSPMODE enables port pin RE0/ \overline{RD} to be the \overline{RD} input, RE1/ \overline{WR} to be the \overline{WR} input and RE2/ \overline{CS} to be the \overline{CS} (chip select) input. For this functionality, the corresponding data direction bits of the TRISE register (TRISE<2:0>) must be configured as inputs (set).

There are actually two 8-bit latches, one for data-out (from the PIC16/17) and one for data input. The user writes 8-bit data to PORTD data latch and reads data from the port pin latch (note that they have the same address). In this mode, the TRISD register is ignored since the microprocessor is controlling the direction of data flow.

A write to the PSP occurs when both the $\overline{\text{CS}}$ and $\overline{\text{WR}}$ lines are first detected low. When either the $\overline{\text{CS}}$ or $\overline{\text{WR}}$ lines become high (level triggered), then the Input Buffer Full status flag bit IBF (TRISE<7>) is set on the Q4 clock cycle, following the next Q2 cycle, to signal the write is complete (Figure 5-12). The interrupt flag bit PSPIF (PIR1<7>) is also set on the same Q4 clock cycle. IBF can only be cleared by reading the PORTD input latch. The input Buffer Overflow status flag bit IBOV (TRISE<5>) is set if a second write to the Parallel Slave Port is attempted when the previous byte has not been read out of the buffer.

A read from the PSP occurs when both the $\overline{\text{CS}}$ and $\overline{\text{RD}}$ lines are first detected low. The Output Buffer Full status flag bit OBF (TRISE<6>) is cleared immediately (Figure 5-13) indicating that the PORTD latch is waiting to be read by the external bus. When either the $\overline{\text{CS}}$ or $\overline{\text{RD}}$ pin becomes high (level triggered), the interrupt flag bit PSPIF is set on the Q4 clock cycle, following the next Q2 cycle, indicating that the read is complete. OBF remains low until data is written to PORTD by the user firmware.

When not in Parallel Slave Port mode, the IBF and OBF bits are held clear. However, if flag bit IBOV was previously set, it must be cleared in firmware.

An interrupt is generated and latched into flag bit PSPIF when a read or write operation is completed. PSPIF must be cleared by the user in firmware and the interrupt can be disabled by clearing the interrupt enable bit PSPIE (PIE1<7>).

FIGURE 5-11: PORTD AND PORTE AS A PARALLEL SLAVE PORT

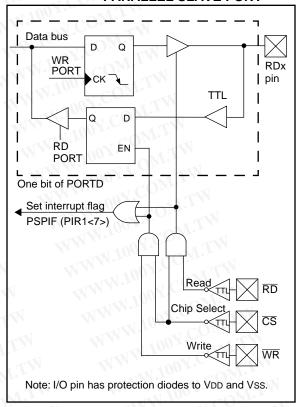


FIGURE 5-12: PARALLEL SLAVE PORT WRITE WAVEFORMS

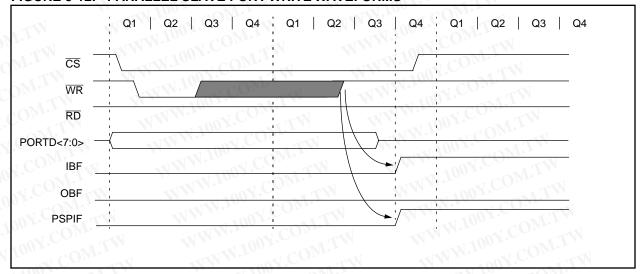


FIGURE 5-13: PARALLEL SLAVE PORT READ WAVEFORMS

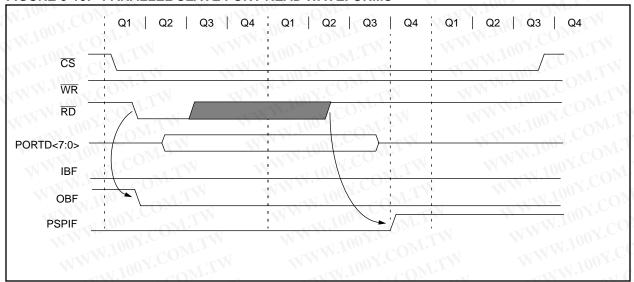


TABLE 5-13: REGISTERS ASSOCIATED WITH PARALLEL SLAVE PORT

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets
08h	PORTD	PSP7	PSP6	PSP5	PSP4	PSP3	PSP2	PSP1	PSP0	xxxx xxxx	uuuu uuuu
09h	PORTE	T	1.100	7.00	W.J.	_	RE2	RE1	RE0	xxx	uuu
89h	TRISE	IBF	OBF	IBOV	PSPMODE	_	PORTE D	ata Direction	n Bits	0000 -111	0000 -111
0Ch	PIR1	PSPIF	(1)	RCIF ⁽²⁾	TXIF ⁽²⁾	SSPIF	CCP1IF	TMR2IF	TRM1IF	0000 0000	0000 0000
8Ch	PIE1	PSPIE	(1)	RCIE ⁽²⁾	TXIE ⁽²⁾	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
										1761 6.7	

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by the PSP.

Note 1: These bits are reserved, always maintain these bits clear.

^{2:} These bits are implemented on the PIC16C65/65A/R65/67 only.

6.0 OVERVIEW OF TIMER MODULES

Applicable Devices

61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

All PIC16C6X devices have three timer modules except for the PIC16C61, which has one timer module. Each module can generate an interrupt to indicate that an event has occurred (i.e., timer overflow). Each of these modules are detailed in the following sections. The timer modules are:

- Timer0 module (Section 7.0)
- Timer1 module (Section 8.0)
- Timer2 module (Section 9.0)

6.1 Timer0 Overview

Applicable Devices

61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

The Timer0 module is a simple 8-bit overflow counter. The clock source can be either the internal system clock (Fosc/4) or an external clock. When the clock source is an external clock, the Timer0 module can be selected to increment on either the rising or falling edge.

The Timer0 module also has a programmable prescaler option. This prescaler can be assigned to either the Timer0 module or the Watchdog Timer. Bit PSA (OPTION<3>) assigns the prescaler, and bits PS2:PS0 (OPTION<2:0>) determine the prescaler value. TMR0 can increment at the following rates: 1:1 when the prescaler is assigned to Watchdog Timer, 1:2, 1:4, 1:8, 1:16, 1:32, 1:64, 1:128, and 1:256.

Synchronization of the external clock occurs after the prescaler. When the prescaler is used, the external clock frequency may be higher then the device's frequency. The maximum frequency is 50 MHz, given the high and low time requirements of the clock.

6.2 Timer1 Overview

Applicable Devices

61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

Timer1 is a 16-bit timer/counter. The clock source can be either the internal system clock (Fosc/4), an external clock, or an external crystal. Timer1 can operate as either a timer or a counter. When operating as a counter (external clock source), the counter can either operate synchronized to the device or asynchronously to the device. Asynchronous operation allows Timer1 to operate during sleep, which is useful for applications that require a real-time clock as well as the power savings of SLEEP mode.

TImer1 also has a prescaler option which allows TMR1 to increment at the following rates: 1:1, 1:2, 1:4, and 1:8. TMR1 can be used in conjunction with the Capture/Compare/PWM module. When used with a CCP module, Timer1 is the time-base for 16-bit capture or 16-bit compare and must be synchronized to the device.

6.3 Timer2 Overview

Applicable Devices

61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

Timer2 is an 8-bit timer with a programmable prescaler and a programmable postscaler, as well as an 8-bit Period Register (PR2). Timer2 can be used with the CCP module (in PWM mode) as well as the Baud Rate Generator for the Synchronous Serial Port (SSP). The prescaler option allows Timer2 to increment at the following rates: 1:1, 1:4, and 1:16.

The postscaler allows TMR2 register to match the period register (PR2) a programmable number of times before generating an interrupt. The postscaler can be programmed from 1:1 to 1:16 (inclusive).

6.4 CCP Overview

Applicable Devices

61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

The CCP module(s) can operate in one of three modes: 16-bit capture, 16-bit compare, or up to 10-bit Pulse Width Modulation (PWM).

Capture mode captures the 16-bit value of TMR1 into the CCPRxH:CCPRxL register pair. The capture event can be programmed for either the falling edge, rising edge, fourth rising edge, or sixteenth rising edge of the CCPx pin.

Compare mode compares the TMR1H:TMR1L register pair to the CCPRxH:CCPRxL register pair. When a match occurs, an interrupt can be generated and the output pin CCPx can be forced to a given state (High or Low) and Timer1 can be reset. This depends on control bits CCPxM3:CCPxM0.

PWM mode compares the TMR2 register to a 10-bit duty cycle register (CCPRxH:CCPRxL<5:4>) as well as to an 8-bit period register (PR2). When the TMR2 register = Duty Cycle register, the CCPx pin will be forced low. When TMR2 = PR2, TMR2 is cleared to 00h, an interrupt can be generated, and the CCPx pin (if an output) will be forced high.

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7.0 TIMERO MODULE

Applicable Devices

61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

The Timer0 module has the following features:

- 8-bit timer/counter register, TMR0
 - Read and write capability
 - Interrupt on overflow from FFh to 00h
- 8-bit software programmable prescaler
- Internal or external clock select
 - Edge select for external clock

Figure 7-1 is a simplified block diagram of the Timer0 module.

Timer mode is selected by clearing bit TOCS (OPTION<5>). In timer mode, the Timer0 module will increment every instruction cycle (without prescaler). If TMR0 register is written, the increment is inhibited for the following two instruction cycles (Figure 7-2 and Figure 7-3). The user can work around this by writing an adjusted value to the TMR0 register.

Counter mode is selected by setting bit T0CS. In this mode, Timer0 will increment either on every rising or falling edge of pin RA4/T0CKI. The incrementing edge is determined by the source edge select bit T0SE

(OPTION<4>). Clearing bit T0SE selects the rising edge. Restrictions on the external clock input are discussed in detail in Section 7.2.

The prescaler is mutually exclusively shared between the Timer0 module and the Watchdog Timer. The prescaler assignment is controlled in software by control bit PSA (OPTION<3>). Clearing bit PSA will assign the prescaler to the Timer0 module. The prescaler is not readable or writable. When the prescaler is assigned to the Timer0 module, prescale values of 1:2, 1:4, ..., 1:256 are selectable. Section 7.3 details the operation of the prescaler.

7.1 TMR0 Interrupt

Applicable Devices

61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

The TMR0 interrupt is generated when the register (TMR0) overflows from FFh to 00h. This overflow sets interrupt flag bit T0IF (INTCON<2>). The interrupt can be masked by clearing enable bit T0IE (INTCON<5>). Flag bit T0IF must be cleared in software by the TImer0 interrupt service routine before re-enabling this interrupt. The TMR0 interrupt cannot wake the processor from SLEEP since the timer is shut off during SLEEP. Figure 7-4 displays the Timer0 interrupt timing.

FIGURE 7-1: TIMERO BLOCK DIAGRAM

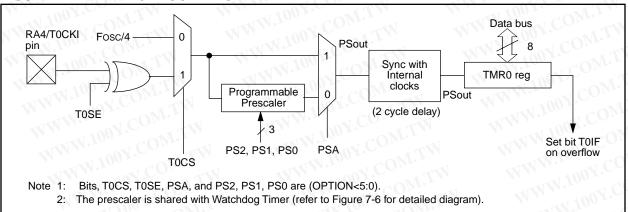


FIGURE 7-2: TIMERO TIMING: INTERNAL CLOCK/NO PRESCALER

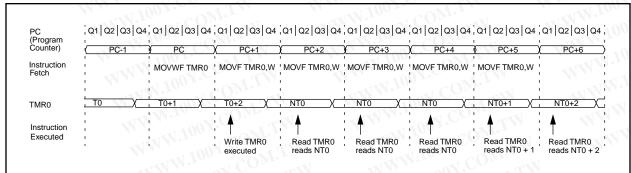
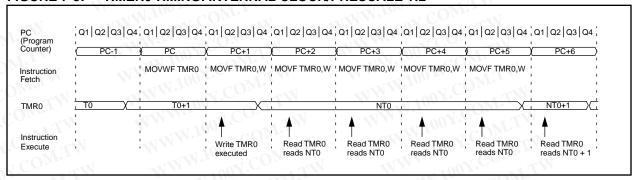
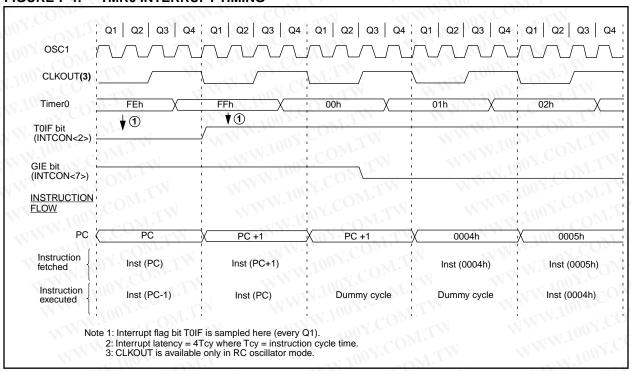


FIGURE 7-3: TIMERO TIMING: INTERNAL CLOCK/PRESCALE 1:2



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FIGURE 7-4: TMR0 INTERRUPT TIMING



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7.2 <u>Using Timer0 with External Clock</u>

Applicable Devices

61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

When an external clock input is used for Timer0, it must meet certain requirements. The requirements ensure the external clock can be synchronized with the internal phase clock (Tosc). Also, there is a delay in the actual incrementing of Timer0 after synchronization.

7.2.1 EXTERNAL CLOCK SYNCHRONIZATION

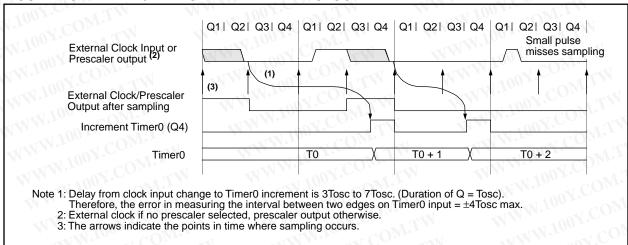
When no prescaler is used, the external clock input is the same as the prescaler output. The synchronization of T0CKI with the internal phase clocks is accomplished by sampling the prescaler output on the Q2 and Q4 cycles of the internal phase clocks (Figure 7-5). Therefore, it is necessary for T0CKI to be high for at least 2Tosc (and a small RC delay of 20 ns) and low for at least 2Tosc (and a small RC delay of 20 ns). Refer to the electrical specification of the desired device.

When a prescaler is used, the external clock input is divided by the asynchronous ripple-counter type prescaler so that the prescaler output is symmetrical. For the external clock to meet the sampling requirement, the ripple-counter must be taken into account. Therefore, it is necessary for TOCKI to have a period of at least 4Tosc (and a small RC delay of 40 ns) divided by the prescaler value. The only requirement on TOCKI high and low time is that they do not violate the minimum pulse width requirement of 10 ns. Refer to parameters 40, 41 and 42 in the electrical specification of the desired device.

7.2.2 TIMERO INCREMENT DELAY

Since the prescaler output is synchronized with the internal clocks, there is a small delay from the time the external clock edge occurs to the time the Timer0 module is actually incremented. Figure 7-5 shows the delay from the external clock edge to the timer incrementing.

FIGURE 7-5: TIMERO TIMING WITH EXTERNAL CLOCK



7.3 Prescaler

Applicable Devices 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

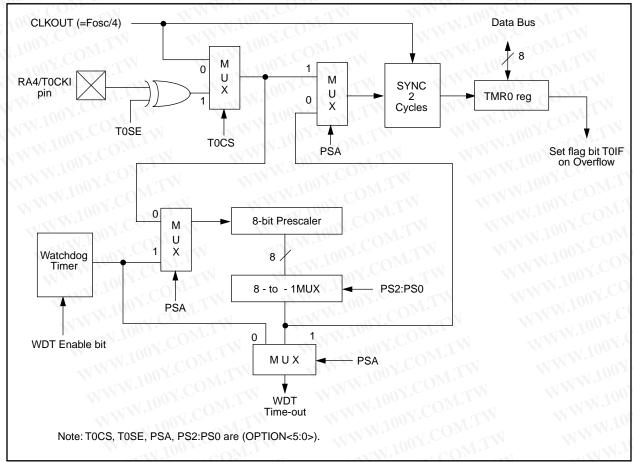
An 8-bit counter is available as a prescaler for the Timer0 module or as a postscaler for the Watchdog Timer (WDT), respectively (Figure 7-6). For simplicity, this counter is being referred to as "prescaler" throughout this data sheet. Note that the prescaler may be used by either the Timer0 module or the Watchdog Timer, but not both. Thus, a prescaler assignment for the Timer0 module means that there is no prescaler for the Watchdog Timer, and vice-versa.

The PSA and PS2:PS0 bits (OPTION<3:0>) determine the prescaler assignment and prescale ratio.

When assigned to the Timer0 module, all instructions writing to the TMR0 register (e.g. CLRF TMR0, MOVWF TMR0, BSF TMR0,bitx) will clear the prescaler count. When assigned to the Watchdog Timer, a CLRWDT instruction will clear the Watchdog Timer and the prescaler count. The prescaler is not readable or writable.

Note: Writing to TMR0 when the prescaler is assigned to Timer0 will clear the prescaler count, but will not change the prescaler assignment.

FIGURE 7-6: BLOCK DIAGRAM OF THE TIMERO/WDT PRESCALER



7.3.1 SWITCHING PRESCALER ASSIGNMENT

The prescaler assignment is fully under software control, i.e., it can be changed "on the fly" during program execution.

Note: To avoid an unintended device RESET, the following instruction sequence (shown in Example 7-1) must be executed when changing the prescaler assignment from Timer0 to the WDT. This precaution must be followed even if the WDT is disabled.

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EXAMPLE 7-1: CHANGING PRESCALER (TIMER0→WDT)

Lines 2 and 3 do NOT have to be included if the final desired prescale value is other than 1:1. If 1:1 is final desired value, then a temporary prescale value is set in lines 2 and 3 and the final prescale value will be set in lines 10 and 11.

```
1) BSF
           STATUS, RPO
                          ;Bank 1
    MOVLW
           b'xx0x0xxx'
                          ; Select clock source and prescale value of
    MOVWF
           OPTION_REG
                          ;other than 1:1
                          ;Bank 0
    BCF
           STATUS, RPO
5)
    CLRF
                          ;Clear TMR0 and prescaler
           TMRO
    BSF
           STATUS, RP1
                          ;Bank 1
6)
7)
           b'xxxx1xxx
                          ;Select WDT, do not change prescale value
    MOVLW
8)
    MOVWF
           OPTION REG
9)
    CLRWDT
                          ;Clears WDT and prescaler
10)
    MOVLW
           b'xxxx1xxx'
                          ;Select new prescale value and WDT
    MOVWF
           OPTION_REG
           STATUS, RPO
   BCF
                          ;Bank 0
```

To change prescaler from the WDT to the Timer0 module, use the sequence shown in Example 7-2.

EXAMPLE 7-2: CHANGING PRESCALER (WDT→TIMER0)

CLRWDT ;Clear WDT and prescaler

BSF STATUS, RP0 ;Bank 1

MOVLW b'xxxx0xxx';Select TMR0, new prescale value and clock source

MOVWF OPTION_REG ;

BCF STATUS, RP0 ;Bank 0

TABLE 7-1: REGISTERS ASSOCIATED WITH TIMERO

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets
01h, 101h	TMR0	Timer0	module's i	egister	V	144	1007		TW	xxxx xxxx	uuuu uuuu
0Bh,8Bh, 10Bh,18Bh	INTCON	GIE	PEIE ⁽¹⁾	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000 000x	0000 000u
81h, 181h	OPTION	RBPU	INTEDG	TOCS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
85h	TRISA		100¥.C	PORTA Data	a Direction I	Register(1)	-W10	07.0	T.Mc	11 1111	11 1111

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by Timer0.

Note 1: TRISA<5> and bit PEIE are not implemented on the PIC16C61, read as '0'.

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8.0 TIMER1 MODULE

Applicable Devices

61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

Timer1 is a 16-bit timer/counter consisting of two 8-bit registers (TMR1H and TMR1L) which are readable and writable. Register TMR1 (TMR1H:TMR1L) increments from 0000h to FFFFh and rolls over to 0000h. The TMR1 Interrupt, if enabled, is generated on overflow which is latched in interrupt flag bit TMR1IF (PIR1<0>). This interrupt can be enabled/disabled by setting/clearing the TMR1 interrupt enable bit TMR1IE (PIE1<0>).

Timer1 can operate in one of two modes:

- As a timer
- As a counter

The operating mode is determined by clock select bit, TMR1CS (T1CON<1>) (Figure 8-2).

In timer mode, Timer1 increments every instruction cycle. In counter mode, it increments on every rising edge of the external clock input.

Timer1 can be enabled/disabled by setting/clearing control bit TMR1ON (T1CON<0>).

Timer1 also has an internal "reset input". This reset can be generated by CCP1 or CCP2 (Capture/Compare/ PWM) module. See Section 10.0 for details. Figure 8-1 shows the Timer1 control register.

For the PIC16C62A/R62/63/R63/64A/R64/65A/R65/R66/67, when the Timer1 oscillator is enabled (T1OSCEN is set), the RC1 and RC0 pins become inputs. That is, the TRISC<1:0> value is ignored.

For the PIC16C62/64/65, when the Timer1 oscillator is enabled (T1OSCEN is set), RC1 pin becomes an input, however the RC0 pin will have to be configured as an input by setting the TRISC<0> bit.

The Timer1 module also has a software programmable prescaler.

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FIGURE 8-1: T1CON: TIMER1 CONTROL REGISTER (ADDRESS 10h)

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	WILLIAM COM.
$M_{\overline{M}}$.,	CV-CV	T1CKPS1	T1CKPS0	T10SCEN	T1SYNC	TMR1CS	TMR10N	R = Readable bit
oit7							bit0	W = Writable bitU = Unimplemented bit, read as '0'- n = Value at POR reset
bit 7-6:	Unimpler	nented: Rea	ad as '0'					
bit 5-4:	11 = 1:8 F 10 = 1:4 F 01 = 1:2 F	:T1CKPS0: Prescale valu Prescale valu Prescale valu Prescale valu	ue ue ue	ut Clock Pre	escale Selec	et bits		
bit 3:	1 = Oscilla 0 = Oscilla	N: Timer1 Os ator is enabl ator is shut o oscillator in	ed off			rned off to e	liminate pow	er drain.
bit 2:	T1SYNC:	Timer1 Exte	ernal Clock I	nput Synch	ronization C	Control bit		
		<u>= 1</u> t synchroniz ronize exter						
	TMR1CS This bit is	= 0 ignored. Tin	ner1 uses th	e internal c	lock when T	MR1CS = 0	100 Y.C.C	
bit 1:	1 = Exterr	Timer1 Cloonal clock from al clock (Fos	m T1OSI (or	7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7	edge) (See	pinouts for p	oin with T1OS	SI function)
bit 0:	TMR1ON	: Timer1 On	bit					

8.1 <u>Timer1 Operation in Timer Mode</u>

Applicable Devices

61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

Timer mode is selected by clearing bit TMR1CS (T1CON<1>). In this mode, the input clock to the timer is Fosc/4. The synchronize control bit T1SYNC (T1CON<2>) has no effect since the internal clock is always in sync.

8.2 <u>Timer1 Operation in Synchronized</u> Counter Mode

Applicable Devices

61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

Counter mode is selected by setting bit TMR1CS. In this mode the timer increments on every rising edge of clock input on T1OSI when enable bit T1OSCEN is set or pin with T1CKI when bit T1OSCEN is cleared.

Note:

The T1OSI function is multiplexed to different pins, depending on the device. See the pinout descriptions to see which pin has the T1OSI function.

If T1SYNC is cleared, then the external clock input is synchronized with internal phase clocks. The synchronization is done after the prescaler stage. The prescaler stage is an asynchronous ripple counter.

In this configuration, during SLEEP mode, Timer1 will not increment even if an external clock is present, since the synchronization circuit is shut off. The prescaler, however, will continue to increment.

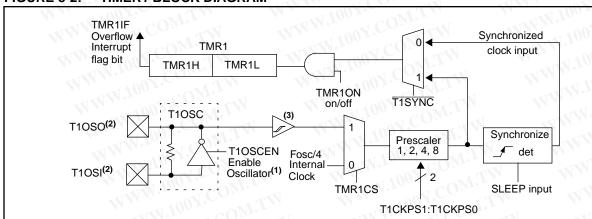
8.2.1 EXTERNAL CLOCK INPUT TIMING FOR SYNCHRONIZED COUNTER MODE

When an external clock input is used for Timer1 in synchronized counter mode, it must meet certain requirements. The external clock requirement is due to internal phase clock (Tosc) synchronization. Also, there is a delay in the actual incrementing of TMR1 after synchronization.

When the prescaler is 1:1, the external clock input is the same as the prescaler output. The synchronization of T1CKI with the internal phase clocks is accomplished by sampling the prescaler output on the Q2 and Q4 cycles of the internal phase clocks. Therefore, it is necessary for T1CKI to be high for at least 2Tosc (and a small RC delay of 20 ns) and low for at least 2Tosc (and a small RC delay of 20 ns). Refer to appropriate electrical specification section, parameters 45, 46, and 47.

When a prescaler other than 1:1 is used, the external clock input is divided by the asynchronous ripple-counter type prescaler so that the prescaler output is symmetrical. In order for the external clock to meet the sampling requirement, the ripple counter must be taken into account. Therefore, it is necessary for T1CKI to have a period of at least 4Tosc (and a small RC delay of 40 ns) divided by the prescaler value. The only requirement on T1CKI high and low time is that they do not violate the minimum pulse width requirements of 10 ns). Refer to applicable electrical specification section, parameters 40, 42, 45, 46, and 47.

FIGURE 8-2: TIMER1 BLOCK DIAGRAM



- Note 1: When enable bit T10SCEN is cleared, the inverter and feedback resistor are turned off. This eliminates power drain.
 - 2: See pinouts for pins with T1OSO and T1OSI functions.
 - 3: For the PIC16C62/64/65, the Schmitt Trigger is not implemented in external clock mode.

8.3 <u>Timer1 Operation in Asynchronous</u> **Counter Mode**

Applicable Devices

61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

If control bit T1SYNC (T1CON<2>) is set, the external clock input is not synchronized. The timer continues to increment asynchronous to the internal phase clocks. The timer will continue to run during SLEEP and generate an interrupt on overflow which will wake the processor. However, special precautions in software are needed to read-from or write-to the Timer1 register pair, TMR1L and TMR1H (Section 8.3.2).

In asynchronous counter mode, Timer1 cannot be used as a time-base for capture or compare operations.

EXTERNAL CLOCK INPUT TIMING WITH 8.3.1 UNSYNCHRONIZED CLOCK

If control bit T1SYNC is set, the timer will increment completely asynchronously. The input clock must meet certain minimum high time and low time requirements, as specified in timing parameters (45 - 47).

8.3.2 READING AND WRITING TMR1 IN ASYNCHRONOUS COUNTER MODE

Reading TMR1H or TMR1L, while the timer is running from an external asynchronous clock, will ensure a valid read (taken care of in hardware). However, the user should keep in mind that reading the 16-bit timer in two 8-bit values itself poses certain problems since the timer may overflow between the reads.

For writes, it is recommended that the user simply stop the timer and write the desired values. A write contention may occur by writing to the timer registers while the register is incrementing. This may produce an unpredictable value in the timer register.

Reading the 16-bit value requires some care. Example 8-1 is an example routine to read the 16-bit timer value. This is useful if the timer cannot be stopped.

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EXAMPLE 8-1: READING A 16-BIT FREE-RUNNING TIMER

```
All Interrupts are disabled
   MOVF
           TMR1H, W
                          ;Read high byte
   MOVWE
           тмрн
           TMR1L,
   MOVE
                          ;Read low byte
   MOVWF
           TMPL
   MOVF
           TMR1H,
                          ;Read high byte
    SUBWF
           TMPH,
                          ;Sub 1st read
                          ;with 2nd read
   BTFSC
           STATUS, Z
                          ;is result = 0
           CONTINUE
                          ;Good 16-bit read
; TMR1L may have rolled over between the read
; of the high and low bytes. Reading the high
 and low bytes now will read a good value.
           TMR1H, W
                          ;Read high byte
   MOVF
    MOVWF
           TMPH
    MOVF
           TMR1L,
                          ;Read low byte
   MOVWE
           TMPL
   Re-enable Interrupt
                        (if required)
CONTINUE
                          ;Continue with
                          ;your code
```

8.4 **Timer1 Oscillator**

Applicable Devices 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

A crystal oscillator circuit is built in-between pins T1OSI (input) and T1OSO (amplifier output). It is enabled by setting control bit T1OSCEN (T1CON<3>). The oscillator is a low power oscillator rated up to 200 kHz. It will continue to run during SLEEP. It is primarily intended for a 32 kHz crystal. Table 8-1 shows the capacitor selection for the Timer1 oscillator.

The Timer1 oscillator is identical to the LP oscillator. The user must allow a software time delay to ensure proper oscillator start-up.

CAPACITOR SELECTION TABLE 8-1: FOR THE TIMER1 **OSCILLATOR**

Osc Type	Freq	C1	C2
LP CO	32 kHz	33 pF	33 pF
	100 kHz	15 pF	15 pF
	200 kHz	15 pF	15 pF
These v	alues are for d	design guidand	e only.
Crystals Tes	sted:	1 -41	MM.Ing
32.768 kHz	Epson C-00	1R32.768K-A	± 20 PPM
100 kHz	Epson C-2 1	00.00 KC-P	± 20 PPM
200 kHz	STD XTL 20	0.000 kHz	± 20 PPM
		ce increases th	

- - Since each resonator/crystal has its own characteristics, the user should consult the resonator/crystal manufacturer for appropriate values of external components.

8.5 Resetting Timer1 using a CCP Trigger Output

Applicable Devices

61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

CCP2 is implemented on the PIC16C63/R63/65/65A/R65/66/67 only.

If CCP1 or CCP2 module is configured in Compare mode to generate a "special event trigger" (CCPxM3:CCPxM0 = 1011), this signal will reset Timer1.

Note: The "special event trigger" from the CCP1 and CCP2 modules will not set interrupt flag bit TMR1IF(PIR1<0>).

Timer1 must be configured for either timer or synchronized counter mode to take advantage of this feature. If the Timer1 is running in asynchronous counter mode, this reset operation may not work.

In the event that a write to Timer1 coincides with a special event trigger from CCP1 or CCP2, the write will take precedence.

In this mode of operation, the CCPRxH:CCPRxL registers pair effectively becomes the period register for the Timer1 module.

8.6 Resetting of TMR1 Register Pair (TMR1H:TMR1L)

Applicable Devices

61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

The TMR1H and TMR1L registers are not reset to 00h on a POR or any other reset except by the CCP1 or CCP2 special event trigger.

The T1CON register is reset to 00h on a Power-on Reset or a Brown-out Reset, which shuts off the timer and leaves a 1:1 prescaler. In all other resets, the register is unaffected.

8.7 Timer1 Prescaler

Applicable Devices 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

The prescaler counter is cleared on writes to the TMR1H or TMR1L registers.

TABLE 8-2: REGISTERS ASSOCIATED WITH TIMER1 AS A TIMER/COUNTER

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	4 011 01	e on: DR, DR	all	e on other sets
0Bh,8Bh 10Bh,18Bh	INTCON	GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000	000x	0000	000u
0Ch	PIR1	PSPIF ⁽²⁾	(3)	RCIF ⁽¹⁾	TXIF ⁽¹⁾	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000	0000	0000	0000
8Ch	PIE1	PSPIE ⁽²⁾	(3)	RCIE ⁽¹⁾	TXIE ⁽¹⁾	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000	0000	0000	0000
0Eh	TMR1L	Holding re	egister	for the Lea	st Significar	nt Byte of th	e 16-bit TN	/IR1 registe	er	xxxx	xxxx	uuuu	uuuu
0Fh	TMR1H	Holding re	egister	for the Mos	st Significan	t Byte of the	16-bit TM	IR1 registe	r	xxxx	xxxx	uuuu	uuuu
10h	T1CON	- 00	A.C.	T1CKPS1	T1CKPS0	T10SCEN	T1SYNC	TMR1CS	TMR10N	00	0000	uu	uuuu

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'. Shaded cells are not used by the Timer1 module.

- Note 1: The USART is implemented on the PIC16C63/R63/65/65A/R65/66/67 only.
 - 2: Bits PSPIE and PSPIF are reserved on the PIC16C62/62A/R62/63/R63/66, always maintain these bits clear.
 - 3: PIR1<6> and PIE1<6> are reserved, always maintain these bits clear.

9.0 TIMER2 MODULE

Applicable Devices

61|62|62A|R62|63|R63|64|64A|R64|65|65A|R65|66|67

Timer2 is an 8-bit timer with a prescaler and a postscaler. It is especially suitable as PWM time-base for PWM mode of CCP module(s). TMR2 is a readable and writable register, and is cleared on any device reset.

The input clock (FOSC/4) has a prescale option of 1:1, 1:4 or 1:16, selected by control bits T2CKPS1:T2CKPS0 (T2CON<1:0>).

The Timer2 module has an 8-bit period register, PR2. Timer2 increments from 00h until it matches PR2 and then resets to 00h on the next increment cycle. PR2 is a readable and writable register. The PR2 register is initialized to FFh upon reset.

The match output of the TMR2 register goes through a 4-bit postscaler (which gives a 1:1 to 1:16 scaling, inclusive) to generate a TMR2 interrupt (latched in flag bit TMR2IF (PIR1<1>)).

The Timer2 module can be shut off by clearing control bit TMR2ON (T2CON<2>) to minimize power consumption.

Figure 9-2 shows the Timer2 control register. T2CON is cleared upon reset which initializes Timer2 as shut off with the prescaler and postscaler at a 1:1 value.

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9.1 Timer2 Prescaler and Postscaler

Applicable Devices

61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

The prescaler and postscaler counters are cleared when any of the following occurs:

- · a write to the TMR2 register
- · a write to the T2CON register
- any device reset (POR, BOR, MCLR Reset, or WDT Reset).

TMR2 is not cleared when T2CON is written.

9.2 Output of TMR2

Applicable Devices

61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

The output of TMR2 (before the postscaler) is fed to the Synchronous Serial Port module which optionally uses it to generate shift clock.

FIGURE 9-1: TIMER2 BLOCK DIAGRAM

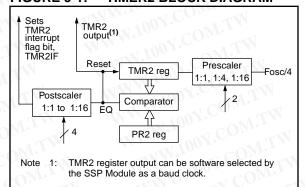


FIGURE 9-2: T2CON: TIMER2 CONTROL REGISTER (ADDRESS 12h)

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		- 100 V
it7	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	bit0	R = Readable bit W = Writable bit U = Unimplementer read as '0' - n = Value at POR r	100
oit 7:	Unimplem	ented: Rea	d as '0'						
bit 6-3:	0000 = 1:1 0001 = 1:2	postscale		put Postsca	ale Select bi	ts WW.100 WW.10			
bit 2:	TMR2ON : 1 = Timer2 0 = Timer2		oit C						
bit 1-0:	T2CKPS1: 00 = 1:1 pr 01 = 1:4 pr	escale	Timer2 Clo	ck Prescale	Select bits				

REGISTERS ASSOCIATED WITH TIMER2 AS A TIMER/COUNTER **TABLE 9-1:**

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value PO BO	R,	all c	e on other sets
0Bh,8Bh 10Bh,18Bh	INTCON	GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000	000x	0000	000u
0Ch	PIR1	PSPIF ⁽²⁾	(3)	RCIF ⁽¹⁾	TXIF ⁽¹⁾	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000	0000	0000	0000
8Ch	PIE1	PSPIE ⁽²⁾	(3)	RCIE ⁽¹⁾	TXIE(1)	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000	0000	0000	0000
11h	TMR2	Timer2 m	odule's reg	ister	Mr.		TIVIN	V	CO_{M_2}	0000	0000	0000	0000
12h	T2CON	- TOUTPS3 TOUTPS2 TOUTPS1 TOUTPS0 TMR2ON T2CKPS1 T2CK							T2CKPS0	-000	0000	-000	0000
92h	PR2	Timer2 Period register								1111	1111	1111	1111

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Note 1: The USART is implemented on the PIC16C63/R63/65/65A/R65/66/67 only.

2: Bits PSPIE and PSPIF are reserved on the PIC16C63/R63/65/65A/R65/66/67 only. Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by Timer2.

- - 2: Bits PSPIE and PSPIF are reserved on the PIC16C62/62A/R62/63/R63/66, always maintain these bits clear.
 - 3: PIR1<6> and PIE1<6> are reserved, always maintain these bits clear.

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CAPTURE/COMPARE/PWM 10.0 (CCP) MODULE(s)

Αŗ	pli	cable	e Dev	/ice	S	N.	100		al		1.1		-	
61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	CCP1
61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	CCP2

Each CCP (Capture/Compare/PWM) module contains a 16-bit register which can operate as a 16-bit capture register, as a 16-bit compare register, or as a PWM master/slave duty cycle register. Both the CCP1 and CCP2 modules are identical in operation, with the exception of the operation of the special event trigger. Table 10-1 and Table 10-2 show the resources and interactions of the CCP modules(s). In the following sections, the operation of a CCP module is described with respect to CCP1. CCP2 operates the same as CCP1, except where noted.

CCP1 module:

Capture/Compare/PWM Register1 (CCPR1) is comprised of two 8-bit registers: CCPR1L (low byte) and CCPR1H (high byte). The CCP1CON register controls the operation of CCP1. All are readable and writable.

CCP2 module:

Capture/Compare/PWM Register2 (CCPR2) is comprised of two 8-bit registers: CCPR2L (low byte) and CCPR2H (high byte). The CCP2CON register controls the operation of CCP2. All are readable and writable.

For use of the CCP modules, refer to the Embedded Control Handbook, "Using the CCP Modules" (AN594).

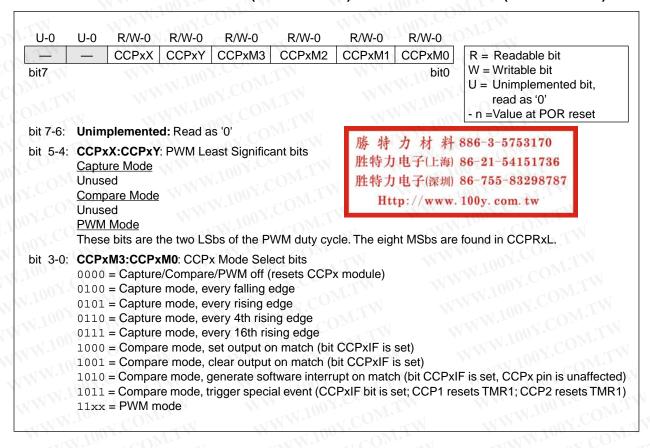
TABLE 10-1: CCP MODE - TIMER RESOURCE

	Timer Resource				
Capture	Timer1				
Compare	Timer1				
PWM	Timer2				

INTERACTION OF TWO CCP MODULES **TABLE 10-2:**

CCPx Mode	CCPy Mode	Interaction
Capture	Capture	Same TMR1 time-base.
Capture	Compare	The compare should be configured for the special event trigger, which clears TMR1.
Compare	Compare	The compare(s) should be configured for the special event trigger, which clears TMR1.
PWM	PWM	The PWMs will have the same frequency, and update rate (TMR2 interrupt).
PWM	Capture	None
PWM	Compare	None

FIGURE 10-1: CCP1CON REGISTER (ADDRESS 17h) / CCP2CON REGISTER (ADDRESS 1Dh)



10.1 Capture Mode

Applicable Devices 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

In Capture mode, CCPR1H:CCPR1L captures the 16-bit value of the TMR1 register when an event occurs on pin RC2/CCP1 (Figure 10-2). An event is defined as:

- · Every falling edge
- · Every rising edge
- · Every 4th rising edge
- · Every 16th rising edge

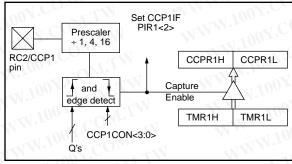
An event is selected by control bits CCP1M3:CCP1M0 (CCP1CON<3:0>). When a capture is made, the interrupt request flag bit CCP1IF (PIR1<2>) is set. It must be cleared in software. If another capture occurs before the value in register CCPR1 is read, the old captured value will be lost.

10.1.1 CCP PIN CONFIGURATION

In Capture mode, the RC2/CCP1 pin should be configured as an input by setting the TRISC<2> bit.

Note: If the RC2/CCP1 pin is configured as an output, a write to PORTC can cause a capture condition.

FIGURE 10-2: CAPTURE MODE OPERATION BLOCK DIAGRAM



10.1.2 TIMER1 MODE SELECTION

Timer1 must be running in Timer mode or Synchronized Counter mode for the CCP module to use the capture feature. In Asynchronous Counter mode, the capture operation may not work consistently.

10.1.3 SOFTWARE INTERRUPT

When the Capture event is changed, a false capture interrupt may be generated. The user should clear enable bit CCP1IE (PIE1<2>) to avoid false interrupts and should clear flag bit CCP1IF following any such change in operating mode.

10.1.4 CCP PRESCALER

There are four prescaler settings, specified by bits CCP1M3:CCP1M0. Whenever the CCP module is turned off, or the CCP module is not in Capture mode, the prescaler counter is cleared. This means that any reset will clear the prescaler counter.

Switching from one capture prescaler to another may generate an interrupt. Also, the prescaler counter will not be cleared, therefore the first capture may be from a non-zero prescaler. Example 10-1 shows the recommended method for switching between capture prescalers. This example also clears the prescaler counter and will not generate the "false" interrupt.

EXAMPLE 10-1: CHANGING BETWEEN CAPTURE PRESCALERS

CLRF CCP1CON ; Turn CCP module off
MOVLW NEW_CAPT_PS ; Load the W reg with
; the new prescaler
; mode value and CCP ON
MOVWF CCP1CON ; Load CCP1CON with
; this value

10.2 Compare Mode

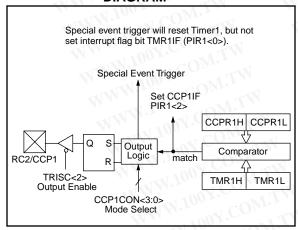
Applicable Devices 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

In Compare mode, the 16-bit CCPR1 register value is constantly compared against the TMR1 register pair value. When a match occurs, the RC2/CCP1 pin is:

- · Driven High
- Driven Low
- Remains Unchanged

The action on the pin is based on the value of control bits CCP1M3:CCP1M0 (CCP1CON<3:0>). At the same time interrupt flag bit CCP1IF is set.

FIGURE 10-3: COMPARE MODE OPERATION BLOCK DIAGRAM



10.2.1 CCP PIN CONFIGURATION

The user must configure the RC2/CCP1 pin as an output by clearing the TRISC<2> bit.

Note: Clearing the CCP1CON register will force the RC2/CCP1 compare output latch to the default low level. This is not the data latch.

10.2.1 TIMER1 MODE SELECTION

Timer1 must be running in Timer mode or Synchronized Counter mode if the CCP module is using the compare feature. In Asynchronous Counter mode, the compare operation may not work.

10.2.2 SOFTWARE INTERRUPT MODE

When Generate Software Interrupt is chosen, the CCP1 pin is not affected. Only a CCP interrupt is generated (if enabled).

10.2.3 SPECIAL EVENT TRIGGER

In this mode, an internal hardware trigger is generated which may be used to initiate an action.

The special event trigger output of CCP1 and CCP2 resets the TMR1 register pair. This allows the CCPR1H:CCPR1L and CCPR2H:CCPR2L registers to effectively be 16-bit programmable period register(s) for Timer1.

For compatibility issues, the special event trigger output of CCP1 (<u>PIC16C72</u>) and CCP2 (all other PIC16C7X devices) also starts an A/D conversion.

Note: The "special event trigger" from the CCP1 and CCP2 modules will not set interrupt flag bit TMR1IF (PIR1<0>).

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10.3 PWM Mode

Applicable Devices
61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

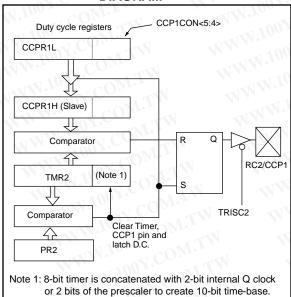
In Pulse Width Modulation (PWM) mode, the CCP1 pin produces up to a 10-bit resolution PWM output. Since the CCP1 pin is multiplexed with the PORTC data latch, the TRISC<2> bit must be cleared to make the CCP1 pin an output.

Note: Clearing the CCP1CON register will force the CCP1 PWM output latch to the default low level. This is not the PORTC I/O data latch.

Figure 10-4 shows a simplified block diagram of the CCP module in PWM mode.

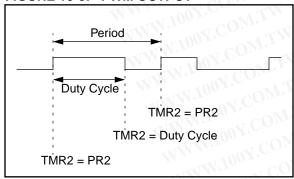
For a step by step procedure on how to set up the CCP module for PWM operation, see Section 10.3.3.

FIGURE 10-4: SIMPLIFIED PWM BLOCK DIAGRAM



A PWM output (Figure 10-5) has a time base (period) and a time that the output stays high (duty cycle). The frequency of the PWM is the inverse of the period (1/period).

FIGURE 10-5: PWM OUTPUT



10.3.1 PWM PERIOD

The PWM period is specified by writing to the PR2 register. The PWM period can be calculated using the following formula:

PWM frequency is defined as 1 / [PWM period].

When TMR2 is equal to PR2, the following three events occur on the next increment cycle:

· TMR2 is cleared

Note:

- The PWM duty cycle is latched from CCPR1L into CCPR1H
- The CCP1 pin is set (exception: if PWM duty cycle = 0%, the CCP1 pin will not be set)

The Timer2 postscaler (see Section 9.1) is not used in the determination of the PWM frequency. The postscaler could be used to have a servo update rate at a different frequency than the PWM output.

10.3.2 PWM DUTY CYCLE

The PWM duty cycle is specified by writing to the CCPR1L register and to the CCP1CON<5:4> bits. Up to 10-bit resolution is available: the CCPR1L contains the eight MSbs and the CCP1CON<5:4> contains the two LSbs. This 10-bit value is represented by CCPR1L:CCP1CON<5:4>. The following equation is used to calculate the PWM duty cycle in time:

CCPR1L and CCP1CON<5:4> can be written to at any time, but the duty cycle value is not latched into CCPR1H until after a match between PR2 and TMR2 occurs (i.e., the period is complete). In PWM mode, CCPR1H is a read-only register.

The CCPR1H register and a 2-bit internal latch are used to double buffer the PWM duty cycle. This double buffering is essential for glitchless PWM operation.

When the CCPR1H and 2-bit latch match TMR2 concatenated with an internal 2-bit Q clock or 2 bits of the TMR2 prescaler, the CCP1 pin is cleared.

Maximum PWM resolution (bits) for a given PWM frequency:

$$= \frac{\log\left(\frac{FOSC}{FPWM}\right)}{\log(2)}$$
 bits

Note: If the PWM duty cycle value is longer than the PWM period the CCP1 pin will not be forced to the low level.

EXAMPLE 10-2: PWM PERIOD AND DUTY CYCLE CALCULATION

Desired PWM frequency is 78.125 kHz, Fosc = 20 MHz TMR2 prescale = 1

 $1/78.125 \text{ kHz} = [(PR2) + 1] \cdot 4 \cdot 1/20 \text{ MHz} \cdot 1$

12.8 μ s = [(PR2) + 1] • 4 • 50 ns • 1

PR2 = 63

Find the maximum resolution of the duty cycle that can be used with a 78.125 kHz frequency and 20 MHz oscillator:

 $1/78.125 \text{ kHz} = 2^{\text{PWM RESOLUTION}} \bullet 1/20 \text{ MHz} \bullet 1$

12.8 μs = $2^{\text{PWM RESOLUTION}} \cdot 50 \text{ ns} \cdot 1$

 $256 = 2^{\text{PWM RESOLUTION}}$

 $log(256) = (PWM Resolution) \cdot log(2)$

8.0 = PWM Resolution

At most, an 8-bit resolution duty cycle can be obtained from a 78.125 kHz frequency and a 20 MHz oscillator, i.e., $0 \le CCPR1L:CCP1CON<5:4> \le 255$. Any value greater than 255 will result in a 100% duty cycle.

In order to achieve higher resolution, the PWM frequency must be decreased. In order to achieve higher PWM frequency, the resolution must be decreased.

Table 10-3 lists example PWM frequencies and resolutions for Fosc = 20 MHz. The TMR2 prescaler and PR2 values are also shown.

10.3.3 SET-UP FOR PWM OPERATION

The following steps should be taken when configuring the CCP module for PWM operation:

- Set the PWM period by writing to the PR2 register.
- Set the PWM duty cycle by writing to the CCPR1L register and CCP1CON<5:4> bits.
- Make the CCP1 pin an output by clearing the TRISC<2> bit.
- Set the TMR2 prescale value and enable Timer2 by writing to T2CON.
- 5. Configure the CCP1 module for PWM operation.

TABLE 10-3: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS AT 20 MHz

PWM Frequency	1.22 kHz	4.88 kHz	19.53 kHz	78.12 kHz	156.3 kHz	208.3 kHz
Timer Prescaler (1, 4, 16)	16	4	1	1	1001	M.1
PR2 Value	0xFF	0xFF	0xFF	0x3F	0x1F	0x17
Maximum Resolution (bits)	10	10	10	8	7 C	5.5

TABLE 10-4: REGISTERS ASSOCIATED WITH TIMER1, CAPTURE AND COMPARE

Add	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	PC	e on: DR, DR	all c	ie on other sets
0Bh,8Bh 10Bh,18Bh	INTCON	GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000	000x	0000	000u
0Ch	PIR1	PSPIF(2)	(3)	RCIF ⁽¹⁾	TXIF(1)	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000	0000	0000	0000
0Dh ⁽⁴⁾	PIR2	- - c0	$N\overline{r}_r$	- I	- W	M.F.	¹ COM	ATN .	CCP2IF	THE T	0	-05	0
8Ch	PIE1	PSPIE ⁽²⁾	(3)	RCIE ⁽¹⁾	TXIE ⁽¹⁾	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000	0000	0000	0000
8Dh ⁽⁴⁾	PIE2	no V.C	71	CW_	-W	-1 10	17:2	NEW	CCP2IE	W	0	400	0
87h	TRISC	PORTC D	ata Dire	ction regist	er 🕠	11/11/11	on V.CC		N	1111	1111	1111	1111
0Eh	TMR1L	Holding re	egister fo	r the Least	Significant	Byte of the	16-bit TMI	R1 register	KNI	xxxx	xxxx	uuuu	uuuu
0Fh	TMR1H	Holding re	egister fo	r the Most	Significant	Byte of the	16-bit TMF	R1 register	4.	xxxx	xxxx	uuuu	uuuu
10h	T1CON	- 00i	1 Co	T1CKPS1	T1CKPS0	T10SCEN	T1SYNC	TMR1CS	TMR10N	00	0000	uu	uuuu
15h	CCPR1L	Capture/C	compare	/PWM1 (LS	B)	WWW	001	COL	TW	xxxx	xxxx	uuuu	uuuu
16h	CCPR1H	Capture/C	ompare	/PWM1 (MS	SB)	-788	M.Ing.	CON	1. 2	xxxx	xxxx	uuuu	uuuu
17h	CCP1CON		007.	CCP1X	CCP1Y	CCP1M3	CCP1M2	CCP1M1	CCP1M0	00	0000	00	0000
1Bh ⁽⁴⁾	CCPR2L <	Capture/C	ompare	/PWM2 (LS	B)	WV	111	OYIC	T. T. V.	xxxx	xxxx	uuuu	uuuu
1Ch ⁽⁴⁾	CCPR2H	Capture/Compare/PWM2 (MSB)							Divi-	xxxx	xxxx	uuuu	uuuu
1Dh ⁽⁴⁾	CCP2CON	W. T.	1.100	CCP2X	CCP2Y	CCP2M3	CCP2M2	CCP2M1	CCP2M0	00	0000	00	0000

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used in these modes.

- Note 1: These bits are associated with the USART module, which is implemented on the PIC16C63/R63/65/65A/R65/66/67 only.
 - 2: Bits PSPIE and PSPIF are reserved on the PIC16C62/62A/R62/63/R66, always maintain these bits clear.
 - 3: The PIR1<6> and PIE1<6> bits are reserved, always maintain these bits clear.
 - 4: These registers are associated with the CCP2 module, which is only implemented on the PIC16C63/R63/65/65A/R65/66/67.

TABLE 10-5: REGISTERS ASSOCIATED WITH PWM AND TIMER2

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
0Bh,8Bh 10Bh,18Bh	INTCON	GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	PSPIF(2)	(3)	RCIF ⁽¹⁾	TXIF(1)	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
0Dh ⁽⁴⁾	PIR2	WW.	M . = 01	$\Gamma C \overline{O}_{M_{\pi}}$	~ \		M.A.	an LCu	CCP2IF	0	0
8Ch	PIE1	PSPIE ⁽²⁾	(3)	RCIE ⁽¹⁾	TXIE(1)	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
8Dh ⁽⁴⁾	PIE2	7/	-1XN-101	-01	V.F.	_	THE WAR	100	CCP2IE	0	0
87h	TRISC	PORTC [Data Directi	on register	TILL	1	MA	1 100 x.	JOM!	1111 1111	1111 1111
11h	TMR2	Timer2 m	odule's reg	ister	TV	V	MM	1007	Co	0000 0000	0000 0000
92h	PR2	Timer2 m	odule's Per	riod register	OMr.	N.	WW	W. P	A'COM,	1111 1111	1111 1111
12h	T2CON	_	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	-000 0000
15h	CCPR1L	Capture/0	Compare/P	WM1 (LSB)	· M	LAA		111.10	0.1.	xxxx xxxx	uuuu uuuu
16h	CCPR1H	Capture/0	Compare/P	WM1 (MSB)	TW	V	VI 1	001.	xxxx xxxx	uuuu uuuu
17h	CCP1CON	«N —	- vV	CCP1X	CCP1Y	CCP1M3	CCP1M2	CCP1M1	CCP1M0	00 0000	00 0000
1Bh ⁽⁴⁾	CCPR2L	Capture/0	Compare/P	WM2 (LSB)	-1 CO	M. I		WW	In	xxxx xxxx	uuuu uuuu
1Ch ⁽⁴⁾	CCPR2H	Capture/0	Compare/P	WM2 (MSB)03.	MITH	-	VV	1.100 x	xxxx xxxx	uuuu uuuu
1Dh ⁽⁴⁾	CCP2CON	TI	- 1	CCP2X	CCP2Y	CCP2M3	CCP2M2	CCP2M1	CCP2M0	00 0000	00 0000

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used in this mode.

Note 1: These bits are associated with the USART module, which is implemented on the PIC16C63/R63/65/65A/R65/66/67 only.

2: Bits PSPIE and PSPIF are reserved on the PIC16C62/62A/R62/63/R63/66, always maintain these bits clear.

3: The PIR1<6> and PIE1<6> bits are reserved, always maintain these bits clear.

4: These registers are associated with the CCP2 module, which is only implemented on the PIC16C63/R63/65/65A/R65/66/67.

11.0 SYNCHRONOUS SERIAL PORT (SSP) MODULE

11.1 SSP Module Overview

The Synchronous Serial Port (SSP) module is a serial interface useful for communicating with other peripheral or microcontroller devices. These peripheral devices may be Serial EEPROMs, shift registers, display drivers, A/D converters, etc. The SSP module can operate in one of two modes:

- Serial Peripheral Interface (SPI)
- Inter-Integrated Circuit (I²C)

The SSP module in I²C mode works the same in all PIC16C6X devices that have an SSP module. However the SSP Module in SPI mode has differences between the PIC16C66/67 and the other PIC16C6X devices.

The register definitions and operational description of SPI mode has been split into two sections because of the differences between the PIC16C66/67 and the other PIC16C6X devices. The default reset values of both the SPI modules is the same regardless of the device:

11.2	SPI Mode for PIC16C62/62A/R62/63/R63/6	34/
	64A/R64/65/65A/R65	84
11.3	SPI Mode for PIC16C66/67	89
11.4	I2C™ Overview	95
11.5	SSP I2C Operation	99

Refer to Application Note AN578, "Use of the SSP Module in the I²C Multi-Master Environment."

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11.2 <u>SPI Mode for PIC16C62/62A/R62/63/</u> R63/64/64A/R64/65/65A/R65

This section contains register definitions and operational characteristics of the SPI module for the PIC16C62, PIC16C62A, PIC16CR62, PIC16CR63, PIC16CR64, PIC16CR64, PIC16CR65, PIC16CR65, PIC16CR65, PIC16CR65.

FIGURE 11-1: SSPSTAT: SYNC SERIAL PORT STATUS REGISTER (ADDRESS 94h)

U-0 R-0 R-0 R-0 R-0 U-0 R-0 R-0 D/\overline{A} Р S R/W UΑ BF bit7 bit0

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

- n =Value at POR reset

- bit 7-6: Unimplemented: Read as '0'
- bit 5: **D/A**: Data/Address bit (I²C mode only)
 - 1 = Indicates that the last byte received or transmitted was data
 - 0 = Indicates that the last byte received or transmitted was address
- bit 4: P: Stop bit (I²C mode only. This bit is cleared when the SSP module is disabled, SSPEN is cleared)
 - 1 = Indicates that a stop bit has been detected last (this bit is '0' on RESET)
 - 0 = Stop bit was not detected last
- bit 3: Start bit (I²C mode only. This bit is cleared when the SSP module is disabled, SSPEN is cleared)
 - 1 = Indicates that a start bit has been detected last (this bit is '0' on RESET)
 - 0 = Start bit was not detected last
- bit 2: **R/W**: Read/Write bit information (I²C mode only)

This bit holds the R/W bit information following the last address match. This bit is valid from the address match to the next start bit, stop bit, or \overline{ACK} bit.

- 1 = Read
- 0 = Write
- bit 1: **UA**: Update Address (10-bit I²C mode only)
 - 1 = Indicates that the user needs to update the address in the SSPADD register
 - 0 = Address does not need to be updated
- bit 0: BF: Buffer Full Status bit

Receive (SPI and I²C modes)

- 1 = Receive complete, SSPBUF is full
- 0 = Receive not complete, SSPBUF is empty

<u>Transmit</u> (I²C mode only)

- 1 = Transmit in progress, SSPBUF is full
- 0 = Transmit complete, SSPBUF is empty

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FIGURE 11-2: SSPCON: SYNC SERIAL PORT CONTROL REGISTER (ADDRESS 14h)

R/W-0	. EXX							
WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	R = Readable bit
bit7	WW	400	I.Co.	TW	W	77	bit0	W = Writable bit
								U = Unimplemented bit,
								read as '0'
								- n =Value at POR reset

bit 7: WCOL: Write Collision Detect bit

1 = The SSPBUF register is written while it is still transmitting the previous word (must be cleared in software)

0 = No collision

bit 6: SSPOV: Receive Overflow Detect bit

In SPI mode

1 = A new byte is received while the SSPBUF register is still holding the previous data. In case of overflow, the data in SSPSR register is lost. Overflow can only occur in slave mode. The user must read the SSPBUF, even if only transmitting data, to avoid setting overflow. In master mode the overflow bit is not set since each new reception (and transmission) is initiated by writing to the SSPBUF register.

0 = No overflow

In I²C mode

1 = A byte is received while the SSPBUF register is still holding the previous byte. SSPOV is a "don't care" in transmit mode. SSPOV must be cleared in software in either mode.

0 = No overflow

bit 5: SSPEN: Synchronous Serial Port Enable bit

In SPI mode

1 = Enables serial port and configures SCK, SDO, and SDI as serial port pins

0 = Disables serial port and configures these pins as I/O port pins

In I²C mode

1 = Enables the serial port and configures the SDA and SCL pins as serial port pins

0 = Disables serial port and configures these pins as I/O port pins

In both modes, when enabled, these pins must be properly configured as input or output.

bit 4: CKP: Clock Polarity Select bit

In SPI mode

1 = Idle state for clock is a high level. Transmit happens on falling edge, receive on rising edge.

0 = Idle state for clock is a low level. Transmit happens on rising edge, receive on falling edge.

In I²C mode

SCK release control

- 1 = Enable clock
- 0 = Holds clock low (clock stretch) (Used to ensure data setup time)

bit 3-0: SSPM3:SSPM0: Synchronous Serial Port Mode Select bits

0000 = SPI master mode, clock = Fosc/4

0001 = SPI master mode, clock = Fosc/16

0010 = SPI master mode, clock = Fosc/64

0011 = SPI master mode, clock = TMR2 output/2

0100 = SPI slave mode, clock = SCK pin. SS pin control enabled.

0101 = SPI slave mode, clock = SCK pin. \overline{SS} pin control disabled. \overline{SS} can be used as I/O pin.

 $0110 = I^2C$ slave mode, 7-bit address

 $0111 = I^2C$ slave mode, 10-bit address

 $1011 = I^2C$ firmware controlled Master Mode (slave idle)

 $1110 = I^2C$ slave mode, 7-bit address with start and stop bit interrupts enabled

 $1111 = I^2C$ slave mode, 10-bit address with start and stop bit interrupts enabled

11.2.1 OPERATION OF SSP MODULE IN SPI MODE

Applicable Devices 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

The SPI mode allows 8-bits of data to be synchronously transmitted and received simultaneously. To accomplish communication, typically three pins are used:

- Serial Data Out (SDO)
- · Serial Data In (SDI)
- · Serial Clock (SCK)

Additionally a fourth pin may be used when in a slave mode of operation:

Slave Select (SS)

When initializing the SPI, several options need to be specified. This is done by programming the appropriate control bits in the SSPCON register (SSPCON<5:0>). These control bits allow the following to be specified:

- · Master Mode (SCK is the clock output)
- Slave Mode (SCK is the clock input)
- Clock Polarity (Output/Input data on the Rising/ Falling edge of SCK)
- · Clock Rate (Master mode only)
- Slave Select Mode (Slave mode only)

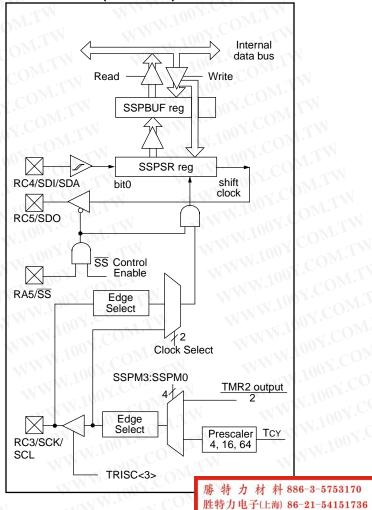
The SSP consists of a transmit/receive Shift Register (SSPSR) and a Buffer register (SSPBUF). The SSPSR shifts the data in and out of the device, MSb first. The SSPBUF holds the data that was written to the SSPSR, until the received data is ready. Once the 8-bits of data have been received, that byte is moved to the SSPBUF register. Then the Buffer Full bit, BF (SSPSTAT<0>) and flag bit SSPIF are set. This double buffering of the received data (SSPBUF) allows the next byte to start reception before reading the data that was just received. Any write to the SSPBUF register during transmission/reception of data will be ignored, and the write collision detect bit, WCOL (SSPCON<7>) will be set. User software must clear bit WCOL so that it can be determined if the following write(s) to the SSPBUF completed successfully. When the application software is expecting to receive valid data, the SSPBUF register should be read before the next byte of data to transfer is written to the SSPBUF register. The Buffer Full bit BF (SSPSTAT<0>) indicates when the SSPBUF register has been loaded with the received data (transmission is complete). When the SSPBUF is read, bit BF is cleared. This data may be irrelevant if the SPI is only a transmitter. Generally the SSP Interrupt is used to determine when the transmission/reception has completed. The SSPBUF register must be read and/or written. If the interrupt method is not going to be used, then software polling can be done to ensure that a write collision does not occur. Example 11-1 shows the loading of the SSPBUF (SSPSR) register for data transmission. The shaded instruction is only required if the received data is meaningful.

EXAMPLE 11-1: LOADING THE SSPBUF (SSPSR) REGISTER

		ama ma	550	
	BSF	STATUS,	RPU	Specify Bank 1
LOOP	BTFSS	SSPSTAT	, BF	;Has data been
				received
				;(transmit
				<pre>;complete)?</pre>
	GOTO	LOOP		;No
	BCF	STATUS,	RP0	;Specify Bank 0
	MOVF	SSPBUF,	W	;W reg = contents
				;of SSPBUF
	MOVWF	RXDATA		;Save in user RAM
	MOVF	TXDATA,	W	;W reg = contents
				; of TXDATA
	MOVWF	SSPBUF		;New data to xmit

The block diagram of the SSP module, when in SPI mode (Figure 11-3), shows that the SSPSR register is not directly readable or writable, and can only be accessed from addressing the SSPBUF register. Additionally, the SSP status register (SSPSTAT) indicates the various status conditions.

FIGURE 11-3: SSP BLOCK DIAGRAM (SPI MODE)



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To enable the serial port, SSP enable bit SSPEN (SSPCON<5>) must be set. To reset or reconfigure SPI mode, clear enable bit SSPEN, re-initialize SSPCON register, and then set enable bit SSPEN. This configures the SDI, SDO, SCK, and \overline{SS} pins as serial port pins. For the pins to behave as the serial port function, they must have their data direction bits (in the TRIS register) appropriately programmed. That is:

- SDI must have TRISC<4> set
- SDO must have TRISC<5> cleared
- SCK (Master mode) must have TRISC<3> cleared
- SCK (Slave mode) must have TRISC<3> set
- SS must have TRISA<5> set (if implemented)

Any serial port function that is not desired may be overridden by programming the corresponding data direction (TRIS) register to the opposite value. An example would be in master mode where you are only sending data (to a display driver), then both SDI and \overline{SS} could be used as general purpose outputs by clearing their corresponding TRIS register bits.

Figure 11-4 shows a typical connection between two microcontrollers. The master controller (Processor 1) initiates the data transfer by sending the SCK signal. Data is shifted out of both shift registers on their programmed clock edge, and latched on the opposite edge of the clock. Both processors should be programmed to the same Clock Polarity (CKP), then both controllers would send and receive data at the same time. Whether the data is meaningful (or dummy data) depends on the application software. This leads to three scenarios for data transmission:

- Master sends data Slave sends dummy data
- Master sends data Slave sends data
- Master sends dummy data Slave sends data

The master can initiate the data transfer at any time because it controls the SCK. The master determines when the slave (Processor 2) is to broadcast data by the software protocol.

In master mode the data is transmitted/received as soon as the SSPBUF register is written to. If the SPI is only going to receive, the SCK output could be disabled (programmed as an input). The SSPSR register will continue to shift in the signal present on the SDI pin at the programmed clock rate. As each byte is received, it will be loaded into the SSPBUF register as if a normal received byte (interrupts and status bits appropriately set). This could be useful in receiver applications as a "line activity monitor" mode.

In slave mode, the data is transmitted and received as the external clock pulses appear on SCK. When the last bit is latched interrupt flag bit SSPIF (PIR1<3>) is set.

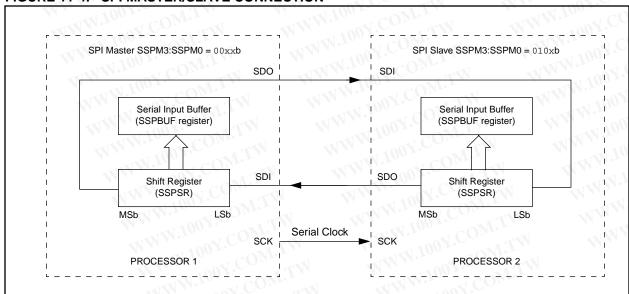
The clock polarity is selected by appropriately programming bit CKP (SSPCON<4>). This then would give waveforms for SPI communication as shown in Figure 11-5 and Figure 11-6 where the MSB is transmitted first. In master mode, the SPI clock rate (bit rate) is user programmable to be one of the following:

- Fosc/4 (or Tcy)
- Fosc/16 (or 4 Tcy)
- Fosc/64 (or 16 Tcy)
- Timer2 output/2

This allows a maximum bit clock frequency (at 20 MHz) of 5 MHz. When in slave mode the external clock must meet the minimum high and low times.

In sleep mode, the slave can transmit and receive data and wake the device from sleep.

FIGURE 11-4: SPI MASTER/SLAVE CONNECTION



The \overline{SS} pin allows a synchronous slave mode. The SPI must be in slave mode (SSPCON<3:0> = 04h) and the TRISA<5> bit must be set the for synchronous slave mode to be enabled. When the \overline{SS} pin is low, transmission and reception are enabled and the SDO pin is driven. When the \overline{SS} pin goes high, the SDO pin is no longer driven, even if in the middle of a transmitted byte, and becomes a floating output. If the \overline{SS} pin is taken low without resetting SPI mode, the transmission will continue from the

point at which it was taken high. External pull-up/pull-down resistors may be desirable, depending on the application.

To emulate two-wire communication, the SDO pin can be connected to the SDI pin. When the SPI needs to operate as a receiver the SDO pin can be configured as an input. This disables transmissions from the SDO. The SDI can always be left as an input (SDI function) since it cannot create a bus conflict.

FIGURE 11-5: SPI MODE TIMING, MASTER MODE OR SLAVE MODE W/O SS CONTROL

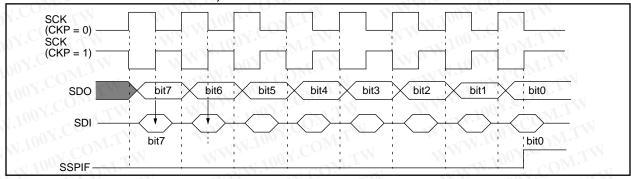


FIGURE 11-6: SPI MODE TIMING, SLAVE MODE WITH SS CONTROL

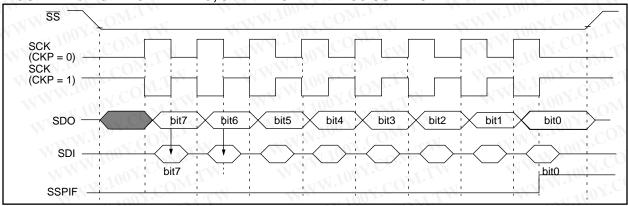


TABLE 11-1: REGISTERS ASSOCIATED WITH SPI OPERATION

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
0Bh,8Bh	INTCON	GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	PSPIF ⁽²⁾	(3)	RCIF ⁽¹⁾	TXIF ⁽¹⁾	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
8Ch	PIE1	PSPIE ⁽²⁾	(3)	RCIE ⁽¹⁾	TXIE ⁽¹⁾	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
13h	SSPBUF	Synchrono	us Serial	Port Rece	ive Buffer	/Transmit	Register	100 r.	OM	xxxx xxxx	uuuu uuuu
14h	SSPCON	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000	0000 0000
85h	TRISA		N.To.	PORTA Da	ta Direction	n Register	WWW		COM,	11 1111	11 1111
87h	TRISC	PORTC D	ata Direct	ion Regist	er	. T	-111	W.100	ALCON	1111 1111	1111 1111
94h	SSPSTAT	Zi,	±10	D/Ā	Р	S	R/W	UA	BF	00 0000	00 0000

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by SSP module in SPI mode.

- Note 1: These bits are associated with the USART which is implemented on the PIC16C63/R63/65/65A/R65 only.
 - 2: PSPIF and PSPIE are reserved on the PIC16C62/62A/R62/63/R63, always maintain these bits clear.
 - 3: PIR1<6> and PIE1<6> are reserved, always maintain these bits clear.

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11.3 SPI Mode for PIC16C66/67

This section contains register definitions and operational characterisitics of the SPI module on the PIC16C66 and PIC16C67 only.

FIGURE 11-7: SSPSTAT: SYNC SERIAL PORT STATUS REGISTER (ADDRESS 94h)(PIC16C66/67)

R/W-0 R/W-0	R-0	R-0	R-0	R-0	R-0	R-0	.ov.TV
SMP CKE	D/Ā	Р	S	R/W	UA	BF	R = Readable bit
bit7						bit0	W = Writable bit U = Unimplemented bit, read as '0' - n = Value at POR reset

bit 7: SMP: SPI data input sample phase

SPI Master Mode

1 = Input data sampled at end of data output time

0 = Input data sampled at middle of data output time

SPI Slave Mode

SMP must be cleared when SPI is used in slave mode

bit 6: CKE: SPI Clock Edge Select (Figure 11-11, Figure 11-12, and Figure 11-13)

CKP = 0

1 = Data transmitted on rising edge of SCK

0 = Data transmitted on falling edge of SCK

CKP = 1

1 = Data transmitted on falling edge of SCK

0 = Data transmitted on rising edge of SCK

bit 5: **D/A**: Data/Address bit (I²C mode only)

1 = Indicates that the last byte received or transmitted was data

0 = Indicates that the last byte received or transmitted was address

bit 4: **P**: Stop bit (I²C mode only. This bit is cleared when the SSP module is disabled, or when the Start bit is detected last, SSPEN is cleared)

1 = Indicates that a stop bit has been detected last (this bit is '0' on RESET)

0 = Stop bit was not detected last

bit 3: **S**: Start bit (I²C mode only. This bit is cleared when the SSP module is disabled, or when the Stop bit is detected last, SSPEN is cleared)

1 = Indicates that a start bit has been detected last (this bit is '0' on RESET)

0 = Start bit was not detected last

bit 2: $\mathbf{R}/\overline{\mathbf{W}}$: Read/Write bit information (I^2 C mode only)

This bit holds the R/W bit information following the last address match. This bit is only valid from the address match to the next start bit, stop bit, or ACK bit.

1 = Read

0 = Write

bit 1: **UA**: Update Address (10-bit I²C mode only)

1 = Indicates that the user needs to update the address in the SSPADD register

0 = Address does not need to be updated

bit 0: **BF**: Buffer Full Status bit

Receive (SPI and I²C modes)

1 = Receive complete, SSPBUF is full

0 = Receive not complete, SSPBUF is empty

Transmit (I²C mode only)

1 = Transmit in progress, SSPBUF is full

0 = Transmit complete, SSPBUF is empty

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FIGURE 11-8: SSPCON: SYNC SERIAL PORT CONTROL REGISTER (ADDRESS 14h)(PIC16C66/67)

R/W-0 R/W-0 **R/W-0** R/W-0 R/W-0 R/W-0 R/W-0 R/W-0 WCOL SSPOV SSPEN **CKP** SSPM3 SSPM2 SSPM1 SSPM0 bit7

R = Readable bit

W = Writable bit U = Unimplemented bit,

read as '0'

n =Value at POR reset

bit 7: WCOL: Write Collision Detect bit

1 = The SSPBUF register is written while it is still transmitting the previous word (must be cleared in software)

0 = No collision

bit 6: SSPOV: Receive Overflow Indicator bit

In SPI mode

1 = A new byte is received while the SSPBUF register is still holding the previous data. In case of overflow, the data in SSPSR is lost. Overflow can only occur in slave mode. The user must read the SSPBUF, even if only transmitting data, to avoid setting overflow. In master mode the overflow bit is not set since each new reception (and transmission) is initiated by writing to the SSPBUF register.

0 = No overflow

In I²C mode

1 = A byte is received while the SSPBUF register is still holding the previous byte. SSPOV is a "don't care" in transmit mode. SSPOV must be cleared in software in either mode.

0 = No overflow

bit 5: SSPEN: Synchronous Serial Port Enable bit

In SPI mode

1 = Enables serial port and configures SCK, SDO, and SDI as serial port pins

0 = Disables serial port and configures these pins as I/O port pins

In I²C mode

1 = Enables the serial port and configures the SDA and SCL pins as serial port pins

0 = Disables serial port and configures these pins as I/O port pins

In both modes, when enabled, these pins must be properly configured as input or output.

bit 4: CKP: Clock Polarity Select bit

In SPI mode

1 = Idle state for clock is a high level

0 = Idle state for clock is a low level

In I²C mode

SCK release control

1 = Enable clock

0 = Holds clock low (clock stretch) (Used to ensure data setup time)

bit 3-0: SSPM3:SSPM0: Synchronous Serial Port Mode Select bits

0000 = SPI master mode, clock = Fosc/4

0001 = SPI master mode, clock = Fosc/16

0010 = SPI master mode, clock = Fosc/64

0011 = SPI master mode, clock = TMR2 output/2

0100 = SPI slave mode, clock = SCK pin. SS pin control enabled.

0101 = SPI slave mode, clock = SCK pin. SS pin control disabled. SS can be used as I/O pin

 $0110 = I^2C$ slave mode, 7-bit address

 $0111 = I^2C$ slave mode, 10-bit address

 $1011 = I^2C$ firmware controlled master mode (slave idle)

 $1110 = I^2C$ slave mode, 7-bit address with start and stop bit interrupts enabled

 $1111 = I^2C$ slave mode, 10-bit address with start and stop bit interrupts enabled

11.3.1 SSP MODULE IN SPI MODE FOR PIC16C66/67

The SPI mode allows 8-bits of data to be synchronously transmitted and received simultaneously. To accomplish communication, typically three pins are used:

- Serial Data Out (SDO) RC5/SDO
- Serial Data In (SDI) RC4/SDI/SDA
- Serial Clock (SCK) RC3/SCK/SCL

Additionally a fourth pin may be used when in a slave mode of operation:

Slave Select (SS) RA5/SS

When initializing the SPI, several options need to be specified. This is done by programming the appropriate control bits in the SSPCON register (SSPCON<5:0>) and SSPSTAT<7:6>. These control bits allow the following to be specified:

- Master Mode (SCK is the clock output)
- Slave Mode (SCK is the clock input)
- · Clock Polarity (Idle state of SCK)
- Clock edge (output data on rising/falling edge of SCK)
- Clock Rate (Master mode only)
- · Slave Select Mode (Slave mode only)

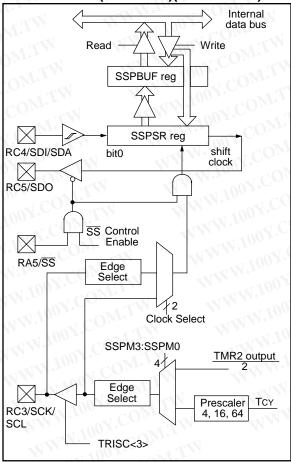
The SSP consists of a transmit/receive Shift Register (SSPSR) and a buffer register (SSPBUF). The SSPSR shifts the data in and out of the device, MSb first. The SSPBUF holds the data that was written to the SSPSR until the received data is ready. Once the 8-bits of data have been received, that byte is moved to the SSPBUF register. Then the buffer full detect bit BF (SSPSTAT<0>) and interrupt flag bit SSPIF (PIR1<3>) are set. This double buffering of the received data (SSPBUF) allows the next byte to start reception before reading the data that was just received. Any write to the SSPBUF register during transmission/reception of data will be ignored, and the write collision detect bit WCOL (SSPCON<7>) will be set. User software must clear the WCOL bit so that it can be determined if the following write(s) to the SSPBUF register completed successfully. When the application software is expecting to receive valid data, the SSPBUF should be read before the next byte of data to transfer is written to the SSPBUF. Buffer full bit BF (SSPSTAT<0>) indicates when SSPBUF has been loaded with the received data (transmission is complete). When the SSPBUF is read, bit BF is cleared. This data may be irrelevant if the SPI is only a transmitter. Generally the SSP Interrupt is used to determine when the transmission/reception has completed. The SSPBUF must be read and/or written. If the interrupt method is not going to be used, then software polling can be done to ensure that a write collision does not occur. Example 11-2 shows the loading of the SSPBUF (SSPSR) for data transmission. The shaded instruction is only required if the received data is meaningful.

EXAMPLE 11-2: LOADING THE SSPBUF (SSPSR) REGISTER (PIC16C66/67)

	BCF	STATUS,	RP1	;Specify Bank 1
	BSF	STATUS,	RP0	;
LOOP	BTFSS	SSPSTAT,	BF	;Has data been
				;received
				;(transmit
				;complete)?
	GOTO	LOOP		; No
	BCF	STATUS,	RP0	;Specify Bank 0
	MOVF	SSPBUF,	W	;W reg = contents
				; of SSPBUF
	MOVWF	RXDATA		;Save in user RAM
	MOVF	TXDATA,	W	;W reg = contents
				; of TXDATA
	MOVWF	SSPBUF		;New data to xmit

The block diagram of the SSP module, when in SPI mode (Figure 11-9), shows that the SSPSR is not directly readable or writable, and can only be accessed from addressing the SSPBUF register. Additionally, the SSP status register (SSPSTAT) indicates the various status conditions.

FIGURE 11-9: SSP BLOCK DIAGRAM (SPI MODE)(PIC16C66/67)



To enable the serial port, SSP Enable bit, SSPEN (SSPCON<5>) must be set. To reset or reconfigure SPI mode, clear bit SSPEN, re-initialize the SSPCON register, and then set bit SSPEN. This configures the SDI, SDO, SCK, and \overline{SS} pins as serial port pins. For the pins to behave as the serial port function, they must have their data direction bits (in the TRISC register) appropriately programmed. That is:

- SDI must have TRISC<4> set
- SDO must have TRISC<5> cleared
- SCK (Master mode) must have TRISC<3> cleared
- SCK (Slave mode) must have TRISC<3> set
- SS must have TRISA<5> set

Any serial port function that is not desired may be overridden by programming the corresponding data direction (TRIS) register to the opposite value. An example would be in master mode where you are only sending data (to a display driver), then both SDI and \overline{SS} could be used as general purpose outputs by clearing their corresponding TRIS register bits.

Figure 11-10 shows a typical connection between two microcontrollers. The master controller (Processor 1) initiates the data transfer by sending the SCK signal. Data is shifted out of both shift registers on their programmed clock edge, and latched on the opposite edge of the clock. Both processors should be programmed to same Clock Polarity (CKP), then both controllers would send and receive data at the same time. Whether the data is meaningful (or dummy data) depends on the application firmware. This leads to three scenarios for data transmission:

- Master sends data Slave sends dummy data
- · Master sends data Slave sends data
- · Master sends dummy data Slave sends data

The master can initiate the data transfer at any time because it controls the SCK. The master determines when the slave (Processor 2) is to broadcast data by the firmware protocol.

In master mode the data is transmitted/received as soon as the SSPBUF register is written to. If the SPI is only going to receive, the SCK output could be disabled (programmed as an input). The SSPSR register will continue to shift in the signal present on the SDI pin at the programmed clock rate. As each byte is received, it will be loaded into the SSPBUF register as if a normal received byte (interrupts and status bits appropriately set). This could be useful in receiver applications as a "line activity monitor" mode.

In slave mode, the data is transmitted and received as the external clock pulses appear on SCK. When the last bit is latched the interrupt flag bit SSPIF (PIR1<3>) is set.

The clock polarity is selected by appropriately programming bit CKP (SSPCON<4>). This then would give waveforms for SPI communication as shown in Figure 11-11, Figure 11-12, and Figure 11-13 where the MSB is transmitted first. In master mode, the SPI clock rate (bit rate) is user programmable to be one of the following:

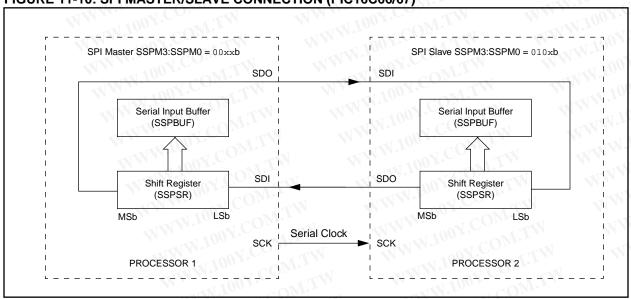
- Fosc/4 (or Tcy)
- Fosc/16 (or 4 Tcy)
- Fosc/64 (or 16 Tcy)
- · Timer2 output/2

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This allows a maximum bit clock frequency (at 20 MHz) of 5 MHz. When in slave mode the external clock must meet the minimum high and low times.

In sleep mode, the slave can transmit and receive data and wake the device from sleep.

FIGURE 11-10: SPI MASTER/SLAVE CONNECTION (PIC16C66/67)



The \overline{SS} pin allows a synchronous slave mode. The SPI must be in slave mode (SSPCON<3:0> = 04h) and the TRISA<5> bit must be set for the synchronous slave mode to be enabled. When the \overline{SS} pin is low, transmission and reception are enabled and the SDO pin is driven. When the \overline{SS} pin goes high, the SDO pin is no longer driven, even if in the middle of a transmitted byte, and becomes a floating output. If the \overline{SS} pin is taken low without resetting SPI mode, the transmission will continue from the point at which it was taken high. External pull-up/ pull-down resistors may be desirable, depending on the application.

Note: When the SPI is in Slave Mode with \overline{SS} pin control enabled, (SSPCON<3:0> = 0100) the SPI module will reset if the \overline{SS} pin is set to VDD.

Note: If the SPI is used in Slave Mode with CKE = '1', then the \overline{SS} pin control must be enabled.

To emulate two-wire communication, the SDO pin can be connected to the SDI pin. When the SPI needs to operate as a receiver the SDO pin can be configured as an input. This disables transmissions from the SDO. The SDI can always be left as an input (SDI function) since it cannot create a bus conflict.

FIGURE 11-11: SPI MODE TIMING, MASTER MODE (PIC16C66/67)

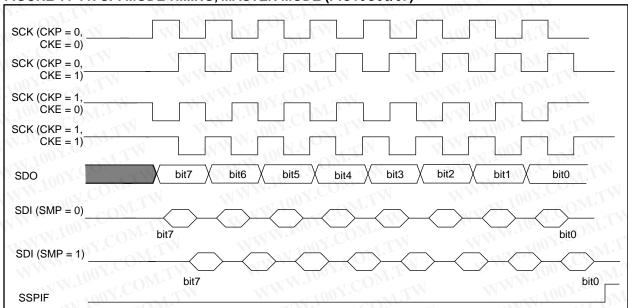


FIGURE 11-12: SPI MODE TIMING (SLAVE MODE WITH CKE = 0) (PIC16C66/67)

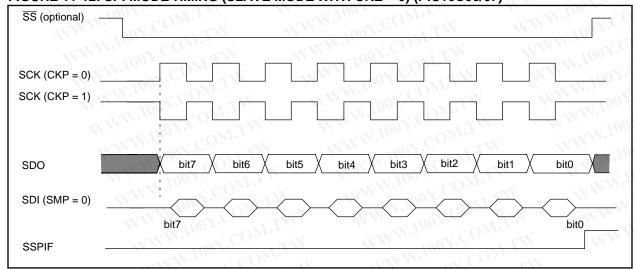


FIGURE 11-13: SPI MODE TIMING (SLAVE MODE WITH CKE = 1) (PIC16C66/67)

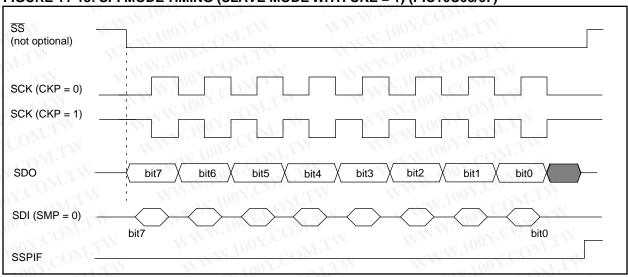


TABLE 11-2: REGISTERS ASSOCIATED WITH SPI OPERATION (PIC16C66/67)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value Powe Res	er-on	Value on all other resets
0Bh,8Bh, 10Bh,18Bh	INTCON	GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000	000x	0000 000u
0Ch	PIR1	PSPIF ⁽¹⁾	(2)	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000	0000	0000 0000
8Ch	PIE1	PSPIE ⁽¹⁾	(2)	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000	0000	0000 0000
13h	SSPBUF	Synchron	ous Seria	Port Rece	eive Buffe	er/Transmi	t Register	-31		xxxx	xxxx	uuuu uuuu
14h	SSPCON	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000	0000	0000 0000
85h	TRISA	I.Co		PORTA D	ata Direc	ction regis	ter	LIW		11	1111	11 1111
87h	TRISC	PORTC D	ata Direc	tion registe	er	100	N.Co.	WILL		1111	1111	1111 1111
94h	SSPSTAT	SMP	CKE	D/A	Р	S	R/W	UA	BF	0000	0000	0000 0000
S Note 1: P	= unknown haded cells SPIF and P IR1<6> and	are not use SPIE are re	ed by SSI eserved o	P module in the PIC1	n SPI mo 6C66, al	de. ways mair	ntain these	e bits clea	LM LM	1	WW	M.100X.

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11.4 I²C™ Overview

This section provides an overview of the Inter-Integrated Circuit (I²C) bus, with Section 11.5 discussing the operation of the SSP module in I²C mode.

The I²C bus is a two-wire serial interface developed by the Philips[®] Corporation. The original specification, or standard mode, was for data transfers of up to 100 Kbps. The enhanced specification (fast mode) is also supported. This device will communicate with both standard and fast mode devices if attached to the same bus. The clock will determine the data rate.

The I²C interface employs a comprehensive protocol to ensure reliable transmission and reception of data. When transmitting data, one device is the "master" which initiates transfer on the bus and generates the clock signals to permit that transfer, while the other device(s) acts as the "slave." All portions of the slave protocol are implemented in the SSP module's hardware, except general call support, while portions of the master protocol need to be addressed in the PIC16CXX software. Table 11-3 defines some of the I²C bus terminology. For additional information on the I²C interface specification, refer to the Philips document "The I²C bus and how to use it."#939839340011, which can be obtained from the Philips Corporation.

In the I²C interface protocol each device has an address. When a master wishes to initiate a data transfer, it first transmits the address of the device that it wishes to "talk" to. All devices "listen" to see if this is their address. Within this address, a bit specifies if the master wishes to read-from/write-to the slave device. The master and slave are always in opposite modes (transmitter/receiver) of operation during a data transfer. That is they can be thought of as operating in either of these two relations:

- Master-transmitter and Slave-receiver
- · Slave-transmitter and Master-receiver

In both cases the master generates the clock signal.

The output stages of the clock (SCL) and data (SDA) lines must have an open-drain or open-collector in order to perform the wired-AND function of the bus. External pull-up resistors are used to ensure a high level when no device is pulling the line down. The number of devices that may be attached to the I²C bus is limited only by the maximum bus loading specification of 400 pF.

11.4.1 INITIATING AND TERMINATING DATA TRANSFER

During times of no data transfer (idle time), both the clock line (SCL) and the data line (SDA) are pulled high through the external pull-up resistors. The START and STOP conditions determine the start and stop of data transmission. The START condition is defined as a high to low transition of the SDA when the SCL is high. The STOP condition is defined as a low to high transition of the SDA when the SCL is high. Figure 11-14 shows the START and STOP conditions. The master generates these conditions for starting and terminating data transfer. Due to the definition of the START and STOP conditions, when data is being transmitted, the SDA line can only change state when the SCL line is low.

FIGURE 11-14: START AND STOP CONDITIONS

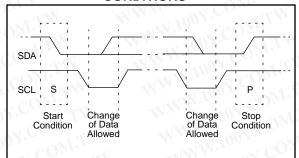


TABLE 11-3: I²C BUS TERMINOLOGY

Term	Description ON The Control of the Co
Transmitter	The device that sends the data to the bus.
Receiver	The device that receives the data from the bus.
Master	The device which initiates the transfer, generates the clock and terminates the transfer.
Slave	The device addressed by a master.
Multi-master	More than one master device in a system. These masters can attempt to control the bus at the same time without corrupting the message.
Arbitration	Procedure that ensures that only one of the master devices will control the bus. This ensure that the transfer data does not get corrupted.
Synchronization	Procedure where the clock signals of two or more devices are synchronized.

11.4.2 ADDRESSING I2C DEVICES

There are two address formats. The simplest is the 7-bit address format with a R/\overline{W} bit (Figure 11-15). The more complex is the 10-bit address with a R/\overline{W} bit (Figure 11-16). For 10-bit address format, two bytes must be transmitted with the first five bits specifying this to be a 10-bit address.

FIGURE 11-15: 7-BIT ADDRESS FORMAT

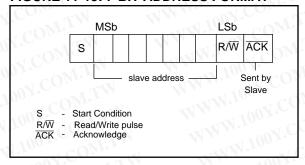
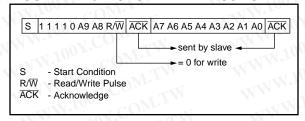


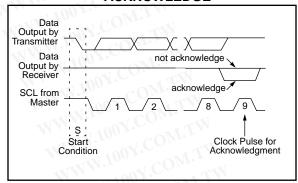
FIGURE 11-16: I²C 10-BIT ADDRESS FORMAT



11.4.3 TRANSFER ACKNOWLEDGE

All data must be transmitted per byte, with no limit to the number of bytes transmitted per data transfer. After each byte, the slave-receiver generates an acknowledge bit (ACK) (Figure 11-17). When a slave-receiver doesn't acknowledge the slave address or received data, the master must abort the transfer. The slave must leave SDA high so that the master can generate the STOP condition (Figure 11-14).

FIGURE 11-17: SLAVE-RECEIVER ACKNOWLEDGE



If the master is receiving the data (master-receiver), it generates an acknowledge signal for each received byte of data, except for the last byte. To signal the end of data to the slave-transmitter, the master does not generate an acknowledge (not acknowledge). The slave then releases the SDA line so the master can generate the STOP condition. The master can also generate the STOP condition during the acknowledge pulse for valid termination of data transfer.

If the slave needs to delay the transmission of the next byte, holding the SCL line low will force the master into a wait state. Data transfer continues when the slave releases the SCL line. This allows the slave to move the received data or fetch the data it needs to transfer before allowing the clock to start. This wait state technique can also be implemented at the bit level, Figure 11-18. The slave will inherently stretch the clock, when it is a transmitter, but will not when it is a receiver. The slave will have to clear the SSPCON<4> bit to enable clock stretching when it is a receiver.

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FIGURE 11-18: DATA TRANSFER WAIT STATE

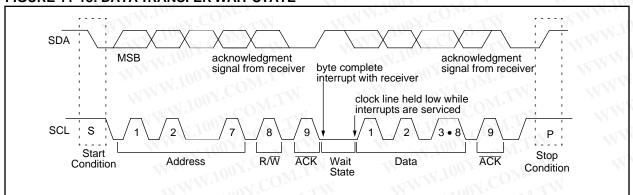


Figure 11-19 and Figure 11-20 show Master-transmitter and Master-receiver data transfer sequences.

When a master does not wish to relinquish the bus (by generating a STOP condition), a repeated START condition (Sr) must be generated. This condition is identical to the start condition (SDA goes high-to-low while

SCL is high), but occurs after a data transfer acknowledge pulse (not the bus-free state). This allows a master to send "commands" to the slave and then receive the requested information or to address a different slave device. This sequence is shown in Figure 11-21.

FIGURE 11-19: MASTER-TRANSMITTER SEQUENCE

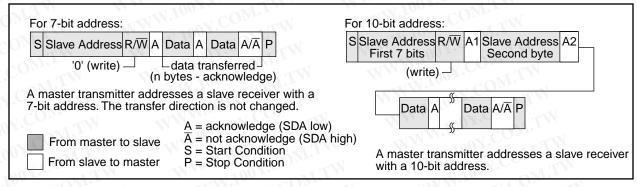
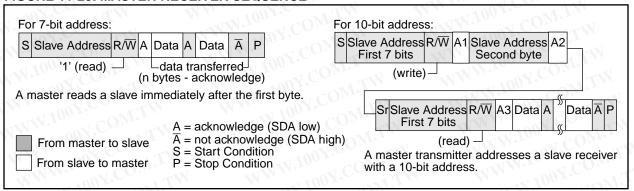
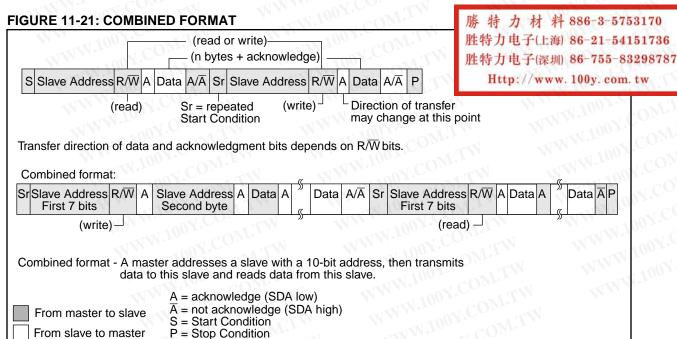


FIGURE 11-20: MASTER-RECEIVER SEQUENCE





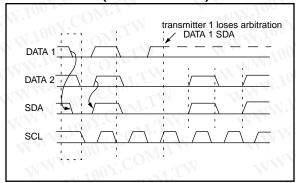
11.4.4 MULTI-MASTER

The I²C protocol allows a system to have more than one master. This is called multi-master. When two or more masters try to transfer data at the same time, arbitration and synchronization occur.

11.4.4.1 ARBITRATION

Arbitration takes place on the SDA line, while the SCL line is high. The master which transmits a high when the other master transmits a low loses arbitration (Figure 11-22), and turns off its data output stage. A master which lost arbitration can generate clock pulses until the end of the data byte where it lost arbitration. When the master devices are addressing the same device, arbitration continues into the data.

FIGURE 11-22: MULTI-MASTER ARBITRATION (TWO MASTERS)



Masters that also incorporate the slave function, and have lost arbitration must immediately switch over to slave-receiver mode. This is because the winning master-transmitter may be addressing it.

Arbitration is not allowed between:

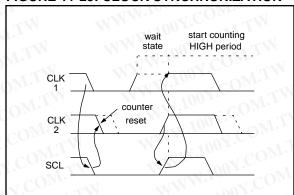
- A repeated START condition
- · A STOP condition and a data bit
- A repeated START condition and a STOP condition

Care needs to be taken to ensure that these conditions do not occur.

11.2.4.2 Clock Synchronization

Clock synchronization occurs after the devices have started arbitration. This is performed using a wired-AND connection to the SCL line. A high to low transition on the SCL line causes the concerned devices to start counting off their low period. Once a device clock has gone low, it will hold the SCL line low until its SCL high state is reached. The low to high transition of this clock may not change the state of the SCL line, if another device clock is still within its low period. The SCL line is held low by the device with the longest low period. Devices with shorter low periods enter a high waitstate, until the SCL line comes high. When the SCL line comes high, all devices start counting off their high periods. The first device to complete its high period will pull the SCL line low. The SCL line high time is determined by the device with the shortest high period, Figure 11-23.

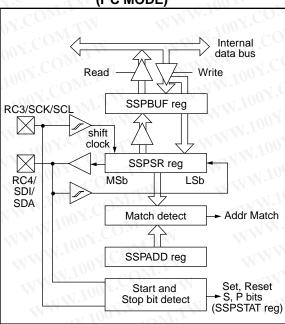
FIGURE 11-23: CLOCK SYNCHRONIZATION



11.5 SSP I²C Operation

The SSP module in I²C mode fully implements all slave functions, except general call support, and provides interrupts on start and stop bits in hardware to facilitate firmware implementations of the master functions. The SSP module implements the standard mode specifications as well as 7-bit and 10-bit addressing. Two pins are used for data transfer. These are the RC3/SCK/SCL pin, which is the clock (SCL), and the RC4/SDI/SDA pin, which is the data (SDA). The user must configure these pins as inputs or outputs through the TRISC<4:3> bits. The SSP module functions are enabled by setting SSP Enable bit SSPEN (SSP-CON<5>).

FIGURE 11-24: SSP BLOCK DIAGRAM (I²C MODE)



The SSP module has five registers for I²C operation. These are the:

- · SSP Control Register (SSPCON)
- SSP Status Register (SSPSTAT)
- Serial Receive/Transmit Buffer (SSPBUF)
- SSP Shift Register (SSPSR) Not directly accessible
- · SSP Address Register (SSPADD)

The SSPCON register allows control of the I²C operation. Four mode selection bits (SSPCON<3:0>) allow one of the following I²C modes to be selected:

- I²C Slave mode (7-bit address)
- I²C Slave mode (10-bit address)
- I²C Slave mode (7-bit address), with start and stop bit interrupts enabled
- I²C Slave mode (10-bit address), with start and stop bit interrupts enabled
- I²C Firmware controlled Master Mode, slave is idle

Selection of any I²C mode, with the SSPEN bit set, forces the SCL and SDA pins to be open drain, provided these pins are programmed to inputs by setting the appropriate TRISC bits.

The SSPSTAT register gives the status of the data transfer. This information includes detection of a START or STOP bit, specifies if the received byte was data or address if the next byte is the completion of 10-bit address, and if this will be a read or write data transfer. The SSPSTAT register is read only.

The SSPBUF is the register to which transfer data is written to or read from. The SSPSR register shifts the data in or out of the device. In receive operations, the SSPBUF and SSPSR create a doubled buffered receiver. This allows reception of the next byte to begin before reading the last byte of received data. When the complete byte is received, it is transferred to the SSPBUF register and flag bit SSPIF is set. If another complete byte is received before the SSPBUF register is read, a receiver overflow has occurred and bit SSPOV (SSPCON<6>) is set and the byte in the SSPSR is lost.

The SSPADD register holds the slave address. In 10-bit mode, the user first needs to write the high byte of the address (1111 0 A9 A8 0). Following the high byte address match, the low byte of the address needs to be loaded (A7:A0).

11.5.1 SLAVE MODE

In slave mode, the SCL and SDA pins must be configured as inputs (TRISC<4:3> set). The SSP module will override the input state with the output data when required (slave-transmitter).

When an address is matched or the data transfer after an address match is received, the hardware automatically will generate the acknowledge (ACK) pulse, and then load the SSPBUF register with the received value currently in the SSPSR register.

There are certain conditions that will cause the SSP module not to give this \overline{ACK} pulse. These are if either (or both):

- a) The buffer full bit BF (SSPSTAT<0>) was set before the transfer was received.
- The overflow bit SSPOV (SSPCON<6>) was set before the transfer was received.

In this case, the SSPSR register value is not loaded into the SSPBUF, but bit SSPIF (PIR1<3>) is set. Table 11-4 shows what happens when a data transfer byte is received, given the status of bits BF and SSPOV. The shaded cells show the condition where user software did not properly clear the overflow condition. Flag bit BF is cleared by reading the SSPBUF register while bit SSPOV is cleared through software.

The SCL clock input must have a minimum high and low for proper operation. The high and low times of the I^2C specification as well as the requirement of the SSP module is shown in timing parameter #100 and parameter #101.

11.5.1.1 ADDRESSING

Once the SSP module has been enabled, it waits for a START condition to occur. Following the START condition, the 8-bits are shifted into the SSPSR register. All incoming bits are sampled with the rising edge of the clock (SCL) line. The value of register SSPSR<7:1> is compared to the value of the SSPADD register. The

address is compared on the falling edge of the eighth clock (SCL) pulse. If the addresses match, and the BF and SSPOV bits are clear, the following events occur:

- The SSPSR register value is loaded into the SSPBUF register.
- b) The buffer full bit, BF is set.
- c) An ACK pulse is generated.
- d) SSP interrupt flag bit, SSPIF (PIR1<3>) is set (interrupt is generated if enabled) - on the falling edge of the ninth SCL pulse.

In 10-bit address mode, two address bytes need to be received by the slave (Figure 11-16). The five Most Significant bits (MSbs) of the first address byte specify if this is a 10-bit address. Bit R / \overline{W} (SSPSTAT<2>) must specify a write so the slave device will receive the second address byte. For a 10-bit address the first byte would equal '1111 0 A9 A8 0', where A9 and A8 are the two MSbs of the address. The sequence of events for 10-bit address is as follows, with steps 7- 9 for slave-transmitter:

- Receive first (high) byte of Address (bits SSPIF, BF, and bit UA (SSPSTAT<1>) are set).
- Update the SSPADD register with second (low) byte of Address (clears bit UA and releases the SCL line).
- Read the SSPBUF register (clears bit BF) and clear flag bit SSPIF.
- Receive second (low) byte of Address (bits SSPIF, BF, and UA are set).
- Update the SSPADD register with the first (high) byte of Address, if match releases SCL line, this will clear bit UA.
- Read the SSPBUF register (clears bit BF) and clear flag bit SSPIF.
- 7. Receive repeated START condition.
- Receive first (high) byte of Address (bits SSPIF and BF are set).
- 9. Read the SSPBUF register (clears bit BF) and clear flag bit SSPIF.

TABLE 11-4: DATA TRANSFER RECEIVED BYTE ACTIONS

	Bits as Data is Received	V.100Y.COM.TW	WWW.1007.C	Set bit SSPIF
BF	SSPOV	$SSPSR \to SSPBUF$	Generate ACK Pulse	(SSP Interrupt occurs if enabled)
0	0	Yes	Yes	Yes
1	0	No No	No	Yes
1	1	No	No	Yes
0	1	No OM	No	Yes

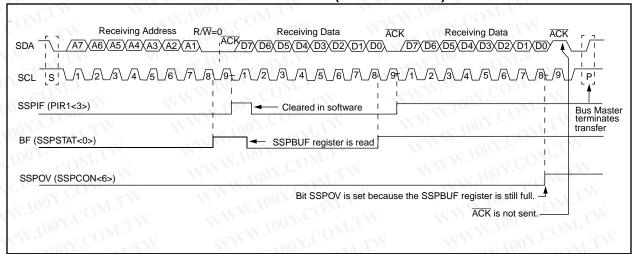
11.5.1.2 RECEPTION

When the R/\overline{W} bit of the address byte is clear and an address match occurs, the R/\overline{W} bit of the SSPSTAT register is cleared. The received address is loaded into the SSPBUF register.

When the address byte overflow condition exists, then no acknowledge (ACK) pulse is given. An overflow condition is defined as either bit BF (SSPSTAT<0>) is set or bit SSPOV (SSPCON<6>) is set.

An SSP interrupt is generated for each data transfer byte. Flag bit SSPIF (PIR1<3>) must be cleared in software. The SSPSTAT register is used to determine the status of the byte.





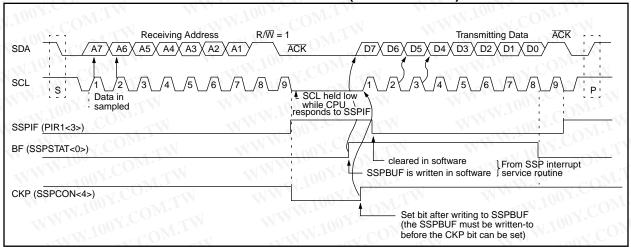
11.5.1.3 TRANSMISSION

When the R/W bit of the incoming address byte is set and an address match occurs, the R/W bit of the SSPSTAT register is set. The received address is loaded into the SSPBUF register. The ACK pulse will be sent on the ninth bit, and pin RC3/SCK/SCL is held low. The transmit data must be loaded into the SSPBUF register, which also loads the SSPSR register. Then pin RC3/SCK/SCL should be enabled by setting bit CKP (SSPCON<4>). The master must monitor the SCL pin prior to asserting another clock pulse. The slave devices may be holding off the master by stretching the clock. The eight data bits are shifted out on the falling edge of the SCL input. This ensures that the SDA signal is valid during the SCL high time (Figure 11-26).

An SSP interrupt is generated for each data transfer byte. Flag bit SSPIF must be cleared in software, and the SSPSTAT register is used to determine the status of the byte. Flag bit SSPIF is set on the falling edge of the ninth clock pulse.

As a slave-transmitter, the \overline{ACK} pulse from the master-receiver is latched on the rising edge of the ninth SCL input pulse. If the SDA line was high (not \overline{ACK}), then the data transfer is complete. When the \overline{ACK} is latched by the slave, the slave logic is reset (resets SSPSTAT register) and the slave then monitors for another occurrence of the START bit. If the SDA line was low (\overline{ACK}), the transmit data must be loaded into the SSPBUF register, which also loads the SSPSR register. Then pin RC3/SCK/SCL should be enabled by setting bit CKP.

FIGURE 11-26: I²C WAVEFORMS FOR TRANSMISSION (7-BIT ADDRESS)



11.5.2 MASTER MODE

Master mode of operation is supported in firmware using interrupt generation on the detection of the START and STOP conditions. The STOP (P) and START (S) bits are cleared from a reset or when the SSP module is disabled. The STOP (P) and START (S) bits will toggle based on the START and STOP conditions. Control of the I²C bus may be taken when the P bit is set, or the bus is idle and both the S and P bits are clear

In master mode the SCL and SDA lines are manipulated by clearing the corresponding TRISC<4:3> bit(s). The output level is always low, irrespective of the value(s) in PORTC<4:3>. So when transmitting data, a '1' data bit must have the TRISC<4> bit set (input) and a '0' data bit must have the TRISC<4> bit cleared (output). The same scenario is true for the SCL line with the TRISC<3> bit.

The following events will cause SSP Interrupt Flag bit, SSPIF, to be set (SSP Interrupt if enabled):

- START condition
- STOP condition
- · Data transfer byte transmitted/received

Master mode of operation can be done with either the slave mode idle (SSPM3:SSPM0 = 1011) or with the slave active. When both master and slave modes are enabled, the software needs to differentiate the source(s) of the interrupt.

11.5.3 MULTI-MASTER MODE

In multi-master mode, the interrupt generation on the detection of the START and STOP conditions allows the determination of when the bus is free. The STOP (P) and START (S) bits are cleared from a reset or when the SSP module is disabled. The STOP (P) and START (S) bits will toggle based on the START and STOP conditions. Control of the I²C bus may be taken when bit P (SSPSTAT<4>) is set, or the bus is idle and both the S and P bits clear. When the bus is busy, enabling the SSP Interrupt will generate the interrupt when the STOP condition occurs.

In multi-master operation, the SDA line must be monitored to see if the signal level is the expected output level. This check only needs to be done when a high level is output. If a high level is expected and a low level is present, the device needs to release the SDA and SCL lines (set TRISC<4:3>). There are two stages where this arbitration can be lost, these are:

- Address Transfer
- Data Transfer

When the slave logic is enabled, the slave continues to receive. If arbitration was lost during the address transfer stage, communication to the device may be in progress. If addressed an \overline{ACK} pulse will be generated. If arbitration was lost during the data transfer stage, the device will need to re-transfer the data at a later time.

TABLE 11-5: REGISTERS ASSOCIATED WITH I²C OPERATION

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other resets
0Bh, 8Bh, 10Bh, 18Bh	INTCON	GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	PSPIF ⁽¹⁾	(2)	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
8Ch	PIE1	PSPIE ⁽¹⁾	(2)	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
13h	SSPBUF	Synchrono	us Serial	Port Rece	ive Buffe	er/Transmi	t Register	CO_{M}		xxxx xxxx	uuuu uuuu
93h	SSPADD	Synchrono	us Serial	Port (I ² C ı	mode) A	ddress Re	gister	COM	11.4	0000 0000	0000 0000
14h	SSPCON	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000	0000 0000
94h	SSPSTAT	SMP ⁽³⁾	CKE ⁽³⁾	D/Ā	Р	S	R/W	UA	BF	0000 0000	0000 0000
87h	TRISC	PORTC Da	ata Directi	on registe	r	W	- x 1	10 Y.C	OM.T'	1111 1111	1111 1111

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by SSP module in SPI mode.

- Note 1: PSPIF and PSPIE are reserved on the PIC16C66, always maintain these bits clear.
 - 2: PIR1<6> and PIE1<6> are reserved, always maintain these bits clear.
 - 3: The SMP and CKE bits are implemented on the PIC16C66/67 only. All other PIC16C6X devices have these two bits unimplemented, read as '0'.

FIGURE 11-27: OPERATION OF THE I²C MODULE IN IDLE_MODE, RCV_MODE OR XMIT_MODE

```
IDLE_MODE (7-bit):
if (Addr_match)
                                           Set interrupt:
                                           if (R/\overline{W} = 1)
                                                                   Send \overline{ACK} = 0:
                                                                   set XMIT_MODE;
                                           else if (R/\overline{W} = 0) set RCV_MODE;
RCV_MODE:
if ((SSPBUF=Full) OR (SSPOV = 1))
                   Set SSPOV;
                   Do not acknowledge;
                   transfer SSPSR → SSPBUF;
                   send \overline{ACK} = 0;
Receive 8-bits in SSPSR;
Set interrupt;
XMIT_MODE:
While ((SSPBUF = Empty) AND (CKP=0)) Hold SCL Low;
Send byte;
Set interrupt;
if (\overline{ACK} Received = 1)
                                           End of transmission;
                                           Go back to IDLE_MODE;
else if ( ACK Received = 0) Go back to XMIT_MODE;
IDLE_MODE (10-Bit):
If (High_byte_addr_match AND (R/\overline{W} = 0))
                   PRIOR_ADDR_MATCH = FALSE;
                   Set interrupt;
                  if ((SSPBUF = Full) OR ((SSPOV = 1))
                                   Set SSPOV;
                                   Do not acknowledge;
                  else
                                   Set UA = 1;
                          {
                                   Send \overline{ACK} = 0;
                                   While (SSPADD not updated) Hold SCL low;
                                   Clear UA = 0;
                                   Receive Low_addr_byte;
                                   Set interrupt;
                                  Set UA = 1;
                                   If (Low_byte_addr_match)
                                                   PRIOR_ADDR_MATCH = TRUE;
                                                   Send \overline{ACK} = 0;
                                                   while (SSPADD not updated) Hold SCL low;
                                                   Clear UA = 0;
                                                   Set RCV_MODE;
else if (High_byte_addr_match AND (R/\overline{W} = 1)
                  if (PRIOR_ADDR_MATCH)
          {
                                  send \overline{ACK} = 0:
                                   set XMIT_MODE;
          else PRIOR_ADDR_MATCH = FALSE;
```

12.0 UNIVERSAL SYNCHRONOUS ASYNCHRONOUS RECEIVER TRANSMITTER (USART) MODULE

Applicable Devices

61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

The Universal Synchronous Asynchronous Receiver Transmitter (USART) module is one of the two serial I/O modules. (USART is also known as a Serial Communications Interface or SCI) The USART can be configured as a full duplex asynchronous system that can communicate with peripheral devices such as CRT ter-

minals and personal computers, or it can be configured as a half duplex synchronous system that can communicate with peripheral devices such as A/D or D/A integrated circuits, Serial EEPROMs etc.

The USART can be configured in the following modes:

- Asynchronous (full duplex)
- · Synchronous Master (half duplex)
- Synchronous Slave (half duplex)

Bit SPEN (RCSTA<7>) and bits TRISC<7:6> have to be set in order to configure pins RC6/TX/CK and RC7/RX/DT as the Universal Synchronous Asynchronous Receiver Transmitter.

FIGURE 12-1: TXSTA: TRANSMIT STATUS AND CONTROL REGISTER (ADDRESS 98h)

R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R-1	R/W-0
CSRC	TX9	TXEN	SYNC	7	BRGH	TRMT	TX9D
bit7	TW	11	MAN	NY.CO	WT		bit0

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

- n =Value at POR reset

bit 7: CSRC: Clock Source Select bit

Asynchronous mode

Don't care

Synchronous mode

1 = Master mode (Clock generated internally from BRG)

0 = Slave mode (Clock from external source)

bit 6: TX9: 9-bit Transmit Enable bit

1 = Selects 9-bit transmission

0 = Selects 8-bit transmission

bit 5: TXEN: Transmit Enable bit

1 = Transmit enabled

0 = Transmit disabled

Note: SREN/CREN overrides TXEN in SYNC mode.

bit 4: SYNC: USART Mode Select bit

1 = Synchronous mode

0 = Asynchronous mode

bit 3: Unimplemented: Read as '0'

bit 2: BRGH: High Baud Rate Select bit

Asynchronous mode

1 = High speed

Note: For the PIC16C63/R63/65/65A/R65 the asynchronous high speed mode (BRGH = 1) may experience a high rate of receive errors. It is recommended that BRGH = 0. If you desire a higher baud rate than BRGH = 0 can support, refer to the device errata for additional information or use the PIC16C66/67.

0 = Low speed

Synchronous mode

Unused in this mode

bit 1: TRMT: Transmit Shift Register Status bit

1 = TSR empty

0 = TSR full

bit 0: TX9D: 9th bit of transmit data. Can be parity bit.

FIGURE 12-2: RCSTA: RECEIVE STATUS AND CONTROL REGISTER (ADDRESS 18h)

R/W-0 R/W-0 R/W-0 R/W-0 U-0 R-0 R-0 R-x **SPEN** RX9 RX9D = Readable bit **SREN CREN FERR OERR** W = Writable bit bit0 bit7 U = Unimplemented bit, read as '0' = Value at POR reset = unknown bit 7: SPEN: Serial Port Enable bit (Configures RC7/RX/DT and RC6/TX/CK pins as serial port pins when bits TRISC<7:6> are set) 1 = Serial port enabled 0 = Serial port disabled bit 6: RX9: 9-bit Receive Enable bit 1 = Selects 9-bit reception 0 = Selects 8-bit reception SREN: Single Receive Enable bit bit 5: Asynchronous mode Don't care Synchronous mode - master 1 = Enables single receive 0 = Disables single receive This bit is cleared after reception is complete. Synchronous mode - slave Unused in this mode **CREN**: Continuous Receive Enable bit bit 4: Asynchronous mode 1 = Enables continuous receive 0 = Disables continuous receive Synchronous mode 1 = Enables continuous receive until enable bit CREN is cleared (CREN overrides SREN) 0 = Disables continuous receive

bit 3: Unimplemented: Read as '0'

bit 2: FERR: Framing Error bit

1 = Framing error (Can be updated by reading RCREG register and receive next valid byte)

0 = No framing error

bit 1: **OERR**: Overrun Error bit

1 = Overrun error (Can be cleared by clearing bit CREN)

0 = No overrun error

bit 0: **RX9D**: 9th bit of received data (Can be parity bit)

12.1 USART Baud Rate Generator (BRG)

Applicable Devices 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

The BRG supports both the Asynchronous and Synchronous modes of the USART. It is a dedicated 8-bit baud rate generator. The SPBRG register controls the period of a free running 8-bit timer. In asynchronous mode bit BRGH (TXSTA<2>) also controls the baud rate. In synchronous mode bit BRGH is ignored. Table 12-1 shows the formula for computation of the baud rate for different USART modes which only apply in master mode (internal clock).

Given the desired baud rate and Fosc, the nearest integer value for the SPBRG register can be calculated using the formula in Table 12-1. From this, the error in baud rate can be determined.

Example 12-1 shows the calculation of the baud rate error for the following conditions:

Fosc = 16 MHz Desired Baud Rate = 9600 BRGH = 0 SYNC = 0

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EXAMPLE 12-1: CALCULATING BAUD RATE ERROR

Desired Baud rate = Fosc / (64 (X + 1))9600 = 16000000 / (64 (X + 1)) $X = \lfloor 25.042 \rfloor = 25$

Calculated Baud Rate=16000000 / (64 (25 + 1))

= 9615

Error = (Calculated Baud Rate - Desired Baud Rate)

Desired Baud Rate

= (9615 - 9600) / 9600

= 0.16%

It may be advantageous to use the high baud rate (BRGH = 1) even for slower baud clocks. This is because the Fosc/(16(X + 1)) equation can reduce the baud rate error in some cases.

Note: For the PIC16C63/R63/65/65A/R65 the asynchronous high speed mode (BRGH = 1) may experience a high rate of receive errors. It is recommended that BRGH = 0. If you desire a higher baud rate than BRGH = 0 can support, refer to the device errata for additional information or use the PIC16C66/67.

Writing a new value to the SPBRG register, causes the BRG timer to be reset (or cleared), this ensures that the BRG does not wait for a timer overflow before outputting the new baud rate.

TABLE 12-1: BAUD RATE FORMULA

SYNC	BRGH = 0 (Low Speed)	BRGH = 1 (High Speed)
0	(Asynchronous) Baud Rate = Fosc/(64(X+1))	Baud Rate = Fosc/(16(X+1))
1	(Synchronous) Baud Rate = Fosc/(4(X+1))	N/A N/A

X = value in SPBRG (0 to 255)

TABLE 12-2: REGISTERS ASSOCIATED WITH BAUD RATE GENERATOR

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
98h	TXSTA	CSRC	TX9	TXEN	SYNC	- TAX	BRGH	TRMT	TX9D	0000 -010	0000 -010
18h	RCSTA	SPEN	RX9	SREN	CREN	11	FERR	OERR	RX9D	0000 -00x	0000 -00x
99h	SPBRG	Baud Rat	e Genera	tor Registe	er	11/1	/ // /	NY.CO		0000 0000	0000 0000

Legend: x = unknown, - = unimplemented read as '0'. Shaded cells are not used by the BRG.

BAUD RATES FOR SYNCHRONOUS MODE TABLE 12-3:

	BAUD	Fosc = 2	20 MHz	SPBRG	16 MHz	3 MHz		10 MHz		SPBRG	7.15909 I	MHz	SPBRG
COJ	RATE (K)	KBAUD	% ERROR	value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	value (decimal)	KBAUD	% ERROR	value (decimal)
CO	0.3	NA	-	- N 3N -	NA	$CG_{k_{r}}$	- X T.	NA	- 1 - N	4	NA		-
	1.2	NA	- 1	V V -	NA	- 1	(J,j_{A})	NA		-x1 ±00	NA	- L	-
0	2.4	NA	-		NA		-XXI	NA	W	///	NA	- W	- W
	9.6	NA	- '	W	NA NA		V . F	9.766	+1.73	255	9.622	+0.23	185
- 7	19.2	19.53	+1.73	255	19.23	+0.16	207	19.23	+0.16	129	19.24	+0.23	92
"	76.8	76.92	+0.16	64	76.92	+0.16	51	75.76	-1.36	32	77.82	+1.32	22
_7	96	96.15	+0.16	51	95.24	-0.79	41	96.15	+0.16	25	94.20	-1.88	18
X	300	294.1	-1.96	16	307.69	+2.56	12	312.5	+4.17	7	298.3	-0.57	5
	500	500	0	9	500	0	7	500	0	4	NA	Co	= 1
00	HIGH	5000	- N	0	4000	100^{-1} .	0	2500	-	0	1789.8	301	0
	LOW	19.53	-×1 -	255	15.625	- 1	255	9.766	-	255	6.991		255

WWW.I	LOW	19.53	- N	255	15.62	5 -	25	5 9.7	66	- 1/2	255 6	5.991	·Co	255		
WWW.10	ooy.C	Fosc = 5	5.0688 MI	Hz	4 MHz	1100	OY.CC	3.579545 MHz			1 MHz			32.768 k		
WWW.	BAUD RATE (K)	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)
Al Al	0.3	NA	11:17	-	NA		100	NA	1.7.	-	NA	-13/1	00:	0.303	+1.14	26
	1.2	NA	TAN-	- XX	NA	T V	- 05	NA	-11	-	1.202	+0.16	207	1.170	-2.48	6
M	2.4	NA	T.A.	<u>-</u>	NA		4.100 ,	NA	$M_{T_{\mu}}$	-	2.404	+0.16	103	NA	1	
W	9.6	9.6	0	131	9.615	+0.16	103	9.622	+0.23	92	9.615	+0.16	25	NA		-
	19.2	19.2	0	65	19.231	+0.16	51	19.04	-0.83	46	19.24	+0.16	12	NA	Mir	
-11	76.8	79.2	+3.13	15	76.923	+0.16	12	74.57	-2.90	11	83.34	+8.51	2	NA	- 1	N -
	96	97.48	+1.54	12	1000	+4.17	9	99.43	+3.57	8	NA	5-41	W. Jan	NA	111.	- T
- 1	300	316.8	+5.60	3	NA	-11	N	298.3	-0.57	2	NA		- 40	NA	- K 1	(1)\-
	500	NA		$N;_{T}$	NA	-71	XI 1	NA	and		NA		111	NA	OJr.	.21
<	HIGH	1267	J.GU	0	100	- 11	0	894.9	CA.	0	250	-	0	8.192	· - K	0
	LOW	4.950	· -	255	3.906	-	255	3.496	. ~	255	0.9766	-	255	0.032	CGM	255

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TABLE 12-4: BAUD RATES FOR ASYNCHRONOUS MODE (BRGH = 0)

BAUD	Fosc = 2	20 MHz	SPBRG	16 MHz		SPBRG	10 MHz		SPBRG	7.15909	MHz	SPBRG
RATE (K)	KBAUD	% ERROR	value (decimal)	KBAUD	% ERROR	value (decimal)	KBAUD	% ERROR	value (decimal)	KBAUD	% ERROR	value (decimal)
0.3	NA	1 100	-71	NA	-	•	NA	• ~(1/1/2-	NA	-	- (P)
1.2	1.221	+1.73	255	1.202	+0.16	207	1.202	+0.16	129	1.203	+0.23	92
2.4	2.404	+0.16	129	2.404	+0.16	103	2.404	+0.16	64	2.380	-0.83	46
9.6	9.469	-1.36	32	9.615	+0.16	25	9.766	+1.73	15	9.322	-2.90	11
19.2	19.53	+1.73	15	19.23	+0.16	12	19.53	+1.73	7	18.64	-2.90	5
76.8	78.13	+1.73	3	83.33	+8.51	2	78.13	+1.73	1	NA	-	4/15/
96	104.2	+8.51	2	NA	-	-	NA	700	CON	NA	-	XX
300	312.5	+4.17	0	NA		- 1	NA	700		NA	-	15 11
500	NA	-5XX	100.	NA		-	NA	V.To	0	NA		- 1
HIGH	312.5		0	250	- 1	0	156.3	00	0	111.9	N -	0
LOW	1.221		255	0.977	1.1.	255	0.6104	TAN - IV	255	0.437		255

	FOSC = 5.0688 MHz		4 MHz			3.579545 MHz			1 MHz			32.768 kHz			
BAUD RATE (K)	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)
0.3	0.31	+3.13	255	0.3005	-0.17	207	0.301	+0.23	185	0.300	+0.16	51	0.256	-14.67	110
1.2	1.2	0	65	1.202	+1.67	51	1.190	-0.83	46	1.202	+0.16	12	NA	-	N. P.
2.4	2.4	0	32	2.404	+1.67	25	2.432	+1.32	22	2.232	-6.99	6	NA	_\\\	-x1 100
9.6	9.9	+3.13	7	NA)//r.	9.322	-2.90	5	NA	<1 (=O)	-	NA		11 -11 -
19.2	19.8	+3.13	3	NA	1 C	-17	18.64	-2.90	2	NA	-	-11	NA	-	
76.8	79.2	+3.13	0	NA	C	Ohr.,	NA	-	- 1	NA	- < 7 - C ()M.	NA		11-
96	NA	-	-	NA	003	- 1	NA	-	1/1-1.	NA	07-	~~1.7	NA	-	W - 411
300	NA	-	1	NA	7	CGMr.	NA	-	-	NA	- 	Oh	NA	-	- N-1
500	NA	-	-11	NA	1087	-	NA	-	1	NA	00_{7} .	100	NA	-	-
HIGH	79.2	-	0	62.500	70.	0	55.93	ī -	0	15.63	-	0	0.512	-	0
LOW	0.3094	-	255	3.906	. 160	255	0.2185	-	255	0.0610	10A F.	255	0.0020	-	255

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TABLE 12-5: BAUD RATES FOR ASYNCHRONOUS MODE (BRGH = 1)

BAUD	Fosc = 2	20 MHz	SPBRG	16 MHz		SPBRG	10 MHz		SPBRG	7.16 MH	Z	SPBRG
RATE (K)	KBAUD	% ERROR	value (decimal)	KBAUD	% ERROR	value (decimal)	KBAUD	% ERROR	value (decimal)	KBAUD	% ERROR	value (decimal)
9.6	9.615	+0.16	129	9.615	+0.16	103	9.615	+0.16	64	9.520	-0.83	46
19.2	19.230	+0.16	64	19.230	+0.16	51	18.939	-1.36	32	19.454	+1.32	22
38.4	37.878	-1.36	32	38.461	+0.16	25	39.062	+1.7	15	37.286	-2.90	11
57.6	56.818	-1.36	21	58.823	+2.12	16	56.818	-1.36	10	55.930	-2.90	7
115.2	113.636	-1.36	10	111.111	-3.55	8	125	+8.51	4	111.860	-2.90	3
250	250	0	4	250	0	3	NA	V .	41 1 OU 3	NA	$V_{i,T}$	-
625	625	0	1	NA	CG_{IA}		625	0	0	NA	-	-
1250	1250	0	0	NA	- 1	(3.5)	NA		_x1 40U	NA	1.1	-

BAUD	Fosc = 5	5.068 MHz	SPBRG	4 MHz		SPBRG	3.579 MI	Ηz	SPBRG	1 MHz		SPBRG	32.768	kHz	SPBRG
RATE (K)	KBAUD	% ERROR	value (decimal)	KBAUD	% ERROR	value (decimal)	KBAUD	% ERROR	value (decimal)	KBAUD	% ERROR	value (decimal)	KBAUD	% ERROR	value (decimal)
9.6	9.6	0	32	NA	100.	Mor	9.727	+1.32	22	8.928	-6.99	6	NA	-	-
19.2	18.645	-2.94	16	1.202	+0.17	207	18.643	-2.90	11	20.833	+8.51	2	NA	-	-
38.4	39.6	+3.12	7	2.403	+0.13	103	37.286	-2.90	5	31.25	-18.61		NA	-	-
57.6	52.8	-8.33	5	9.615	+0.16	25	55.930	-2.90	3	62.5	+8.51	0	NA	-	-
115.2	105.6	-8.33	2	19.231	+0.16	12	111.860	-2.90	1	NA	10	- (' 0\	NA	×1 -	-
250	NA		-	NA	0		223.721	-10.51	0	NA	170	1.	NA	_	-
625	NA		-	NA	11-10	C	NA	-e-T	-	NA	11.70	-1 CO	NA	- IX	-
1250	NA	T=11	-	NA			NA		-	NA	. = (()	07	NA	-	-

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Note: For the PIC16C63/R63/65/65A/R65 the asynchronous high speed mode (BRGH = 1) may experience a high rate of receive errors. It is recommended that BRGH = 0. If you desire a higher baud rate than BRGH = 0 can support, refer to the device errata for additional information or use the PIC16C66/67.

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12.1.1 SAMPLING

The data on the RC7/RX/DT pin is sampled three times by a majority detect circuit to determine if a high or a low level is present at the RX pin. If bit BRGH (TXSTA<2>) is clear (i.e., at the low baud rates), the sampling is done on the seventh, eighth and ninth falling edges of a x16 clock (Figure 12-3). If bit BRGH is

set (i.e., at the high baud rates), the sampling is done on the 3 clock edges preceding the second rising edge after the first falling edge of a x4 clock (Figure 12-4 and Figure 12-5).

FIGURE 12-3: RX PIN SAMPLING SCHEME (BRGH = 0) PIC16C63/R63/65/65A/R65

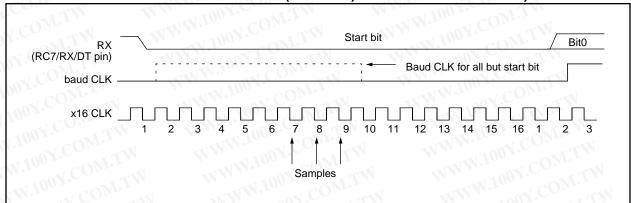


FIGURE 12-4: RX PIN SAMPLING SCHEME (BRGH = 1) (PIC16C63/R63/65/65A/R65)

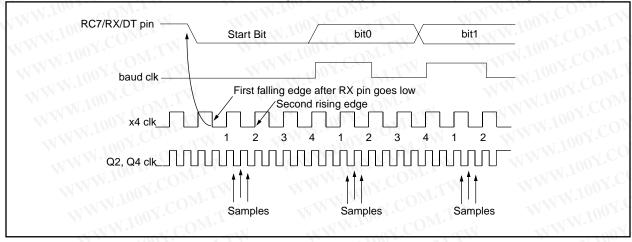
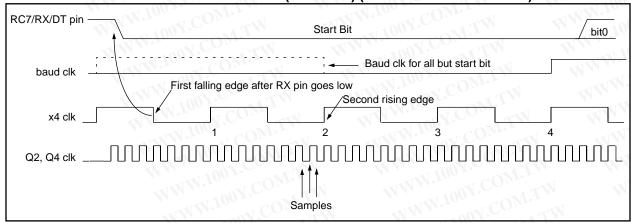
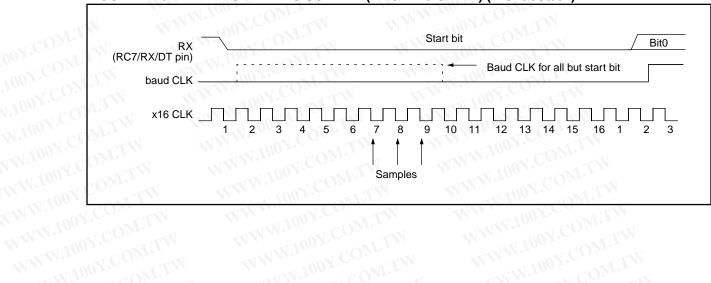


FIGURE 12-5: RX PIN SAMPLING SCHEME (BRGH = 1) (PIC16C63/R63/65/65A/R65)







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12.2 <u>USART Asynchronous Mode</u>

Applicable Devices
61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

In this mode, the USART uses standard nonreturn-to-zero (NRZ) format (one start bit, eight or nine data bits and one stop bit). The most common data format is 8-bits. An on-chip dedicated 8-bit baud rate generator can be used to derive standard baud rate frequencies from the oscillator. The USART transmits and receives the LSb first. The USART's transmitter and receiver are functionally independent but use the same data format and baud rate. The baud rate generator produces a clock either x16 or x64 of the bit shift rate, depending on bit BRGH (TXSTA<2>). Parity is not supported by the hardware, but can be implemented in software (and stored as the ninth data bit). Asynchronous mode is stopped during SLEEP.

Asynchronous mode is selected by clearing bit SYNC (TXSTA<4>).

The USART Asynchronous module consists of the following important elements:

- Baud Rate Generator
- Sampling Circuit
- · Asynchronous Transmitter
- · Asynchronous Receiver

12.2.1 USART ASYNCHRONOUS TRANSMITTER

The USART transmitter block diagram is shown in Figure 12-7. The heart of the transmitter is the transmit (serial) shift register (TSR). The shift register obtains its data from the read/write transmit buffer, TXREG. The TXREG register is loaded with data in software. The TSR register is not loaded until the STOP bit has been transmitted from the previous load. As soon as the STOP bit is transmitted, the TSR is loaded with new data from the TXREG (if available). Once the TXREG register transfers the data to the TSR register (occurs in one TCY) the TXREG register is empty and flag bit TXIF (PIR1<4>) is set. This interrupt is enabled/dis-

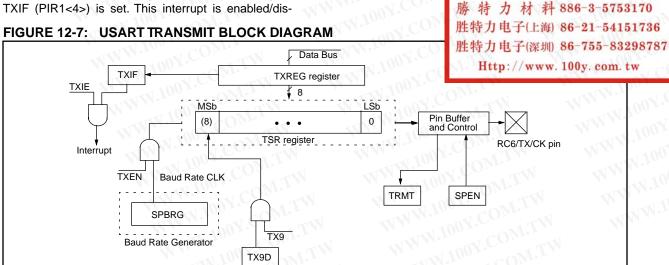
abled by setting/clearing enable bit TXIE (PIE1<4>). Flag bit TXIF will be set regardless of the state of enable bit TXIE and cannot be cleared in software. It will reset only when new data is loaded into the TXREG register. While flag bit TXIF indicates the status of the TXREG register, another bit, TRMT (TXSTA<1>) shows the status of the TSR register. Status bit TRMT is a read only bit which is set when the TSR register is empty. No interrupt logic is tied to this bit, so the user has to poll this bit in order to determine if the TSR register is empty.

Note 1: The TSR register is not mapped in data memory so it is not available to the user.

Note 2: Flag bit TXIF is set when enable bit TXEN is set.

Transmission is enabled by setting enable bit TXEN (TXSTA<5>). The actual transmission will not occur until the TXREG register has been loaded with data and the baud rate generator (BRG) has produced a shift clock (Figure 12-7). The transmission can also be started by first loading the TXREG register and then setting enable bit TXEN. Normally when transmission is first started, the TSR register is empty, so a transfer to the TXREG register will result in an immediate transfer to TSR register resulting in an empty TXREG register. A back-to-back transfer is thus possible (Figure 12-9). Clearing enable bit TXEN during a transmission will cause the transmission to be aborted and will reset the transmitter. As a result the RC6/TX/CK pin will revert to hi-impedance.

In order to select 9-bit transmission, transmit bit TX9 (TXSTA<6>) should be set and the ninth bit should be written to bit TX9D (TXSTA<0>). The ninth bit must be written before writing the 8-bit data to the TXREG register. This is because a data write to the TXREG register can result in an immediate transfer of the data to the TSR register (if the TSR is empty). In such a case, an incorrect ninth data bit maybe loaded in the TSR register.



Steps to follow when setting up an Asynchronous Transmission:

- 1. Initialize the SPBRG register for the appropriate baud rate. If a high speed baud rate is desired, then set bit BRGH. (Section 12.1).
- Enable the asynchronous serial port by clearing bit SYNC and setting bit SPEN.
- If interrupts are desired, then set enable bit TXIE.
- If 9-bit transmission is desired, then set transmit bit TX9.

- 5. Enable the transmission by setting bit TXEN, which will also set bit TXIF.
- 6. If 9-bit transmission is selected, the ninth bit should be loaded in bit TX9D.
- Load data to the TXREG register (starts transmission).

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FIGURE 12-8: ASYNCHRONOUS MASTER TRANSMISSION

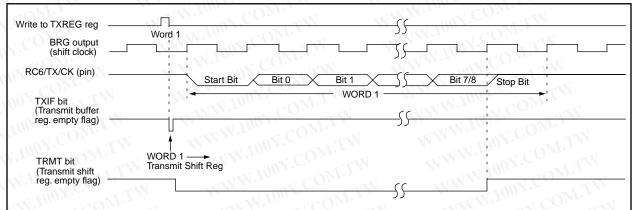


FIGURE 12-9: ASYNCHRONOUS MASTER TRANSMISSION (BACK TO BACK)

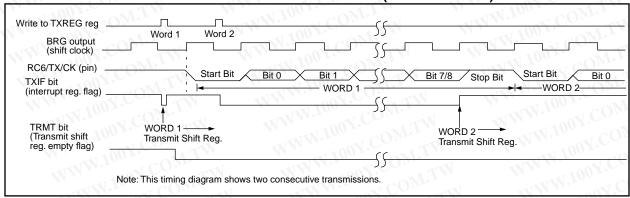


TABLE 12-6: REGISTERS ASSOCIATED WITH ASYNCHRONOUS TRANSMISSION

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR,	Value on all other
		M. A.	V.U.		N		NY 1	107.0	VITA	BOR	Resets
0Ch	PIR1	PSPIF ⁽¹⁾	(2)	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
18h	RCSTA	SPEN	RX9	SREN	CREN		FERR	OERR	RX9D	0000 -00x	0000 -00x
19h	TXREG	USART Tra	nsmit R	egister	IN			1.100	COM	0000 0000	0000 0000
8Ch	PIE1	PSPIE ⁽¹⁾	(2)	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
98h	TXSTA	CSRC	TX9	TXEN	SYNC	_	BRGH	TRMT	TX9D	0000 -010	0000 -010
99h	SPBRG	Baud Rate	General	tor Registe	er	* I	- 11	Mira	A COL	0000 0000	0000 0000

Legend: x = unknown, - = unimplemented locations read as '0'. Shaded cells are not used for Asynchronous Transmission.

Note 1: PSPIF and PSPIE are reserved on the PIC16C63/R63/66, always maintain these bits clear.

2: PIR1<6> and PIE1<6> are reserved, always maintain these bits clear.

12.2.2 USART ASYNCHRONOUS RECEIVER

The receiver block diagram is shown in Figure 12-10. The data comes in the RC7/RX/DT pin and drives the data recovery block. The data recovery block is actually a high speed shifter operating at x16 times the baud rate, whereas the main receive serial shifter operates at the bit rate or at Fosc.

Once Asynchronous mode is selected, reception is enabled by setting bit CREN (RCSTA<4>).

The heart of the receiver is the receive (serial) shift register (RSR). After sampling the STOP bit, the received data in the RSR is transferred to the RCREG register (if it is empty). If the transfer is complete, flag bit RCIF (PIR1<5>) is set. The actual interrupt can be enabled/disabled by setting/clearing enable bit RCIE (PIE1<5>). Flag bit RCIF is a read only bit which is cleared by the hardware. It is cleared when the RCREG register has been read and is empty. The RCREG is double buffered register, i.e., it is a two deep FIFO. It is

possible for two bytes of data to be received and transferred to the RCREG FIFO and a third byte begin shifting to the RSR register. On the detection of the STOP bit of the third byte, if the RCREG is still full, then the overrun error bit, OERR (RCSTA<1>) will be set. The word in the RSR register will be lost. The RCREG register can be read twice to retrieve the two bytes in the FIFO. Overrun bit OERR has to be cleared in software. This is done by resetting the receive logic (CREN is cleared and then set). If bit OERR is set, transfers from the RSR register to the RCREG register are inhibited, so it is essential to clear overrun bit OERR if it is set. Framing error bit FERR (RCSTA<2>) is set if a stop bit is detected as clear. Error bit FERR and the 9th receive bit are buffered the same way as the receive data. Reading the RCREG register will load bits RX9D and FERR with new values. Therefore it is essential for the user to read the RCSTA register before reading RCREG in order not to lose the old FERR and RX9D information.

FIGURE 12-10: USART RECEIVE BLOCK DIAGRAM

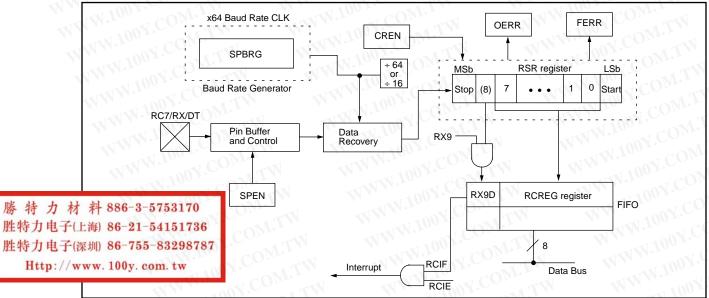
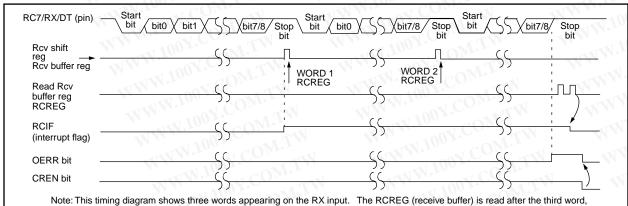


FIGURE 12-11: ASYNCHRONOUS RECEPTION



Note: This timing diagram shows three words appearing on the RX input. The RCREG (receive buffer) is read after the third word causing overrun error bit OERR to be set.

Steps to follow when setting up an Asynchronous Reception:

- Initialize the SPBRG register for the appropriate baud rate. If a high speed baud rate is desired, set bit BRGH (Section 12.1).
- Enable the asynchronous serial port by clearing bit SYNC and setting bit SPEN.
- If interrupts are desired, then set enable bit RCIE.
- If 9-bit reception is desired, then set bit RX9.
- 5. Enable the reception by setting enable bit CREN.

- 6. Flag bit RCIF will be set when reception is complete, and an interrupt will be generated if enable bit RCIE was set.
- 7. Read the RCSTA register to get the ninth bit (if enabled) and determine if any error occurred during reception.
 - Read the 8-bit received data by reading the RCREG register.
 - If any error occurred, clear the error by clearing enable bit CREN.

TABLE 12-7: REGISTERS ASSOCIATED WITH ASYNCHRONOUS RECEPTION

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
0Ch	PIR1	PSPIF ⁽¹⁾	(2)	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
18h (.C	RCSTA	SPEN	RX9	SREN	CREN	T	FERR	OERR	RX9D	0000 -00x	0000 -00x
1Ah	RCREG	USART Re	ceive Re	egister	OV.C	Ohr.	TW	W	MAN	0000 0000	0000 0000
8Ch	PIE1	PSPIE ⁽¹⁾	(2)	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
98h	TXSTA	CSRC	TX9	TXEN	SYNC	MA	BRGH	TRMT	TX9D	0000 -010	0000 -010
99h	SPBRG	Baud Rate	Genera	tor Regist	er (00)		N.T.W		M. A.	0000 0000	0000 0000

Legend: x = unknown, - = unimplemented locations read as '0'. Shaded cells are not used for Asynchronous Reception.

Note 1: PSPIE and PSPIF are reserved on the PIC16C63/R63/66, always maintain these bits clear. WWW.100Y.COM.T

2: PIE1<6> and PIR1<6> are reserved, always maintain these bits clear.

12.3 <u>USART Synchronous Master Mode</u>

Applicable Devices

61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

In Synchronous Master mode the data is transmitted in a half-duplex manner i.e., transmission and reception do not occur at the same time. When transmitting data the reception is inhibited and vice versa. Synchronous mode is entered by setting bit SYNC (TXSTA<4>). In addition enable bit SPEN (RCSTA<7>) is set in order to configure the RC6 and RC7 I/O pins to CK (clock) and DT (data) lines respectively. The Master mode indicates that the processor transmits the master clock on the CK line. The Master mode is entered by setting bit CSRC (TXSTA<7>).

12.3.1 USART SYNCHRONOUS MASTER TRANSMISSION

The USART transmitter block diagram is shown in Figure 12-7. The heart of the transmitter is the transmit (serial) shift register (TSR). The shift register obtains its data from the read/write transmit buffer register, TXREG. The TXREG register is loaded with data in software. The TSR register is not loaded until the last bit has been transmitted from the previous load. As soon as the last bit is transmitted, the TSR register is loaded with new data from the TXREG register (if available). Once the TXREG register transfers the data to the TSR register (occurs in one Tcycle), the TXREG register is empty and interrupt flag bit TXIF (PIR1<4>) is set. This interrupt can be enabled/disabled by setting/clearing enable bit TXIE (PIE1<4>). Flag bit TXIF will be set regardless of the status of enable bit TXIE and cannot be cleared in software. It will clear only when new data is loaded into the TXREG register. While flag bit TXIF indicates the status of the TXREG register, another bit, TRMT (TXSTA<1>), shows the status of the TSR register. Status bit TRMT is a read only bit which is set when the TSR register is empty. No interrupt logic is tied to this bit, so the user has to poll this bit in order to determine if the TSR register is empty. The TSR register is not mapped in data memory so it is not available to the user.

Transmission is enabled by setting enable bit TXEN (TXSTA<5>). The actual transmission will not occur until the TXREG register has been loaded with data. The first data bit will be shifted out on the next available rising edge of the clock on the CK line. Data out is stable around the falling edge of the synchronous clock (Figure 12-12). The transmission can also be started by first loading the TXREG register and then setting enable bit TXEN (Figure 12-13). This is advantageous when slow baud rates are selected, since the BRG is kept in reset when bits TXEN, CREN, and SREN are clear. Setting enable bit TXEN will start the BRG, creating a shift clock immediately. Normally when transmission is first started, the TSR register is empty, so a transfer to the TXREG register will result in an immediate transfer to TSR resulting in an empty TXREG register. Back-to-back transfers are possible.

Clearing enable bit TXEN, during a transmission, will cause the transmission to be aborted and will reset the transmitter. The DT and CK pins will revert to hi-impedance. If, during a transmission, either bit CREN or bit SREN is set the transmission is aborted and the DT pin reverts to a hi-impedance state (for a reception). The CK pin will remain an output if bit CSRC is set (internal clock). The transmitter logic however, is not reset although it is disconnected from the pins. In order to reset the transmitter, the user has to clear enable bit TXEN. If enable bit SREN is set (to interrupt an on going transmission and receive a single word), then after the single word is received, enable bit SREN will be cleared, and the serial port will revert back to transmitting since enable bit TXEN is still set. The DT line will immediately switch from hi-impedance receive mode to transmit and start driving. To avoid this, enable bit TXEN should be cleared.

In order to select 9-bit transmission, bit TX9 (TXSTA<6>) should be set and the ninth bit should be written to bit TX9D (TXSTA<0>). The ninth bit must be written before writing the 8-bit data to the TXREG register. This is because a data write to the TXREG register can result in an immediate transfer of the data to the TSR register (if the TSR is empty). If the TSR register was empty and the TXREG register was written before writing the "new" TX9D, the "present" value of bit TX9D is loaded.

Steps to follow when setting up a Synchronous Master Transmission:

- 1. Initialize the SPBRG register for the appropriate baud rate (Section 12.1).
- Enable the synchronous master serial port by setting bits SYNC, SPEN, and CSRC.
- If interrupts are desired, then set enable bit TXIE.
- 4. If 9-bit transmission is desired, then set bit TX9.
- Enable the transmission by setting enable bit TXEN.
- If 9-bit transmission is selected, the ninth bit should be loaded in bit TX9D.
- Start transmission by loading data to the TXREG register.

TABLE 12-8: REGISTERS ASSOCIATED WITH SYNCHRONOUS MASTER TRANSMISSION

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
0Ch	PIR1	PSPIF ⁽¹⁾	(2)	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
18h	RCSTA	SPEN	RX9	SREN	CREN	_	FERR	OERR	RX9D	0000 -00x	0000 -00x
19h	TXREG	USART Tra	nsmit Re	egister	1		V	1.100	COM.	0000 0000	0000 0000
8Ch	PIE1	PSPIE ⁽¹⁾	(2)	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
98h	TXSTA	CSRC	TX9	TXEN	SYNC	_	BRGH	TRMT	TX9D	0000 -010	0000 -010
99h	SPBRG	Baud Rate	Generat	or Regis	ter	N	WV	111	W.Co.	0000 0000	0000 0000

Legend: x = unknown, - = unimplemented locations read as '0'. Shaded cells are not used for Synchronous Master Transmission.

Note 1: PSPIE and PSPIF are reserved on the PIC16C63/R63/66, always maintain these bits clear.

PIE1<6> and PIR1<6> are reserved, always maintain these bits clear.

FIGURE 12-12: SYNCHRONOUS TRANSMISSION

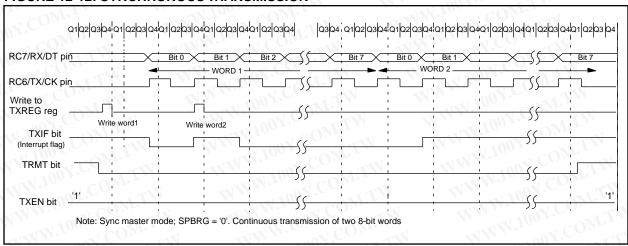
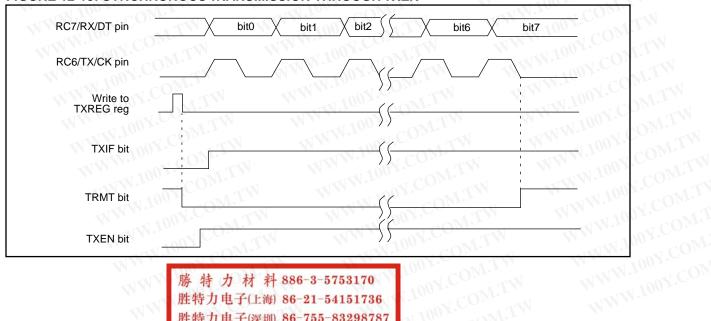


FIGURE 12-13: SYNCHRONOUS TRANSMISSION THROUGH TXEN



12.3.2 USART SYNCHRONOUS MASTER RECEPTION

Once Synchronous Mode is selected, reception is enabled by setting either enable bit SREN (RCSTA<5>) bit or enable bit CREN (RCSTA<4>). Data is sampled on the DT pin on the falling edge of the clock. If enable bit SREN is set, then only a single word is received. If enable bit CREN is set, the reception is continuous until bit CREN is cleared. If both the bits are set then bit CREN takes precedence. After clocking the last bit, the received data in the Receive Shift Register (RSR) is transferred to the RCREG register (if it is empty). When the transfer is complete, interrupt bit RCIF (PIR1<5>) is set. The actual interrupt can be enabled/disabled by setting/clearing enable bit RCIE (PIE1<5>). Flag bit RCIF is a read only bit which is reset by the hardware. In this case, it is reset when the RCREG register has been read and is empty. The RCREG is a double buffered register, i.e., it is a two deep FIFO. It is possible for two bytes of data to be received and transferred to the RCREG FIFO and a third byte to begin shifting into the RSR register. On the clocking of the last bit of the third byte, if the RCREG register is still full, then overrun error bit, OERR (RCSTA<1>) is set. The word in the RSR register will be lost. The RCREG register can be read twice to retrieve the two bytes in the FIFO. Overrun error bit OERR has to be cleared in software (by clearing bit CREN). If bit OERR is set, transfers from the RSR to the RCREG are inhibited, so it is essential to clear bit OERR if it is set. The 9th receive bit is buffered the same way as the receive data. Reading the RCREG register will load bit RX9D with a new value. Therefore it is essential for the user to read the RCSTA register before reading the RCREG register in order not to lose the old RX9D bit information.

Steps to follow when setting up Synchronous Master Reception:

- 1. Initialize the SPBRG register for the appropriate baud rate (Section 12.1).
- Enable the synchronous master serial port by setting bits SYNC, SPEN, and CSRC.
- 3. Ensure bits CREN and SREN are clear.
- If interrupts are desired, then set enable bit RCIE.
- 5. If 9-bit reception is desired, then set bit RX9.
- If a single reception is required, set enable bit SREN. For continuous reception set enable bit CREN.
- Flag bit RCIF will be set when reception is complete and an interrupt will be generated if enable bit RCIE was set.
- Read the RCSTA register to get the ninth bit (if enabled) and determine if any error occurred during reception.
- Read the 8-bit received data by reading the RCREG register.
- If any error occurred, clear the error by clearing enable bit CREN.

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TABLE 12-9: REGISTERS ASSOCIATED WITH SYNCHRONOUS MASTER RECEPTION

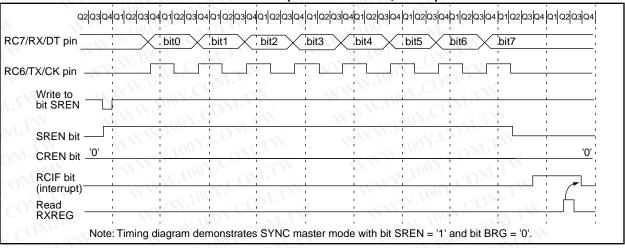
Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
0Ch	PIR1	PSPIF ⁽¹⁾	(2)	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
18h	RCSTA	SPEN	RX9	SREN	CREN	_	FERR	OERR	RX9D	0000 -00x	0000 -00x
1Ah	RCREG	USART Re	ceive Re	egister	IW		11	1.100 1.	MON.	0000 0000	0000 0000
8Ch	PIE1	PSPIE ⁽¹⁾	(2)	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
98h	TXSTA	CSRC	TX9	TXEN	SYNC	1 —	BRGH	TRMT	TX9D	0000 -010	0000 -010
99h	SPBRG	Baud Rate	General	tor Regis	ter	X	TAIN	Mir	V.CO	0000 0000	0000 0000

Legend: x = unknown, - = unimplemented locations read as '0'. Shaded cells are not used for Synchronous Master Reception.

Note 1: PSPIF and PSPIE are reserved on the PIC16C63/R63/66, always maintain these bits clear.

2: PIR1<6> and PIE1<6> are reserved, always maintain these bits clear.





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12.4 USART Synchronous Slave Mode

Applicable Devices

61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

Synchronous Slave Mode differs from Master Mode in the fact that the shift clock is supplied externally at the CK pin (instead of being supplied internally in master mode). This allows the device to transfer or receive data while in SLEEP mode. Slave mode is entered by clearing bit CSRC (TXSTA<7>).

12.4.1 USART SYNCHRONOUS SLAVE TRANSMIT

The operation of the synchronous master and slave modes are identical except in the case of the SLEEP mode.

If two words are written to the TXREG and then the SLEEP instruction is executed, the following will occur:

- The first word will immediately transfer to the TSR register and transmit.
- b) The second word will remain in TXREG register.
- c) Flag bit TXIF will not be set.
- d) When the first word has been shifted out of TSR, the TXREG register will transfer the second word to the TSR and flag bit TXIF will now be set.
- e) If enable bit TXIE is set, the interrupt will wake the chip from SLEEP and if the global interrupt is enabled, the program will branch to the interrupt vector (0004h).

Steps to follow when setting up Synchronous Slave Transmission:

- Enable the synchronous slave serial port by setting bits SYNC and SPEN, and clearing bit CSRC.
- 2. Clear bits CREN and SREN.
- If interrupts are desired, then set enable bit TXIE.
- If 9-bit transmission is desired, then set bit TX9.
- 5. Enable the transmission by setting bit TXEN.
- If 9-bit transmission is selected, the ninth bit should be loaded in bit TX9D.
- Start transmission by loading data to the TXREG register.

12.4.2 USART SYNCHRONOUS SLAVE RECEPTION

The operation of the synchronous master and slave modes is identical except in the case of the SLEEP mode. Also, enable bit SREN is a don't care in slave mode.

If receive is enabled by setting bit CREN prior to the SLEEP instruction, then a word may be received during SLEEP. On completely receiving the word, the RSR register will transfer the data to the RCREG register and if enable bit RCIE is set, the interrupt generated will wake the chip from SLEEP. If the global interrupt is enabled, the program will branch to the interrupt vector (0004h).

Steps to follow when setting up a Synchronous Slave Reception:

- Enable the synchronous master serial port by setting bits SYNC and SPEN, and clearing bit CSRC.
- If interrupts are desired, then set enable bit RCIE.
- 3. If 9-bit reception is desired, then set bit RX9.
- 4. To enable reception, set enable bit CREN.
- Flag bit RCIF will be set when reception is complete, and an interrupt will be generated if enable bit RCIE was set.
- Read the RCSTA register to get the ninth bit (if enabled) and determine if any error occurred during reception.
- Read the 8-bit received data by reading the RCREG register.
- 8. If any error occurred, clear the error by clearing enable bit CREN.

TABLE 12-10: REGISTERS ASSOCIATED WITH SYNCHRONOUS SLAVE TRANSMISSION

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
0Ch	PIR1 📢	PSPIF ⁽¹⁾	(2)	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
18h	RCSTA	SPEN	RX9	SREN	CREN	- 1	FERR	OERR	RX9D	0000 -00x	0000 -00x
19h	TXREG	USART Tra	ansmit R	egister	WT	•	MMA	100Y	COS	0000 0000	0000 0000
8Ch	PIE1	PSPIE ⁽¹⁾	(2)	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
98h	TXSTA	CSRC	TX9	TXEN	SYNC	(—	BRGH	TRMT	TX9D	0000 -010	0000 -010
99h	SPBRG	Baud Rate	Genera	tor Regist	er	N	W	Min	WY.CO	0000 0000	0000 0000

Legend: x = unknown, - = unimplemented locations read as '0'. Shaded cells are not used for Synchronous Slave Transmission.

TABLE 12-11: REGISTERS ASSOCIATED WITH SYNCHRONOUS SLAVE RECEPTION

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
0Ch	PIR1	PSPIF ⁽¹⁾	(2)	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
18h	RCSTA	SPEN	RX9	SREN	CREN		FERR	OERR	RX9D	0000 -00x	0000 -00x
1Ah	RCREG	USART Re	ceive Re	egister	100	Y.Co.	WILL		MAN	0000 0000	0000 0000
8Ch	PIE1	PSPIE ⁽¹⁾	(2)	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
98h	TXSTA	CSRC	TX9	TXEN	SYNC	. √.C	BRGH	TRMT	TX9D	0000 -010	0000 -010
99h	SPBRG	Baud Rate	Genera	tor Regis	ter	- 01	OM		WV	0000 0000	0000 0000

Legend: x = unknown, - = unimplemented locations read as '0'. Shaded cells are not used for Synchronous Slave Reception.

Note 1: PSPIF and PSPIE are reserved on the PIC16C63/R63/66, always maintain these bits clear.

^{2:} PIR1<6> and PIE1<6> are reserved, always maintain these bits clear.

Note 1: PSPIF and PSPIE are reserved on the PIC16C63/R63/66, always maintain these bits clear.

^{2:} PIR1<6> and PIE1<6> are reserved, always maintain these bits clear.

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NOTES:

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13.0 SPECIAL FEATURES OF THE CPU

Applicable Devices

61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

What sets a microcontroller apart from other processors are special circuits to deal with the needs of real-time applications. The PIC16CXX family has a host of such features intended to maximize system reliability, minimize cost through elimination of external components, provide power saving operating modes and offer code protection. These are:

- Oscillator selection
- Reset
 - Power-on Reset (POR)
 - Power-up Timer (PWRT)
 - Oscillator Start-up Timer (OST)
 - Brown-out Reset (BOR)
- Interrupts
- Watchdog Timer (WDT)
- SLEEP mode
- · Code protection
- ID locations
- · In-circuit serial programming

The PIC16CXX has a Watchdog Timer which can be shut off only through configuration bits. It runs off its own RC oscillator for added reliability. There are two

timers that offer necessary delays on power-up. One is the Oscillator Start-up Timer (OST), intended to keep the chip in RESET until the crystal oscillator is stable. The other is the Power-up Timer (PWRT), which provides a fixed delay of 72 ms (nominal) on power-up only, designed to keep the part in reset while the power supply stabilizes. With these two timers on-chip, most applications need no external reset circuitry.

SLEEP mode is designed to offer a very low current power-down mode. The user can wake from SLEEP through external reset, Watchdog Timer Wake-up or through an interrupt. Several oscillator options are also made available to allow the part to fit the application. The RC oscillator option saves system cost while the LP crystal option saves power. A set of configuration bits are used to select various options.

13.1 Configuration Bits

Applicable Devices

61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

The configuration bits can be programmed (read as '0') or left unprogrammed (read as '1') to select various device configurations. These bits are mapped in program memory location 2007h.

The user will note that address 2007h is beyond the user program memory space. In fact, it belongs to the special test/configuration memory space (2000h - 3FFFh), which can be accessed only during programming.

FIGURE 13-1: CONFIGURATION WORD FOR PIC16C61



FIGURE 13-2: CONFIGURATION WORD FOR PIC16C62/64/65

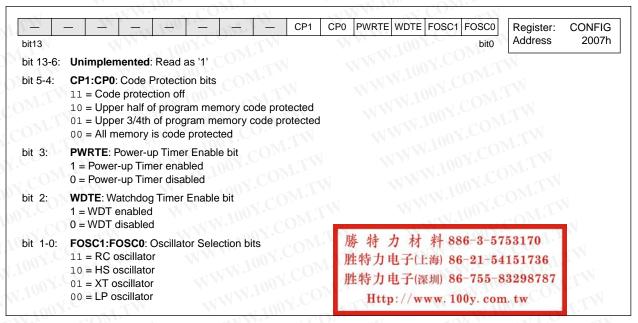
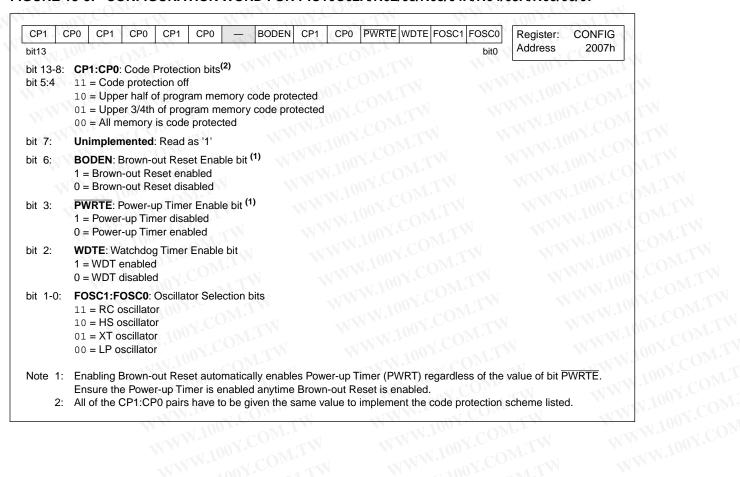


FIGURE 13-3: CONFIGURATION WORD FOR PIC16C62A/R62/63/R63/64A/R64/65A/R65/66/67



13.2 Oscillator Configurations

Applicable Devices
61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

13.2.1 OSCILLATOR TYPES

The PIC16CXX can be operated in four different oscillator modes. The user can program two configuration bits (FOSC1 and FOSC0) to select one of these four modes:

LP Low Power CrystalXT Crystal/Resonator

HS High Speed Crystal/Resonator

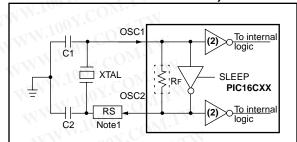
RC Resistor/Capacitor

13.2.2 CRYSTAL OSCILLATOR/CERAMIC RESONATORS

In LP, XT, or HS modes a crystal or ceramic resonator is connected to the OSC1/CLKIN and OSC2/CLKOUT pins to establish oscillation (Figure 13-4). The PIC16CXX oscillator design requires the use of a parallel cut crystal. Use of a series cut crystal may give a frequency out of the crystal manufacturers specifications. When in LP, XT, or HS modes, the device can have an external clock source to drive the OSC1/CLKIN pin (Figure 13-5).

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FIGURE 13-4: CRYSTAL/CERAMIC
RESONATOR OPERATION
(HS, XT OR LP OSC
CONFIGURATION)



See Table 13-1, Table 13-3, Table 13-2 and Table 13-4 for recommended values of C1 and C2.

- Note 1: A series resistor may be required for AT strip cut crystals.
 - For the PIC16C61 the buffer is on the OSC2 pin, all other devices have the buffer on the OSC1 pin.

FIGURE 13-5: EXTERNAL CLOCK INPUT OPERATION (HS, XT OR LP OSC CONFIGURATION)

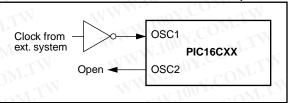


TABLE 13-1: CERAMIC RESONATORS PIC16C61

Ranges T	ested:	N.Ing. C.	OMIT
Mode	Freq	OSC1	OSC2
XT.	455 kHz 2.0 MHz 4.0 MHz	47 - 100 pF 15 - 68 pF 15 - 68 pF	47 - 100 pF 15 - 68 pF 15 - 68 pF
HS	8.0 MHz 16.0 MHz	15 - 68 pF 10 - 47 pF	15 - 68 pF 10 - 47 pF
not	ese values are for es at bottom of p		nce only. See
Resonato	rs Used:	N Y	1001.
455 kHz	Panasonic EF	O-A455K04B	± 0.3%
2.0 MHz	Murata Erie C	SA2.00MG	± 0.5%
4.0 MHz	Murata Erie C	SA4.00MG	± 0.5%
8.0 MHz	Murata Erie C	SA8.00MT	± 0.5%
16.0 MHz	Murata Erie C	SA16.00MX	± 0.5%
All res	onators used did	not have built-in	capacitors.

TABLE 13-2: CERAMIC RESONATORS PIC16C62/62A/R62/63/R63/64/ 64A/R64/65/65A/R65/66/67

Ranges Tested:								
Mode	Freq	OSC1	OSC2					
XT	455 kHz 2.0 MHz 4.0 MHz	68 - 100 pF 15 - 68 pF 15 - 68 pF	68 - 100 pF 15 - 68 pF 15 - 68 pF					
HS	8.0 MHz 16.0 MHz	10 - 68 pF 10 - 22 pF	10 - 68 pF 10 - 22 pF					
not	es at bottom of	for design guida page.	nce only. See					
Resonato	rs Usea:	COMP	1					
455 kHz	Panasonic I	EFO-A455K04B	± 0.3%					
2.0 MHz	Murata Erie	CSA2.00MG	± 0.5%					
4.0 MHz	Murata Erie	CSA4.00MG	± 0.5%					
8.0 MHz	Murata Erie	CSA8.00MT	± 0.5%					
16.0 MHz	Murata Erie	CSA16.00MX	± 0.5%					
All res	onators used d	lid not have built-in	capacitors.					

TABLE 13-3: CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR FOR PIC16C61

Mode	Freq	OSC1	OSC2
LP	32 kHz	33 - 68 pF	33 - 68 pF
	200 kHz	15 - 47 pF	15 - 47 pF
XT	100 kHz	47 - 100 pF	47 - 100 pF
	500 kHz	20 - 68 pF	20 - 68 pF
	1 MHz	15 - 68 pF	15 - 68 pF
	2 MHz	15 - 47 pF	15 - 47 pF
	4 MHz	15 - 33 pF	15 - 33 pF
HS <	8 MHz	15 - 47 pF	15 - 47 pF
	20 MHz	15 - 47 pF	15 - 47 pF

TABLE 13-4: CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR FOR PIC16C62/62A/R62/63/ R63/64/64A/R64/65/65A/R65/ 66/67

Osc Type	Crystal Freq	Cap. Range C1	Cap. Range C2
LP	32 kHz	33 pF	33 pF
	200 kHz	15 pF	15 pF
XT	200 kHz	47-68 pF	47-68 pF
	1 MHz	15 pF	15 pF
	4 MHz	15 pF	15 pF
HS	4 MHz	15 pF	15 pF
	8 MHz	15-33 pF	15-33 pF
	20 MHz	15-33 pF	15-33 pF
	se values are f	or design guidand page.	e only. See
100	Crys	tals Used	11.100
32 kHz	Epson C-00	1R32.768K-A	± 20 PPM
200 kHz	STD XTL 20	00.000KHz	± 20 PPM
1 MHz	ECS ECS-1	0-13-1	± 50 PPM
4 MHz	ECS ECS-4	0-20-1	± 50 PPM
8 MHz	EPSON CA	-301 8.000M-C	± 30 PPM
20 MHz	EPSON CA	-301 20.000M-C	± 30 PPM

- Note 1: Recommended values of C1 and C2 are identical to the ranges tested Table 13-1 and Table 13-2.
 - 2: Higher capacitance increases the stability of oscillator but also increases the start-up time.
 - 3: Since each resonator/crystal has its own characteristics, the user should consult the resonator/crystal manufacturer for appropriate values of external components.
 - 4: Rs may be required in HS mode as well as XT mode to avoid overdriving crystals with low drive level specification.

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13.2.3 EXTERNAL CRYSTAL OSCILLATOR CIRCUIT

Either a prepackaged oscillator can be used or a simple oscillator circuit with TTL gates can be built. Prepackaged oscillators provide a wide operating range and better stability. A well-designed crystal oscillator will provide good performance with TTL gates. Two types of crystal oscillator circuits can be used; one with series resonance, or one with parallel resonance.

Figure 13-6 shows implementation of a parallel resonant oscillator circuit. The circuit is designed to use the fundamental frequency of the crystal. The 74AS04 inverter performs the 180-degree phase shift that a parallel oscillator requires. The 4.7 k Ω resistor provides the negative feedback for stability. The 10 k Ω potentiometer biases the 74AS04 in the linear region. This could be used for external oscillator designs.

FIGURE 13-6: EXTERNAL PARALLEL RESONANT CRYSTAL OSCILLATOR CIRCUIT

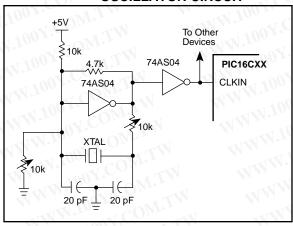
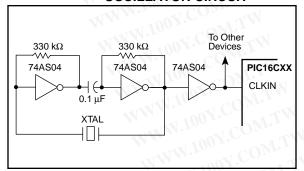


Figure 13-7 shows a series resonant oscillator circuit. This circuit is also designed to use the fundamental frequency of the crystal. The inverter performs a 180-degree phase shift in a series resonant oscillator circuit. The 330 k Ω resistors provide the negative feedback to bias the inverters in their linear region.

FIGURE 13-7: EXTERNAL SERIES
RESONANT CRYSTAL
OSCILLATOR CIRCUIT



13.2.4 RC OSCILLATOR

For timing insensitive applications the RC device option offers additional cost savings. The RC oscillator frequency is a function of the supply voltage, the resistor (Rext) and capacitor (Cext) values, and the operating temperature. In addition to this, the oscillator frequency will vary from unit to unit due to normal process parameter variation. Furthermore, the difference in lead frame capacitance between package types will also affect the oscillation frequency, especially for low Cext values. The user also needs to take into account variation due to tolerance of external R and C components used. Figure 13-8 shows how the RC combination is connected to the PIC16CXX. For Rext values below $2.2 \text{ k}\Omega$, the oscillator operation may become unstable or stop completely. For very high Rext values (e.g. 1 M Ω), the oscillator becomes sensitive to noise, humidity and leakage. Thus, we recommend keeping Rext between 3 k Ω and 100 k Ω .

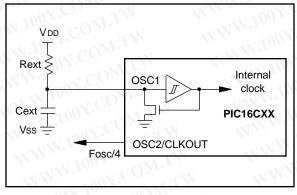
Although the oscillator will operate with no external capacitor (Cext = 0 pF), we recommend using values above 20 pF for noise and stability reasons. With no or small external capacitance, the oscillation frequency can vary dramatically due to changes in external capacitances, such as PCB trace capacitance or package lead frame capacitance.

See characterization data for desired device for RC frequency variation from part to part due to normal process variation. The variation is larger for larger R (since leakage current variation will affect RC frequency more for large R) and for smaller C (since variation of input capacitance will affect RC frequency more).

See characterization data for desired device for variation of oscillator frequency due to VDD for given Rext/ Cext values as well as frequency variation due to operating temperature for given R, C, and VDD values.

The oscillator frequency, divided by 4, is available on the OSC2/CLKOUT pin, and can be used for test purposes or to synchronize other logic (see Figure 3-5 for waveform).

FIGURE 13-8: RC OSCILLATOR MODE



PIC16C6X

13.3 Reset

Applicable Devices

61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

The PIC16CXX differentiates between various kinds of reset:

- Power-on Reset (POR)
- MCLR reset during normal operation
- MCLR reset during SLEEP
- WDT Reset (normal operation)
- Brown-out Reset (BOR) Not on PIC16C61/62/

Some registers are not affected in any reset condition, their status is unknown on POR and unchanged in any other reset. Most other registers are reset to a "reset state" on Power-on Reset (POR), on MCLR or WDT Reset, on MCLR reset during SLEEP, and on Brownout Reset (BOR). They are not affected by a WDT Wake-up, which is viewed as the resumption of normal operation.

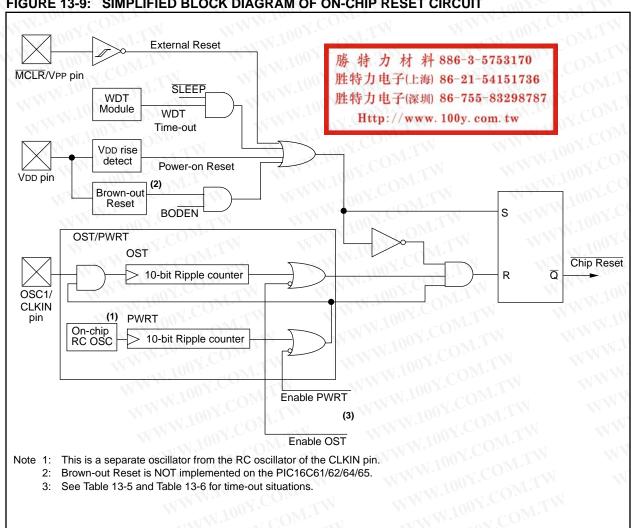
The TO and PD bits are set or cleared differently in different reset situations as indicated in Table 13-7, Table 13-8, and Table 13-9. These bits are used in software to determine the nature of the reset. See Table 13-12 for a full description of reset states of all registers.

A simplified block diagram of the on-chip reset circuit is shown in Figure 13-9.

On the PIC16C62A/R62/63/R63/64A/R64/65A/R65/ 66/67, the MCLR reset path has a noise filter to detect and ignore small pulses. See parameter #34 for pulse width specifications.

It should be noted that a WDT Reset does not drive the MCLR pin low.

FIGURE 13-9: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT



13.4 Power-on Reset (POR), Power-up Timer (PWRT), Oscillator Start-up Timer (OST) and Brown-out Reset (BOR)

Applicable Devices
61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

13.4.1 POWER-ON RESET (POR)

A Power-on Reset pulse is generated on-chip when VDD rise is detected (in the range of 1.5V - 2.1V). To take advantage of the POR, just tie the MCLR/VPP pin directly (or through a resistor) to VDD. This will eliminate external RC components usually needed to create a Power-on Reset. A maximum rise time for VDD is required. See Electrical Specifications for details.

When the device starts normal operation (exits the reset condition), device operating parameters (voltage, frequency, temperature, ...) must be met to ensure operation. If these conditions are not met, the device must be held in reset until the operating conditions are met. Brown-out Reset may be used to meet the startup conditions.

For additional information, refer to Application Note AN607, "Power-up Trouble Shooting."

13.4.2 POWER-UP TIMER (PWRT)

The Power-up Timer provides a fixed 72 ms nominal time-out on power-up only, from POR. The Power-up Timer operates on an internal RC oscillator. The chip is kept in reset as long as PWRT is active. The PWRT's time delay allows VDD to rise to an acceptable level. A configuration bit is provided to enable/disable the PWRT.

The power-up time delay will vary from chip to chip due to VDD, temperature, and process variation. See DC parameters for details.

13.4.3 OSCILLATOR START-UP TIMER (OST)

The Oscillator Start-up Timer (OST) provides 1024 oscillator cycle (from OSC1 input) delay after the PWRT delay is over. This ensures the crystal oscillator or resonator has started and stabilized.

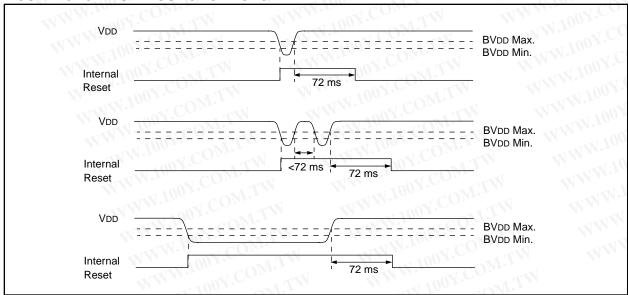
The OST time-out is invoked only for XT, LP and HS modes and only on Power-on Reset or wake-up from SLEEP.

13.4.4 BROWN-OUT RESET (BOR)

Applicable Devices
61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

A configuration bit, BODEN, can disable (if clear/programmed) or enable (if set) the Brown-out Reset circuitry. If VDD falls below 4.0V (parameter D005 in Electrical Specification section) for greater than parameter #34 (see Electrical Specification section), the brown-out situation will reset the chip. A reset may not occur if VDD falls below 4.0V for less than parameter #34. The chip will remain in Brown-out Reset until VDD rises above BVDD. The Power-up Timer will now be invoked and will keep the chip in RESET an additional 72 ms. If VDD drops below BVDD while the Power-up Timer is running, the chip will go back into a Brown-out Reset and the Power-up Timer will be initialized. Once VDD rises above BVDD, the Power-up Timer will execute a 72 ms time delay. The Power-up Timer should always be enabled when Brown-out Reset is enabled. Figure 13-10 shows typical brown-out situations.

FIGURE 13-10: BROWN-OUT SITUATIONS



13.4.5 TIME-OUT SEQUENCE

On power-up the time-out sequence is as follows: First a PWRT time-out is invoked after the POR time delay has expired. Then OST is activated. The total time-out will vary based on oscillator configuration and the status of the PWRT. For example, in RC mode, with the PWRT disabled, there will be no time-out at all. Figure 13-11, Figure 13-12, and Figure 13-13 depict time-out sequences on power-up.

Since the time-outs occur from the POR pulse, if the \overline{MCLR}/VPP pin is kept low long enough, the time-outs will expire. Then bringing the \overline{MCLR}/VPP pin high will begin execution immediately (Figure 13-14). This is useful for testing purposes or to synchronize more than one PIC16CXX device operating in parallel.

Table 13-10 and Table 13-11 show the reset conditions for some special function registers, while Table 13-12 shows the reset conditions for all the registers.

13.4.6 POWER CONTROL/STATUS REGISTER (PCON)

Applicable Devices 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

The Power Control/Status Register, PCON has up to two bits, depending upon the device. Bit0 is not implemented on the PIC16C62/64/65.

Bit0 is BOR (Brown-out Reset Status bit). BOR is unknown on Power-on Reset. It must then be set by the user and checked on subsequent resets to see if BOR cleared, indicating that a brown-out has occurred. The BOR status bit is a "Don't Care" and is not necessarily predictable if the Brown-out Reset circuitry is disabled (by clearing bit BODEN in the Configuration Word).

Bit1 is POR (Power-on Reset Status bit). It is cleared on a Power-on Reset and unaffected otherwise. The user must set this bit following a Power-on Reset.

TABLE 13-5: TIME-OUT IN VARIOUS SITUATIONS, PIC16C61/62/64/65

Oscillator Configuration	Powe	Wake-up from SLEEP			
TW. TW	PWRTE = 1	PWRTE = 0	1001. OM.TV		
XT, HS, LP	72 ms + 1024Tosc	1024Tosc	1024 Tosc		
RC)	72 ms	OM	MINN. PO T. COM.		

TABLE 13-6: TIME-OUT IN VARIOUS SITUATIONS, PIC16C62A/R62/63/R63/64A/R64/65A/R65/66/67

Ossillatan Canfinunation	Power-	up ()	Lu - M.	Wake up from		
Oscillator Configuration	PWRTE = 0	PWRTE = 1	Brown-out	SLEEP		
XT, HS, LP	72 ms + 1024Tosc	1024Tosc	72 ms + 1024Tosc	1024 Tosc		
RC	72 ms	11 10 <u>0</u>	72 ms	M.100		

TABLE 13-7: STATUS BITS AND THEIR SIGNIFICANCE, PIC16C61

TO	PD	OW.I.A. WANN.IOO TOW.I	MWW.IOOV.C
1	100	Power-on Reset or MCLR reset during normal operation	1 100 z
0	1,00	WDT Reset	W 1 100 x
0	0	WDT Wake-up	11/1/
1	0.100	MCLR reset during SLEEP or interrupt wake-up from SLEEP	WWW.

TABLE 13-8: STATUS BITS AND THEIR SIGNIFICANCE, PIC16C62/64/65

POR	TO	PD	ON TW WWW.TOOX.COM.TW
0	1	1 1	Power-on Reset
0	0	x	Illegal, TO is set on a Power-on Reset
0	х	0	Illegal, PD is set on a Power-on Reset
1	0	1	WDT Reset
1	0	0	WDT Wake-up
1	u	u	MCLR reset during normal operation
1	1	0	MCLR reset during SLEEP or interrupt wake-up from SLEEP

Legend: x = unknown, u = unchanged

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TABLE 13-9: STATUS BITS AND THEIR SIGNIFICANCE FOR PIC16C62A/R62/63/R63/64A/R64/65A/R65/66/67

POR	BOR	TO	PD	WWW.Ioo COM.
0	x	1_0	1,	Power-on Reset
0	х	0 0	x	Illegal, TO is set on a Power-on Reset
0	х	x	0	Illegal, PD is set on a Power-on Reset
1	0	x	x	Brown-out Reset
1	1	0	1	WDT Reset
111	1	0 0 7	0	WDT Wake-up
0 1	1	u	Cu	MCLR reset during normal operation
	1	1	- 00	MCLR reset during SLEEP or interrupt wake-up from SLEEP

Legend: x = unknown, u = unchanged

TABLE 13-10: RESET CONDITION FOR SPECIAL REGISTERS ON PIC16C61/62/64/65

Program Counter	STATUS	PCON ⁽²⁾
000h	0001 1xxx	0-
000h	000u uuuu	u-
000h	0001 0uuu	u-
000h	0000 1uuu	COu-
PC + 1	uuu0 0uuu	u-
PC + 1 ⁽¹⁾	uuu1 0uuu	u-
	000h 000h 000h 000h PC + 1	000h 0001 1xxx 000h 000u uuuu 000h 0001 0uuu 000h 0000 1uuu PC + 1 uuu0 0uuu

Legend: u = unchanged, x = unknown, - = unimplemented bit read as '0'.

Note 1: When the wake-up is due to an interrupt and the global enable bit, GIE is set, the PC is loaded with the interrupt vector (0004h) after execution of PC+1.

TABLE 13-11: RESET CONDITION FOR SPECIAL REGISTERS ON PIC16C62A/R62/63/R63/64A/R64/65A/R65/66/67

2: The PCON register is not implemente TABLE 13-11: RESET CONDITION FOR	ed on the PIC16C61.	SON	
PIC16C62A/R62/63/R63/6			PCON
Power-on Reset	000h	0001 1xxx	0x
MCLR reset during normal operation	000h	000u uuuu	uu
MCLR reset during SLEEP	000h	0001 0uuu	uu
WDT Reset	000h	0000 1uuu	uu
Brown-out Reset	000h	0001 luuu	u0
WDT Wake-up	PC + 1	uuu0 0uuu	uu
Interrupt wake-up from SLEEP	PC + 1 ⁽¹⁾	uuu1 0uuu	uu

Legend: u = unchanged, x = unknown, - = unimplemented bit read as '0'.

Note 1: When the wake-up is due to an interrupt and global enable bit, GIE is set, the PC is loaded with the interrupt vector (0004h) after execution of PC+1.

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TABLE 13-12: INITIALIZATION CONDITIONS FOR ALL REGISTERS

Register	WWW.Ap		Appli	cab	le De	evices	IV T	I N		N	N	Power-on Reset Brown-out Reset	MCLR Reset during: - normal operation - SLEEP WDT Reset	Wake-up via interrupt or WDT Wake-up			
W	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	xxxx xxxx	uuuu uuuu	uuuu uuuu
INDF	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	N/A	N/A	N/A
TMR0	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	xxxx xxxx	uuuu uuuu	uuuu uuuu
PCL	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	0000h	0000h	PC + 1(2)
STATUS	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	0001 1xxx	000q quuu(3)	uuuq quuu(3)
FSR	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	xxxx xxxx	uuuu uuuu	uuuu uuuu
DODE O	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	x xxxx	u uuuu	u uuuu
PORTA	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	xx xxxx	uu uuuu	uu uuuu
PORTB	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTC	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTD	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTE	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	xxx	uuu	uuu
PCLATH	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	0 0000	0 0000	u uuuu
INTCON	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	0000 000x	0000 000u	uuuu uuuu(1)
PIR1	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	00 0000	00 0000	uu uuuu(1)
	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	0000 0000	0000 0000	uuuu uuuu(1)
PIR2	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	0	0	(2)
TMR1L	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	xxxx xxxx	uuuu uuuu	uuuu uuuu
TMR1H	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	xxxx xxxx	uuuu uuuu	uuuu uuuu
T1CON	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	00 0000	uu uuuu	uu uuuu
TMR2	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	0000 0000	0000 0000	uuuu uuuu
T2CON	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	-000 0000	-000 0000	-uuu uuuu
SSPBUF	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	xxxx xxxx	uuuu uuuu	uuuu uuuu
SSPCON	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	0000 0000	0000 0000	uuuu uuuu
CCPR1L	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCPR1H	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCP1CON	61		62A	4.0		0		64A				R65			00 0000	00 0000	uu uuuu
RCSTA	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	0000 -00x	0000 -00x	uuuu -uuu
TXREG	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	0000 0000	0000 0000	uuuu uuuu
RCREG	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	0000 0000	0000 0000	uuuu uuuu
CCPR2L	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCPR2H	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCP2CON	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	0000 0000	0000 0000	uuuu uuuu
OPTION	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	1111 1111	1111 1111	uuuu uuuu
TRISA						4	W	64A		MIT					1 1111	1 1111	u uuuu
	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	11 1111	11 1111	uu uuuu
TRISB	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	1111 1111	1111 1111	uuuu uuuu

Legend: u = unchanged, x = unknown, -= unimplemented bit read as '0', q = value depends on condition.

Note 1: One or more bits in INTCON, PIR1 and/or PIR2 will be affected (to cause wake-up).

^{2:} When the wake-up is due to an interrupt and the global enable bit, GIE is set, the PC is loaded with the interrupt vector (0004h) after execution of PC + 1.

^{3:} See Table 13-10 and Table 13-11 for reset value for specific conditions.

TABLE 13-12: INITIALIZATION CONDITIONS FOR ALL REGISTERS (Cont.'d)

Register	*				05	Appli	icab	le De	evice	S				4	Power-or Brown Res	n-out	MCLR Res – normal of – SLEEP	U	Wake-up via interrupt or WDT Wake-up
- 1			- TXN	W.	100	×7 (cC	M.)	ĸ.T				W	. 10	$^{\Gamma}CO_{D}$	WDT Rese	t	
TRISC	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	1111	1111	1111	1111	uuuu uuuu
TRISD	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	1111	1111	1111	1111	uuuu uuuu
TRISE	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	0000	-111	0000	-111	uuuu -uuu
PIE1	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	00	0000	00	0000	uu uuuu
$O_{M',T,\lambda}$	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	0000	0000	0000	0000	uuuu uuuu
PIE2	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	ZZTVÍ	0	. COA	0	u
PCON	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	W	0u		uu	uu
PCON	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	ALM.	0-	7	u-	u-
PR2	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	1111	1111	1111	1111	1111 1111
SSPADD	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	0000	0000	0000	0000	uuuu uuuu
SSPSTAT	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	00	0000	00	0000	uu uuuu
TXSTA	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	0000	-010	0000	-010	uuuu -uuu
SPBRG	61	62	62A	R62	63	R63	64	64A	R64	65	65A	R65	66	67	0000	0000	0000	0000	uuuu uuuu

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Legend: u = unchanged, x = unknown, -= unimplemented bit read as '0', q = value depends on condition.

- Note 1: One or more bits in INTCON, PIR1 and/or PIR2 will be affected (to cause wake-up).
 - When the wake-up is due to an interrupt and the global enable bit, GIE is set, the PC is loaded with the interrupt vector (0004h) after execution of PC + 1.
 - See Table 13-10 and Table 13-11 for reset value for specific conditions.

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FIGURE 13-11: TIME-OUT SEQUENCE ON POWER-UP (MCLR NOT TIED TO VDD): CASE 1

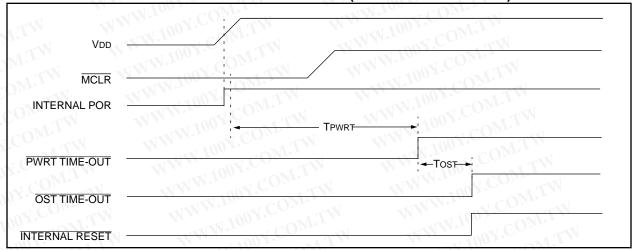


FIGURE 13-12: TIME-OUT SEQUENCE ON POWER-UP (MCLR NOT TIED TO VDD): CASE 2

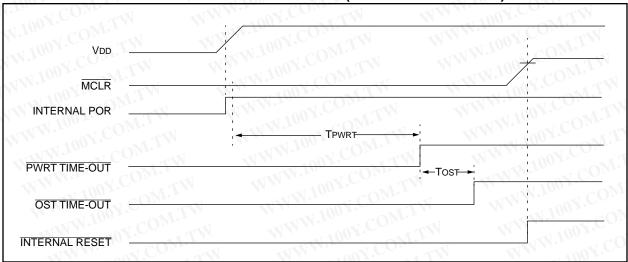


FIGURE 13-13: TIME-OUT SEQUENCE ON POWER-UP (MCLR TIED TO VDD)

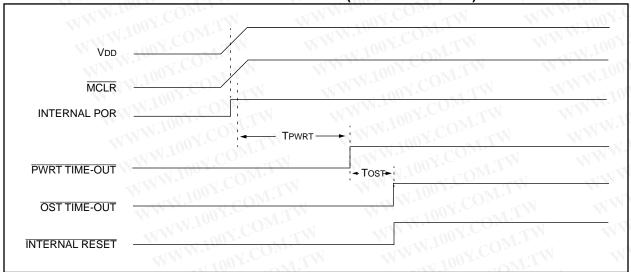
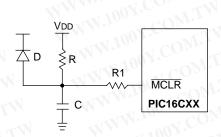


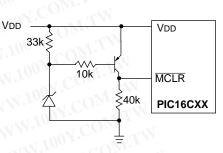
FIGURE 13-14: EXTERNAL POWER-ON RESET CIRCUIT (FOR SLOW VDD POWER-UP)



- Note 1: External Power-on Reset circuit is required only if VDD power-up slope is too slow. The diode D helps discharge the capacitor quickly when VDD powers down.
 - 2: $R < 40 \text{ k}\Omega$ is recommended to make sure that voltage drop across R does not violate the devices electrical specifications.
 - 3: $R1 = 100\Omega$ to 1 $k\Omega$ will limit any current flowing into \overline{MCLR} from external capacitor C in the event of \overline{MCLR} /VPP pin breakdown due to Electrostatic Discharge (ESD) or Electrostatic Overstress (EOS).

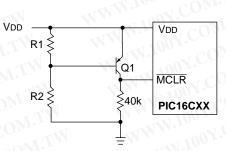
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FIGURE 13-15: EXTERNAL BROWN-OUT PROTECTION CIRCUIT 1



- Note 1: This circuit will activate reset when VDD goes below (Vz + 0.7V) where Vz = Zener voltage.
 - Internal brown-out detection on the PIC16C62A/R62/63/R63/64A/R64/65A/ R65/66/67 should be disabled when using this circuit.
 - Resistors should be adjusted for the characteristics of the transistors.

FIGURE 13-16: EXTERNAL BROWN-OUT PROTECTION CIRCUIT 2



Note 1: This brown-out circuit is less expensive, albeit less accurate. Transistor Q1 turns off when VDD is below a certain level such that:

$$V_{DD} \bullet \frac{R1}{R1 + R2} = 0.7V$$

- Internal brown-out detection on the PIC16C62A/R62/63/R63/64A/R64/65A/ R65/66/67 should be disabled when using this circuit.
- Resistors should be adjusted for the characteristics of the transistors.

13.5 Interrupts

Applicable Devices

61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

The PIC16C6X family has up to 11 sources of interrupt. The interrupt control register (INTCON) records individual interrupt requests in flag bits. It also has individual and global interrupt enable bits.

Note: Individual interrupt flag bits are set regardless of the status of their corresponding mask bit or global enable bit, GIE.

Global interrupt enable bit, GIE (INTCON<7>) enables (if set) all un-masked interrupts or disables (if cleared) all interrupts. When bit GIE is enabled, and an interrupt flag bit and mask bit are set, the interrupt will vector immediately. Individual interrupts can be disabled through their corresponding enable bits in the INTCON register. GIE is cleared on reset.

The "return from interrupt" instruction, RETFIE, exits the interrupt routine as well as sets the GIE bit, which re-enable interrupts.

The RB0/INT pin interrupt, the RB port change interrupt and the TMR0 overflow interrupt flag bits are contained in the INTCON register.

The peripheral interrupt flag bits are contained in special function registers PIR1 and PIR2. The corresponding interrupt enable bits are contained in special function registers PIE1 and PIE2 and the peripheral interrupt enable bit is contained in special function register INTCON.

When an interrupt is responded to, bit GIE is cleared to disable any further interrupts, the return address is pushed onto the stack and the PC is loaded with 0004h. Once in the interrupt service routine the source(s) of the interrupt can be determined by polling the interrupt flag bits. The interrupt flag bit(s) must be cleared in software before re-enabling interrupts to avoid recursive interrupts.

For external interrupt events, such as the RB0/INT pin or RB port change interrupt, the interrupt latency will be three or four instruction cycles. The exact latency depends when the interrupt event occurs (Figure 13-19). The latency is the same for one or two cycle instructions. Once in the interrupt service routine the source(s) of the interrupt can be determined by polling the interrupt flag bits. The interrupt flag bit(s) must be cleared in software before re-enabling interrupts to

avoid infinite interrupt requests. Individual interrupt flag bits are set regardless of the status of their corresponding mask bit or the GIE bit.

Note:

For the PIC16C61/62/64/65, if an interrupt occurs while the Global Interrupt Enable bit, GIE is being cleared, bit GIE may unintentionally be re-enabled by the user's Interrupt Service Routine (the RETFIE instruction). The events that would cause this to occur are:

- An instruction clears the GIE bit while an interrupt is acknowledged
- The program branches to the Interrupt vector and executes the Interrupt Service Routine.
- The Interrupt Service Routine completes with the execution of the RET-FIE instruction. This causes the GIE bit to be set (enables interrupts), and the program returns to the instruction after the one which was meant to disable interrupts.
- 4. Perform the following to ensure that interrupts are globally disabled.

LOOP BCF INTCON,GIE

BTFSC INTCON,GIE

GOTO LOOP

;Disable Global ;Interrupt bit ;Global Interrupt ;Disabled? ;NO, try again ;Yes, continue ;with program flow

FIGURE 13-17: INTERRUPT LOGIC FOR PIC16C61

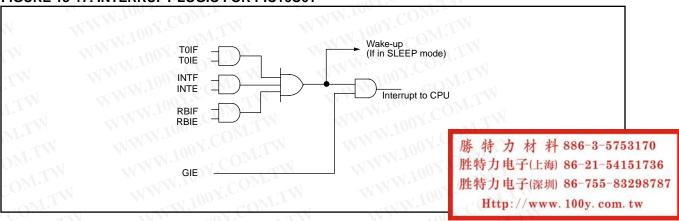
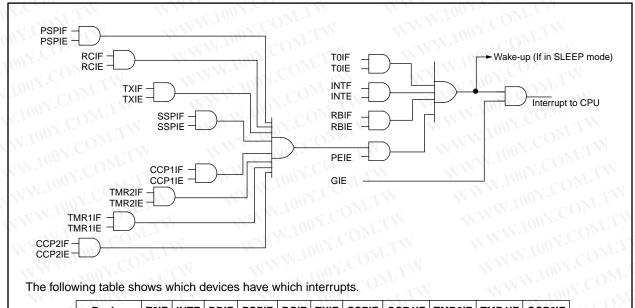


FIGURE 13-18: INTERRUPT LOGIC FOR PIC16C6X



The following table shows which devices have which interrupts.

Device	TOIF	INTF	RBIF	PSPIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	CCP2IF
PIC16C62	Yes	Yes	Yes	-	- T	Nin	Yes	Yes	Yes	Yes	MAIN
PIC16C62A	Yes	Yes	Yes	-		1.1	Yes	Yes	Yes	Yes	M-W.
PIC16CR62	Yes	Yes	Yes	-	17		Yes	Yes	Yes	Yes	-757
PIC16C63	Yes	Yes	Yes	-	Yes	Yes	Yes	Yes	Yes	Yes	Yes
PIC16CR63	Yes	Yes	Yes	кт -	Yes	Yes	Yes	Yes	Yes	Yes	Yes
PIC16C64	Yes	Yes	Yes	Yes	- 1		Yes	Yes	Yes	Yes	
PIC16C64A	Yes	Yes	Yes	Yes	-	MIN	Yes	Yes	Yes	Yes	- IN
PIC16C64	Yes	Yes	Yes	Yes	-	<-IV	Yes	Yes	Yes	Yes	-01
PIC16C65	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
PIC16C65A	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
PIC16CR65	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
PIC16C66	Yes	Yes	Yes	Nr.	Yes	Yes	Yes	Yes	Yes	Yes	Yes
PIC16C67	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes

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INT INTERRUPT 13.5.1

External interrupt on RB0/INT pin is edge triggered: either rising if edge select bit INTEDG (OPTION<6>) is set, or falling, if bit INTEDG is clear. When a valid edge appears on the RB0/INT pin, flag bit INTF (INTCON<1>) is set. This interrupt can be disabled by clearing enable bit INTE (INTCON<4>). The INTF bit must be cleared in software in the interrupt service routine before re-enabling this interrupt. The INT interrupt can wake the processor from SLEEP, if enable bit INTE was set prior to going into SLEEP. The status of global enable bit GIE decides whether or not the processor branches to the interrupt vector following wake-up. See Section 13.8 for details on SLEEP mode.

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13.5.2 TMR0 INTERRUPT

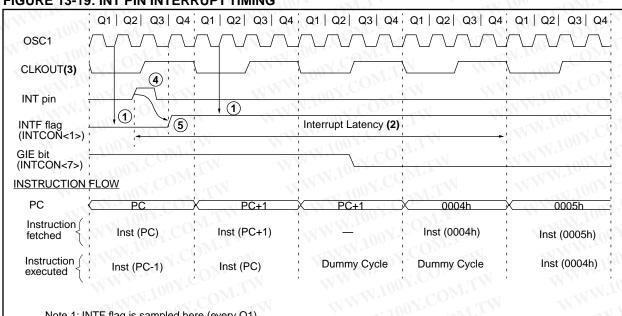
An overflow (FFh \rightarrow 00h) in the TMR0 register will set flag bit T0IF (INTCON<2>). The interrupt can be enabled/disabled by setting/clearing enable bit T0IE (INTCON<5>) (Section 7.0).

13.5.3 PORTB INTERRUPT ON CHANGE

An input change on PORTB<7:4> sets flag bit RBIF (INTCON<0>). The interrupt can be enabled/disabled by setting/clearing enable bit RBIE (INTCON<4>) (Section 5.2).

For the PIC16C61/62/64/65, if a change on Note: the I/O pin should occur when the read operation is being executed (start of the Q2 cycle), then flag bit RBIF may not get set.

FIGURE 13-19: INT PIN INTERRUPT TIMING



Note 1: INTF flag is sampled here (every Q1).

- 2: Interrupt latency = 3TCY for synchronous interrupt and 3-4TCY for asynchronous interrupt. Latency is the same whether Inst (PC) is a single cycle or a 2-cycle instruction.
- 3: CLKOUT is available only in RC oscillator mode.
- 4: For minimum width spec of INT pulse, refer to AC specs.
- 5: INTF can to be set anytime during the Q4-Q1 cycles.

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13.6 Context Saving During Interrupts

Applicable Devices

61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

During an interrupt, only the return PC value is saved on the stack. Typically, users may wish to save key registers during an interrupt i.e., W register and STATUS register. This will have to be implemented in software.

Example 13-1 stores and restores the STATUS and W registers. Example 13-2 stores and restores the STATUS, W, and PCLATH registers (Devices with paged program memory). For all PIC16C6X devices with greater than 1K of program memory (all devices except PIC16C61), the register, W_TEMP, must be

defined in all banks and must be defined at the same offset from the bank base address (i.e., if W_TEMP is defined at 0x20 in bank 0, it must also be defined at 0xA0 in bank 1, 0x120 in bank 2, and 0x1A0 in bank 3).

The examples:

- a) Stores the W register
- b) Stores the STATUS register in bank 0
- c) Stores PCLATH
- d) Executes ISR code
- e) Restores PCLATH
- f) Restores STATUS register (and bank select bit)
- g) Restores W register

EXAMPLE 13-1: SAVING STATUS AND W REGISTERS IN RAM (PIC16C61)

```
MOVWF
         W_TEMP
                            ;Copy W to TEMP register, could be bank one or zero
SWAPF
         STATUS, W
                            ; Swap status to be saved into W
MOVWF
         STATUS_TEMP
                            ; Save status to bank zero STATUS_TEMP register
:(ISR)
SWAPF
                            ;Swap STATUS_TEMP register into W
         STATUS_TEMP, W
                            ; (sets bank to original state)
MOVWF
         STATUS
                            ; Move W into STATUS register
SWAPF
         W_TEMP, F
                            ;Swap W_TEMP
                            ;Swap W_TEMP into W
SWAPF
         W_TEMP,W
```

EXAMPLE 13-2: SAVING STATUS, W, AND PCLATH REGISTERS IN RAM (ALL OTHER PIC16C6X DEVICES)

```
MOVWE
         W_TEMP
                            ;Copy W to TEMP register, could be bank one or zero
                            ; Swap status to be saved into W
SWAPF
          STATUS, W
CLRF
          STATUS
                            ; bank 0, regardless of current bank, Clears IRP, RP1, RP0
         STATUS_TEMP
MOVWF
                            ; Save status to bank zero STATUS TEMP register
          PCLATH, W
MOVF
                            ;Only required if using pages 1, 2 and/or 3
MOVWE
         PCLATH_TEMP
                            ;Save PCLATH into W
CLRF
          PCLATH
                            ;Page zero, regardless of current page
BCF
          STATUS, IRP
                            ;Return to Bank 0
MOVE
          FSR, W
                            ;Copy FSR to W
MOVWF
          FSR TEMP
                            ;Copy FSR from W to FSR_TEMP
:(ISR)
MOVF
          PCLATH_TEMP, W
                            ;Restore PCLATH
                            ; Move W into PCLATH
MOVWF
          PCLATH
SWAPF
          STATUS_TEMP, W
                            ;Swap STATUS TEMP register into W
                            ; (sets bank to original state)
MOVWF
         STATUS
                            ; Move W into STATUS register
SWAPE
          W_TEMP,F
                            ; Swap W_TEMP
SWAPF
         W_TEMP, W
                            ;Swap W_TEMP into W
```

13.7 Watchdog Timer (WDT)

Applicable Devices 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

The Watchdog Timer is a free running on-chip RC oscillator which does not require any external components. This RC oscillator is separate from the RC oscillator of the OSC1/CLKIN pin. That means that the WDT will run, even if the clock on the OSC1/CLKIN and OSC2/CLKOUT pins of the device has been stopped, for example, by execution of a SLEEP instruction. During normal operation, a WDT time-out generates a device reset. If the device is in SLEEP mode, a WDT time-out causes the device to wake-up and continue with normal operation (WDT Wake-up). The WDT can be permanently disabled by clearing configuration bit WDTE (Section 13.1).

13.7.1 WDT PERIOD

The WDT has a nominal time-out period of 18 ms, (with no prescaler). The time-out periods vary with temperature, VDD and process variations from part to part (see DC specs). If longer time-out periods are desired, a prescaler with a division ratio of up to 1:128 can be

assigned to the WDT under software control by writing to the OPTION register. Thus, time-out periods up to 2.3 seconds can be realized.

The CLRWDT and SLEEP instructions clear the WDT and the postscaler, if assigned to the WDT, and prevent it from timing out and generating a device RESET condition.

The TO bit in the STATUS register will be cleared upon a WDT time-out.

13.7.2 WDT PROGRAMMING CONSIDERATIONS

It should also be taken in account that under worst case conditions (VDD = Min., Temperature = Max., max. WDT prescaler) it may take several seconds before a WDT time-out occurs.

Note: When a CLRWDT instruction is executed and the prescaler is assigned to the WDT, the prescaler count will be cleared, but the prescaler assignment is not changed.

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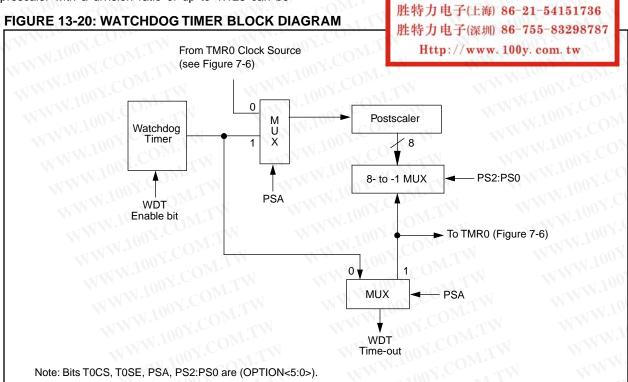


FIGURE 13-21: SUMMARY OF WATCHDOG TIMER REGISTERS

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
2007h	Config. bits	(1)	BODEN ⁽¹⁾	CP1	CP0	PWRTE ⁽¹⁾	WDTE	FOSC1	FOSC0
81h,181h	OPTION	RBPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0

Legend: Shaded cells are not used by the Watchdog Timer.

Note 1: See Figure 13-1, Figure 13-2, and Figure 13-3 for details of these bits for the specific device.

13.8 Power-down Mode (SLEEP)

Applicable Devices

61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

Power-down mode is entered by executing a SLEEP instruction.

If enabled, the Watchdog Timer will be cleared but keeps running, status bit \overline{PD} (STATUS<3>) is cleared, status bit \overline{TO} (STATUS<4>) is set, and the oscillator driver is turned off. The I/O ports maintain the status they had before the SLEEP instruction was executed (driving high, low, or hi-impedance).

For lowest current consumption in this mode, place all I/O pins at either VDD, or Vss, ensure no external circuitry is drawing current from the I/O pin, and disable external clocks. Pull all I/O pins, that are hi-impedance inputs, high or low externally to avoid switching currents caused by floating inputs. The TOCKI input should also be at VDD or Vss for lowest current consumption. The contribution from on-chip pull-ups on PORTB should be considered.

The \overline{MCLR}/VPP pin must be at a logic high level (VIHMC).

13.8.1 WAKE-UP FROM SLEEP

The device can wake from SLEEP through one of the following events:

- External reset input on MCLR/VPP pin.
- Watchdog Timer Wake-up (if WDT was enabled).
- Interrupt from RB0/INT pin, RB port change, or some peripheral interrupts.

External $\overline{\text{MCLR}}$ Reset will cause a device reset. All other events are considered a continuation of program execution and cause a "wake-up". The $\overline{\text{TO}}$ and $\overline{\text{PD}}$ bits in the STATUS register can be used to determine the cause of device reset. The $\overline{\text{PD}}$ bit, which is set on power-up is cleared when SLEEP is invoked. The $\overline{\text{TO}}$ bit is cleared if WDT time-out occurred (and caused wake-up).

The following peripheral interrupts can wake the device from SLEEP:

- TMR1 interrupt. Timer1 must be operating as an asynchronous counter.
- 2. SSP (Start/Stop) bit detect interrupt.
- 3. SSP transmit or receive in slave mode (SPI/I²C).
- 4. CCP capture mode interrupt.
- 5. Parallel Slave Port read or write.
- USART TX or RX (synchronous slave mode).

Other peripherals can not generate interrupts since during SLEEP, no on-chip Q clocks are present.

When the SLEEP instruction is being executed, the next instruction (PC + 1) is pre-fetched. For the device to wake-up through an interrupt event, the corresponding interrupt enable bit must be set (enabled). Wake-up is regardless of the state of the GIE bit. If the GIE bit is clear (disabled), the device continues execution at the instruction after the SLEEP instruction. If the GIE bit is set (enabled), the device executes the instruction after the SLEEP instruction and then branches to the interrupt address (0004h). In cases where the execution of the instruction following SLEEP is not desirable, the user should have a NOP after the SLEEP instruction.

13.8.2 WAKE-UP USING INTERRUPTS

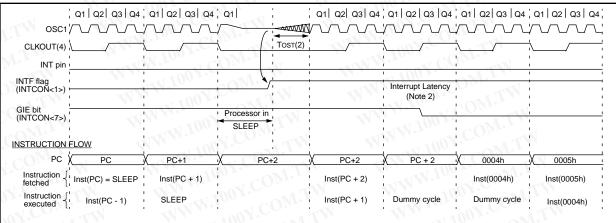
When global interrupts are disabled (GIE cleared) and any interrupt source has both its interrupt enable bit and interrupt flag bit set, one of the following will occur:

- If the interrupt occurs before the execution of a SLEEP instruction, the SLEEP instruction will complete as a NOP. Therefore, the WDT and WDT postscaler will not be cleared, the TO bit will not be set and PD bits will not be cleared.
- If the interrupt occurs during or after the execution of a SLEEP instruction, the device will immediately wake up from sleep. The SLEEP instruction will be completely executed before the wake-up. Therefore, the WDT and WDT postscaler will be cleared, the TO bit will be set and the PD bit will be cleared.

Even if the flag bits were checked before executing a SLEEP instruction, it may be possible for flag bits to become set before the SLEEP instruction completes. To determine whether a SLEEP instruction executed, test the $\overline{\text{PD}}$ bit. If the $\overline{\text{PD}}$ bit is set, the SLEEP instruction was executed as a NOP.

To ensure that the WDT is cleared, a CLRWDT instruction should be executed before a SLEEP instruction.

FIGURE 13-22: WAKE-UP FROM SLEEP THROUGH INTERRUPT



Note 1: XT, HS or LP oscillator mode assumed.

- 2: Tost = 1024Tosc (drawing not to scale) This delay will not be there for RC osc mode.
- 3: GIE = '1' assumed. In this case after wake-up, the processor jumps to the interrupt routine. If GIE = '0', execution will continue in-line.
- 4: CLKOUT is not available in these osc modes, but shown here for timing reference.

13.9 Program Verification/Code Protection

Applicable Devices

61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

If the code protection bit(s) have not been programmed, the on-chip program memory can be read out for verification purposes.

Note: Microchip does not recommend code protecting windowed devices.

13.10 ID Locations

Applicable Devices 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

Four memory locations (2000h - 2003h) are designated as ID locations where the user can store checksum or other code-identification numbers. These locations are not accessible during normal execution but are readable and writable during program/verify. It is recommended that only the 4 least significant bits of the ID location are used.

For ROM devices, these values are submitted along with the ROM code.

13.11 <u>In-Circuit Serial Programming</u>

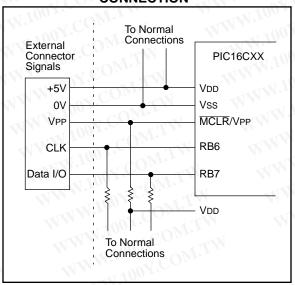
Applicable Devices 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

The PIC16CXX microcontrollers can be serially programmed while in the end application circuit. This is simply done with two lines for clock and data, and three other lines for power, ground, and the programming voltage. This allows customers to manufacture boards with unprogrammed devices, and then program the microcontroller just before shipping the product. This also allows the most recent firmware or a custom firmware to be programmed.

The device is placed into a program/verify mode by holding pins RB6 and RB7 low while raising the MCLR (VPP) pin from VIL to VIHH (see programming specification). RB6 becomes the programming clock and RB7 becomes the programming data. Both RB6 and RB7 are Schmitt Trigger inputs in this mode.

After reset, to place the device in program/verify mode, the program counter (PC) is at location 00h. A 6-bit command is then supplied to the device. Depending on the command, 14-bits of program data are then supplied to or from the device, depending if the command was a load or a read. For complete details of serial programming, please refer to the PIC16C6X/7X Programming Specifications (Literature #DS30228).

FIGURE 13-23: TYPICAL IN-CIRCUIT SERIAL PROGRAMMING CONNECTION



14.0 INSTRUCTION SET SUMMARY

Each PIC16CXX instruction is a 14-bit word divided into an OPCODE which specifies the instruction type and one or more operands which further specify the operation of the instruction. The PIC16CXX instruction set summary in Table 14-2 lists byte-oriented, bit-oriented, and literal and control operations. Table 14-1 shows the opcode field descriptions.

For **byte-oriented** instructions, 'f' represents a file register designator and 'd' represents a destination designator. The file register designator specifies which file register is to be used by the instruction.

The destination designator specifies where the result of the operation is to be placed. If 'd' is zero, the result is placed in the W register. If 'd' is one, the result is placed in the file register specified in the instruction.

For **bit-oriented** instructions, 'b' represents a bit field designator which selects the number of the bit affected by the operation, while 'f' represents the number of the file in which the bit is located.

For **literal and control** operations, 'k' represents an eight or eleven bit constant or literal value.

TABLE 14-1: OPCODE FIELD DESCRIPTIONS

Field	Description
f	Register file address (0x00 to 0x7F)
W	Working register (accumulator)
b	Bit address within an 8-bit file register
k	Literal field, constant data or label
x	Don't care location (= 0 or 1) The assembler will generate code with x = 0. It is the recommended form of use for compatibility with all Microchip software tools.
d	Destination select; d = 0: store result in W, d = 1: store result in file register f. Default is d = 1
label	Label name
TOS	Top of Stack
PC	Program Counter
PCLATH	Program Counter High Latch
GIE	Global Interrupt Enable bit
WDT	Watchdog Timer/Counter
$\overline{\text{TO}}$	Time-out bit
$\overline{\mathtt{PD}}$	Power-down bit
dest	Destination either the W register or the specified register file location
[]	Options
()	Contents
\rightarrow	Assigned to
<>	Register bit field
€	In the set of
italics	User defined term (font is courier)

The instruction set is highly orthogonal and is grouped into three basic categories:

- · Byte-oriented operations
- · Bit-oriented operations
- · Literal and control operations

All instructions are executed within one single instruction cycle, unless a conditional test is true or the program counter is changed as a result of an instruction. In this case, the execution takes two instruction cycles with the second cycle executed as a NOP. One instruction cycle consists of four oscillator periods. Thus, for an oscillator frequency of 4 MHz, the normal instruction execution time is 1 μs . If a conditional test is true or the program counter is changed as a result of an instruction, the instruction execution time is 2 μs .

Table 14-2 lists the instructions recognized by the MPASM assembler.

Figure 14-1 shows the general formats that the instructions can have.

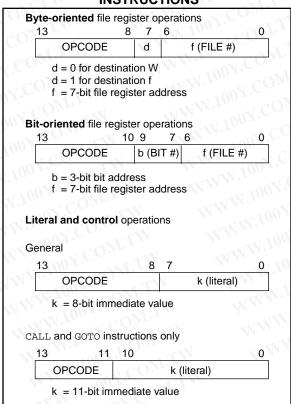
Note: To maintain upward compatibility with future PIC16CXX products, <u>do not use</u> the OPTION and TRIS instructions.

All examples use the following format to represent a hexadecimal number:

Oxhh

where h signifies a hexadecimal digit.

FIGURE 14-1: GENERAL FORMAT FOR INSTRUCTIONS



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PIC16CXX INSTRUCTION SET TABLE 14-2:

Mnemonic, Operands		Description	Cycles	14-Bit Opcode				Status	Notes
			WW.	MSb	I.CO	Are.	LSb	Affected	
BYTE-ORIE	NTED	FILE REGISTER OPERATIONS	WWW	Tan	V.CC	DM:	rW		
ADDWF	f, d	Add W and f	1	00	0111	dfff	ffff	C,DC,Z	1,2
ANDWF	f, d	AND W with f	1	00	0101	dfff	ffff	Z	1,2
CLRF	f	Clear f	1	00	0001	lfff	ffff	Z	2
CLRW	N-	Clear W	1	00	0001	0xxx	xxxx	Z	
COMF	f, d	Complement f	1 1	00	1001	dfff	ffff	Z	1,2
DECF	f, d	Decrement f	1	00	0011	dfff	ffff	Z	1,2
DECFSZ	f, d	Decrement f, Skip if 0	1(2)	00	1011	dfff	ffff		1,2,3
INCF	f, d	Increment f	1	00	1010	dfff	ffff	Z	1,2
INCFSZ	f, d	Increment f, Skip if 0	1(2)	00	1111	dfff	ffff	TW	1,2,3
IORWF	f, d	Inclusive OR W with f	ì	00	0100	dfff	ffff	Z	1,2
MOVF	f, d	Move f	1	00	1000	dfff	ffff	Z	1,2
MOVWF	f	Move W to f	1	00	0000	lfff	ffff	11.	
NOP	TI	No Operation	1	00	0000	0xx0	0000	TIM	
RLF	f, d	Rotate Left f through Carry	1	00	1101	dfff	ffff	С	1,2
RRF	f, d	Rotate Right f through Carry	- 1 T	00	1100	dfff	ffff	C	1,2
SUBWF	f, d	Subtract W from f)NI	00	0010	dfff	ffff	C,DC,Z	1,2
SWAPF	f, d	Swap nibbles in f	M. 1	00	1110	dfff	ffff		1,2
XORWF	f, d	Exclusive OR W with f	11	0.0	0110	dfff	ffff	Z	1,2
BIT-ORIEN	TED FI	LE REGISTER OPERATIONS	COM		**************************************	MAN	005	COM	TW
BCF 1	f, b	Bit Clear f	1	01	00bb	bfff	ffff	- COM	1,2
BSF	f, b	Bit Set f	1	01		bfff	ffff	Y.C.	1,2
BTFSC	f, b	Bit Test f, Skip if Clear	1 (2)	01	10bb	bfff	ffff	-1 COD	3
BTFSS	f, b	Bit Test f, Skip if Set	1 (2)	01	11bb	bfff	ffff	07.0	3
LITERAL A	ND CO	NTROL OPERATIONS	NY.COX	W		WW	1	00 A .C.	-117
ADDLW	k	Add literal and W	< (01	11	111x	kkkk	kkkk	C,DC,Z	D.S.
ANDLW	- k00	AND literal with W	100 1.	11	1001	kkkk	kkkk	Z	Mo
CALL	k	Call subroutine	C 2	10	0kkk	kkkk		anv.	
CLRWDT	×=10	Clear Watchdog Timer	1003	00	0000	0110	0100	TO,PD	CON
GOTO	k	Go to address	2	10	1kkk		kkkk	1003	
IORLW	k	Inclusive OR literal with W	N.100 10	11	1000		kkkk	Z	- cO
MOVLW	k	Move literal to W	1001	11	00xx	kkkk		100	X.C
RETFIE	XN	Return from interrupt	200	00	0000	0000	1001	M.10	×7 C.
RETLW	k	Return with literal in W	2	11	01xx	kkkk	kkkk	110	01.
RETURN	-11	Return from Subroutine	2	00	0000	0000	1000	MM.	NV C
SLEEP	Nin .	Go into standby mode	100	00	0000	0110	0011	TO.PD	00 r.
SUBLW	k	Subtract W from literal	100	11		kkkk	kkkk	C,DC,Z	LOON.
XORLW	k	Exclusive OR literal with W	11100	11	1010		kkkk	Z	Ton r.
A OILEV	N.	Exclusive OIX literal WITH VV		14	71010	VVVV	VVVV	-	-03

Note 1: When an I/O register is modified as a function of itself (e.g., MOVF PORTB, 1), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.

If this instruction is executed on the TMR0 register (and, where applicable, d = 1), the prescaler will be cleared if assigned

If Program Counter (PC) is modified or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a NOP.

14.1 <u>Instruction Descriptions</u>

ADDLW	Add Lite	ral and	N		ANDLW	AND Lit	eral with	W	
Syntax:	[label] A	DDLW	k	N	Syntax:	[label] A	NDLW	k	
Operands:	$0 \le k \le 2$	55			Operands:	$0 \le k \le 2$	55		
Operation:	(W) + k -	→ (W)			Operation:	(W) .ANI	O. (k) \rightarrow (W)	
Status Affected:	C, DC, Z				Status Affected:	Z			
Encoding:	11	111x	kkkk	kkkk	Encoding:	11	1001	kkkk	kkkk
Description:	The conte added to t result is pl	he eight b	it literal 'k'	and the	Description:		ith the eig	egister are ht bit litera ne W regis	al 'k'. The
Words:	1				Words:	1.00			
Cycles:	1				Cycles:	1 Y.CC			
Q Cycle Activity:	Q1	Q2	Q3	Q4	Q Cycle Activity:	Q1	Q2	Q3	Q4
	Decode	Read literal 'k'	Process data	Write to		Decode	Read literal "k"	Process data	Write to W
Example:	ADDLW	0x15			Example	ANDLW	0x5F		
	Before In	W =	0x10			Before In	W =	0xA3	
		W =	0x25				W =	0x03	

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ADDWF	Add W and f	ANDWF	AND W with f
Syntax:	[label] ADDWF f,d	Syntax:	[label] ANDWF f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$	Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	(W) + (f) \rightarrow (destination)	Operation:	(W) .AND. (f) \rightarrow (destination)
Status Affected:	C, DC, Z	Status Affected:	Z W 1001. COM.T
Encoding:	00 0111 dfff ffff	Encoding:	00 0101 dfff ffff
Description:	Add the contents of the W register with register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.	Description:	AND the W register with register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.
Words:	N100X.COM.TW	Words:	1 CC
Cycles:	1 100 Y. COM. TW	Cycles:	T1 W 100 1.
Q Cycle Activity:	Q1 Q2 Q3 Q4	Q Cycle Activity:	Q1 Q2 Q3 Q4
	Decode Read register data Write to destination		Decode Read register data Write to destination
Example	ADDWF FSR, 0	Example	ANDWF FSR, 1
	Before Instruction		Before Instruction
	W = 0x17		W = 0x17
	FSR = 0xC2 After Instruction		FSR = 0xC2 After Instruction
	W = 0xD9		W = 0x17
	FSR = 0xC2		FSR = 0x02

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BCF Bit Clear f [label] BCF Syntax: f,b Operands: $0 \le f \le 127$ $0 \le b \le 7$ Operation: $0 \rightarrow (f < b >)$ Status Affected: None Encoding: 01 00bb bfff ffff Description: Bit 'b' in register 'f' is cleared. Words: Cycles: Q1 Q2 Q3 Q4 Q Cycle Activity: Decode Read Process Write

Example BCF FLAG_REG, 7

Before Instruction

register

 $FLAG_REG = 0xC7$

data

register 'f

After Instruction

 $FLAG_REG = 0x47$

BTFSC Bit Test, Skip if Clear [label] BTFSC f,b Syntax: Operands: $0 \le f \le 127$ $0 \le b \le 7$ skip if (f < b >) = 0Operation: Status Affected: None 10bb bfff ffff Encoding: 0.1 Description: If bit 'b' in register 'f' is '1' then the next instruction is executed. If bit 'b', in register 'f', is '0' then the next instruction is discarded, and a NOP is executed instead, making this a 2Tcy instruction. Words: 1 Cycles: 1(2) Q Cycle Activity: Q1 Q2 Q3 Q4 Decode Read Process Noregister 'f' Operation data If Skip: (2nd Cycle) Q1 Q2 Q3 Q4 No-No-No-No-Operation Operation Operation Operation Example HERE FLAG, 1 FALSE GOTO PROCESS_CODE TRIF Before Instruction PC = address HERE

BSF Bit Set f
Syntax: [label] BSF

Operands: $0 \le f \le 127$ $0 \le b \le 7$

Operation: $1 \rightarrow (f < b >)$

Status Affected: None

Encoding: 01 01bb bfff ffff

Description: Bit 'b' in register 'f' is set.

Words: 1 Cycles: 1

Q Cycle Activity: Q1 Q2 Q3 Q4

Decode Read Process Write register 'f'

f,b

Example BSF FLAG_REG,

Before Instruction

 $FLAG_REG = 0x0A$

After Instruction

 $FLAG_REG = 0x8A$

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After Instruction

PC =

PC =

if FLAG<1>=0,

if FLAG<1>=1,

address TRUE

address FALSE

BTFSS	Bit Test f	, Skip if S	Set	- N	CALL	Call Sul	broutine		
Syntax:	[label] BT	FSS f,b	W.	()	Syntax:	[label]	CALL k	(
Operands:	$0 \le f \le 12$	27			Operands:	$0 \le k \le 2$	2047		
	$0 \le b < 7$				Operation:	(PC)+ 1-	\rightarrow TOS,		
Operation:	skip if (f<	b>) = 1				$k \to PC$			
Status Affected:	None					(PCLATI	H<4:3>) -	→ PC<12	:11>
Encoding:	01	11bb	bfff	ffff	Status Affected:	None	- XI		
Description:	If bit 'b' in	register 'f' i	s '0' then tl	ne next	Encoding:	10	0kkk	kkkk	kkkk
COM.TW	If bit 'b' is '	and a NOF	e next instr e is execute	ed	Description:	(PC+1) is eleven bit into PC b	outine. First pushed or immediate its <10:0>. re loaded fr	nto the stace address i The upper	ck. The s loaded bits of
Words:	1					is a two c	ycle instruc	ction.	I II. CAL.
Cycles:	1(2)				Words:	1007			
Q Cycle Activity:	Q1	Q2	Q3	Q4	Cycles:	2			
	Decode	Read register 'f'	Process data	No- Operation	Q Cycle Activity:	Q1	Q2	Q3	Q4
If Skip:	(2nd Cyc	le)	11.100	-1 COM.	1st Cycle	Decode	Read	Process	Write
100 Y. G. O.M.	Q1	Q2	Q3	Q4		WW.10	literal 'k', Push PC to Stack	data	PC
	No- Operation	No- Operation	No- Operation	No- Operation	2nd Cycle	No- Operation	No-	No- Operation	No- Operat
Example	HERE	BTFSC	FLAG,1		Example	HERE	CALL	THERE	
	FALSE	GOTO	PROCESS_	_CODE	Example		nstruction		
	TRUE	sī•				belore ii		ı .ddress не	RE
		•				After Ins		-1 CO	M.
	Before In	struction						ddress TH	
		PC = a	address I	IERE			TOS = A	ddress HE	CRE+1
	After Inst								
		if FLAG<1: PC =	> = 0, address F	NT GE 331 1					
		rc = if FLAG<1:		ALSE					
			address Ti	RIIE					

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CLRF Clear f

Syntax: [label] CLRF f

Operands: $0 \le f \le 127$ Operation: $00h \rightarrow (f)$ $1 \rightarrow Z$

Status Affected: Z

Encoding: 00 0001 1fff ffff

Description: The contents of register 'f' are cleared

and the Z bit is set.

Words: 1 Cycles: 1

Q Cycle Activity: Q1

Q1 Q2 Q3 Q4

Decode Read Process Write register 'f' register 'f'

Example CLRF FLAG_REG

Before Instruction

 $FLAG_REG = 0x5A$

After Instruction

 $\begin{array}{ccc} FLAG_REG & = & 0x00 \\ Z & = & 1 \end{array}$

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Example CLRW

Before Instruction

W = 0x5A

After Instruction

W = 0x00 Z = 1

CLRWDT Clear Watchdog Timer

Syntax: [label] CLRWDT

Operands: None

Operation: $00h \rightarrow WDT$

 $0 \rightarrow WDT$ prescaler,

 $1 \to \overline{\mathsf{TO}} \\ 1 \to \overline{\mathsf{PD}}$

Status Affected: TO, PD

Encoding: 00 0000

Description: CLRWDT instruction resets the Watch-

dog Timer. It also resets the prescaler of the WDT. Status bits TO and PD are

0110

0100

set.

Words: 1

Q Cycle Activity:

Cycles:

 Q1
 Q2
 Q3
 Q4

 Decode
 No-Operation
 Process data
 Clear WDT Counter

Example CLRWDT

Before Instruction

WDT counter = ?

After Instruction

 WDT counter
 =
 0x00

 WDT prescaler
 0

 TO
 =
 1

 PD
 =
 1

COMF	Complen	nent f	1:11		DECFSZ	Decrem	ent f, Ski	p if 0	
Syntax:	[label]	COMF	f,d		Syntax:	[label]	DECFSZ	f,d	
Operands:	$0 \le f \le 12$ $d \in [0,1]$	7 1.00			Operands:	$0 \le f \le 12$ $d \in [0,1]$			
Operation: Status Affected:	$(\bar{f}) \rightarrow (des)$	stination)			Operation:	(f) - 1 \rightarrow skip if re	(destinati sult = 0	on);	
Encoding:	00	1001	dfff	ffff	Status Affected:	None			
Description:	The conte				Encoding:	00	1011	dfff	ffff
Words: Cycles:	mented. If W. If 'd' is register 'f'.				Description:	mented. If W register back in register If the resu	nts of regist 'd' is 0 the '. If 'd' is 1 th gister 'f'. It is 1, the n If the result	result is pla ne result is p ext instruct	ced in the placed ion, is
27/12	Q1	Q2	Q3	04		executed i	nstead mak		
Q Cycle Activity:	Decode	Read	Process	Q4 Write to	Words:	tion.			
	Decode	register 'f'	data	destination	Cycles:	1(2)			
	N .	WW	110	M.COP	Q Cycle Activity:		Q2	Q3	Q4
Example	COMF	REG	1,0		Q Oycle Activity.	Decode	Read	Process	Write to
	Before In	struction				200000	register 'f'	data	destinatio
	After Inst	REG1	= 0x1	3 (V) 5 CO	If Skip:	(2nd Cy	cle)		
	W 1/1// 1	REG1	= 0x1	3.100 1.00		Q1	Q2	Q3	Q4
	MI.W	W	= 0xE	C 100 Y.C		No- Operation	No- Operation	No- Operation	No- Operation
DECF	Decreme	ent f				Operation	Operation	Operation	Operation
Syntax:	[label] D	_	W	1100 X.	Example	HERE	DECFS		
Operands:	0 ≤ f ≤ 12					CONTIN	GOTO IUE •	LOO	PITW
W.100 F	$d \in [0,1]$						MAIN		
Operation:	(f) - 1 \rightarrow ((destinat	ion)			Before Ir	nstruction		
Status Affected:	Z					PC	= add	ress here	
Encoding:	00	0011	dfff	ffff		After Ins		E100X.	
Description:	Decremen result is sto 1 the resul	t register ored in the t is stored	'f'. If 'd' is e W regist I back in i	0 the er. If 'd' is egister 'f'.		if CN' PC if CN'	T = 0, = add	ress CONT	INUE
Words:	100 2					PC		ress HERE	+1 .CO
Cycles:	100								
Q Cycle Activity:	Q1	Q2	Q3	Q4					
	Decode	Read	Process	Write to	N 1 100Y.	WTI	V	NA .	100 X'
	N. T.	register 'f'	data	destination	KYYY	特力和	才料886	3-3-5758	3170
	M.M.In	ov CC	Mr.	N ·	胜	特力电子		21-5415	
Example	DECF	CNT,	10M.		pt.100 pt	特力电子		755-832	

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Before Instruction

After Instruction CNT

CNT Z

0x01

0

0x00

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GOTO	Uncondi	tional Br	anch		INCF	Increme	nt f		
Syntax:	[label]	GOTO	k 1	N	Syntax:	[label]	INCF	f,d	
Operands:	$0 \le k \le 20$	047			Operands:	$0 \le f \le 12$	27		
Operation:	$k \to PC <$	10:0>				$d \in [0,1]$			
	PCLATH-	<4:3> → I	PC<12:11	l>	Operation:	$(f) + 1 \rightarrow$	(destina	ition)	
Status Affected:	None				Status Affected:	Z			
Encoding:	10	1kkk	kkkk	kkkk	Encoding:	00	1010	dfff	ffff
Description:	eleven bit into PC bit	n unconditi immediate ts <10:0>. aded from two cycle i	value is lo The upper PCLATH<	paded bits of 4:3>.	Description:	The conte mented. If the W reg placed ba	'd' is 0 th ster. If 'd'	e result is is 1 the re	placed in
Words:	,1				Words:	11			
Cycles:	2				Cycles:	1.100 1			
Q Cycle Activity:	Q 1	Q2	Q3	Q4	Q Cycle Activity:	Q1	Q2	Q3	Q4
1st Cycle	Decode	Read literal 'k'	Process data	Write to PC		Decode	Read register	Process data	Write destinat
2nd Cycle	No- Operation	No- Operation	No- Operation	No- Operation		TWW.1	-7 C	OM	
	Орогалогі	Орогалогі	Operation	Operation	Example	INCF	CNT,	1	
Example	GOTO T	HERE				Before In	struction	i M	
	After Inst	ruction					CNT Z	= 0xF	F
		PC = .	Address	THERE		After Inst		= CO	
							CNT	= 0x0	0
							Z	= 1	,

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INCFSZ	Increme	nt f, Skip	if 0	
Syntax:	[label]	INCFSZ	f,d	
Operands:	$0 \le f \le 12$	27		
William V	d ∈ [0,1]	OOY.C	x 1 T	
Operation:	(f) + 1 \rightarrow skip if res		tion),	
Status Affected:	None			
Encoding:	00	1111	dfff	ffff
Description:	mented. If the W regi placed ba- If the resu executed.	'd' is 0 the ister. If 'd' i ck in regis It is 1, the If the resuinstead ma	ster 'f' are e result is p is 1 the res ter 'f'. next instru lt is 0, a N aking it a 2	placed in sult is uction is OP is
Words:	1			
Cycles:	1(2)			
Q Cycle Activity:	√ Q1	Q2	Q3	Q4
	Decode	Read register 'f'	Process data	Write to destination
If Skip:	(2nd Cyc	•	W.	00X:C
	Q1	Q2	Q3	Q4
	No- Operation	No- Operation	No- Operation	No- Operation
Example	HERE CONTIN	INCFS GOTO UE	SZ C	NT, 1 OP
	Before In PC After Inst CNT if CNT PC if CNT PC	= add cruction = CN = 0, = add = 0, = add	ress here T + 1 ress cont	INUE

IORLW			eral with	W
Syntax:	[label]	IORLW	k	
Operands:	$0 \le k \le 2$	55		
Operation:	(W) .OR.	$k \rightarrow (W)$)	
Status Affected:	Z			
Encoding:	0 11	1000	kkkk	kkkk
Description:	OR'ed wit	h the eigh	W register t bit literal ne W regist	'k'. The
Words:	1.00			
Cycles:	1			
Q Cycle Activity:	00 Q1	Q2	Q3	Q4
	Decode	Read literal 'k'	Process data	Write t
Example	IORLW	0x35		
	Before In	struction W =	0x9A	
	After Inst	** =	UX9A	
		W =	0xBF	

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IORWF	Inclusive	e OR W	with f	
Syntax:	[label]	IORWF	f,d	-31
Operands:	$0 \le f \le 12$ $d \in [0,1]$	27100		
Operation:	(W) .OR.	$(f) \rightarrow (de)$	estination	
Status Affected:	Z			
Encoding:	0.0	0100	dfff	ffff
Description:	Inclusive (ter 'f'. If 'd' W register back in re	is 0 the re r. If 'd' is 1	sult is pla	ced in the
Words:	1			
Cycles:	1			
Q Cycle Activity:	Q1	Q2	Q3	Q4
	Decode	Read register 'f'	Process data	Write to destination
Example	IORWF		RESULT,	0.100Y

					1.1/
Al'To	TW		W	MM	
Example	IORWF		RES	JLT, 0	
	Before Ir	nstruction	1 🌃		
		RESULT	= 4	0x13	
		W	=	0x91	
	After Ins	truction			
		RESULT	=	0x13	
		W	=	0x93	
		Z	=	1	
MOVF	Move f				
Syntax:	[label]	MOVF	f,d		11
Operands:	0 ≤ f ≤ 12	27			
WWW	d ∈ [0,1]				
Operation:	$(f) \rightarrow (de$	estination	i)		
Status Affected:					

MOVF	Move t			
Syntax:	[label]	MOVF	f,d	- TXX
Operands:	$0 \le f \le 12$ $d \in [0,1]$	7 _{M.T}		
Operation:	$(f) \rightarrow (de$	stination)	
Status Affected:	Z			
Encoding:	00	1000	dfff	ffff
Description:	The conte destination of d. If d = d = 1, the itself. d = d ter since s	n dependa 0, destina destination 1 is useful	ant upon thation is Wir on is file re I to test a t	he status register. If gister f file regis-
Words:	1, WW			
Cycles:	1			
Q Cycle Activity:	Q1	Q2	Q3	Q4
	Decode	Read register 'f'	Process data	Write to destination
Example	MOVF	FSR,	0100Y.	COM.T
	After Inst		ue in FSR	register

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MOVLW	Move Lit	teral to V	٧	
Syntax:	[label]	MOVLW	/ k	
Operands:	$0 \le k \le 2$	55		
Operation:	$k \rightarrow (W)$			
Status Affected:	None			
Encoding:	11	00xx	kkkk	kkkk
Description:			k' is loaded ares will as	
Words:	1001.			
Cycles:	1			
Q Cycle Activity:	Q1	Q2	Q3	Q4
	Decode	Read literal 'k'	Process data	Write to
Example	MOVLW	0x5A		

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Syntax:	[label]	MOVWI	₹V-Vf	COM.
Operands:	0 ≤ f ≤ 12	27		
Operation:	$(W) \rightarrow (f)$			
Status Affected:	None			
Encoding:	00	0000	1fff	ffff
Description:	Move data	from W r	egister to	register
Words:	1			
	1			
Words: Cycles: Q Cycle Activity:	1 1 Q1	N Q2	Q3	Q4
Cycles:	1 1 Q1 Decode	Q2 Read register 'f'	Q3 Process data	Q4 Write register 'f'
Cycles: Q Cycle Activity:		Read register 'f'	Process	Write
Cycles:	MOVWF Before In	Read register 'f' OPTIC struction OPTION W	Process data	Write register 'f'

NOP No Operation Syntax: [label] NOP Operands: None Operation: No operation Status Affected: None Encoding: 00 0000 0xx00000 Description: No operation. Words: Cycles: Q Cycle Activity: Q1 Q2 Q3 Q4 Decode No-No-Operation Operation Operation Example NOP

RETFIE	Return f	rom Inter	rupt	
Syntax:	[label]	RETFIE		
Operands:	None			
Operation:	$\begin{array}{c} TOS \to F \\ 1 \to GIE \end{array}$	PC,		
Status Affected:	None			
Encoding:	00	0000	0000	1001
Description:	Return from Interrupt. Stack is PC and Top of Stack (TOS) is loaded PC. Interrupts are enabled by set Global Interrupt Enable bit, GIE (INTCON<7>). This is a two cycle instruction.			
Words:	1C			
Cycles:	2			
Q Cycle Activity:	Q1	Q2	Q3	Q4
1st Cycle	Decode	No- Operation	Set the GIE bit	Pop from the Stack
2nd Cycle	No- Operation	No- Operation	No- Operation	No- Operation

OPTION Load Option Register [label] OPTION Syntax: Operands: None Operation: $(W) \rightarrow OPTION$ Status Affected: None Encoding: 0000 0110 Description: The contents of the W register are loaded in the OPTION register. This instruction is supported for code compatibility with PIC16C5X products. Since OPTION is a readable/writable register, the user can directly address Words: Cycles: Example To maintain upward compatibility with future PIC16CXX products, do not use this instruction.

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RETFIE

After Interrupt

PC =

GIE =

TOS

Example

RETLW	Return v	vith Liter	al in W	
Syntax:	[label]	RETLW	k	111
Operands:	$0 \le k \le 2$	55		
Operation:	$k \rightarrow (W); \\ TOS \rightarrow F$	C 100		
Status Affected:	None			
Encoding:	11	01xx	kkkk	kkkk
escription:	bit literal 'k loaded fro	c'. The proo m the top Iress). This	aded with the gram count of the stacts is a two co	ter is k (the
Vords:	1			
cycles:	2			
Cycle Activity:	Q1	Q2	Q3	Q4
1st Cycle	Decode	Read literal 'k'	No- Operation	Write to W, Pop from the Stack
2nd Cycle	No- Operation	No- Operation	No- Operation	No- Operation
xample	CALL TABLE	;offse	tains tabl t value has table	
TABLE	ADDWF PC RETLW k1 RETLW k2	;W = o ;Begin ;	ffset table	

RETLW kn

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Before Instruction

After Instruction

; End of table

W = value of k8

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W = 0x07

RETURN	Return f	rom Sub	routine	
Syntax:	[label]	RETURI	N	
Operands:	None			
Operation:	$TOS \to F$	C		
Status Affected:	None			
Encoding:	00	0000	0000	1000
Description:	Return fro POPed an is loaded i is a two cy	d the top on the top of	of the stack	(TOS)
Words:	100Y.			
Cycles:	2			
Q Cycle Activity:	Q1	Q2	Q3	Q4
1st Cycle	Decode	No- Operation	No- Operation	Pop from the Stack
2nd Cycle	No- Operation	No- Operation	No- Operation	No- Operation
Example	RETURN			
	After Inte	rrupt PC =	TOS	

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RLF	Rotate L	eft f thr	ough Ca	rry	RRF	Rotate R	light f th	rough C	arry
Syntax:	[label]	RLF	f,d		Syntax:	[label]	RRF f	,d	
Operands:	$0 \le f \le 12$ $d \in [0,1]$	27 CO			Operands:	$0 \le f \le 12$ $d \in [0,1]$	27		
Operation:	See desc	cription b	elow		Operation:	See desc	cription b	elow	
Status Affected:	C				Status Affected:	CMIT			
Encoding:	0.0	1101	dfff	ffff	Encoding:	00	1100	dfff	ffff
Description:	The conte one bit to Flag. If 'd' W register back in re	the left th is 0 the re r. If 'd' is 1 gister 'f'.	rough the esult is pla	Carry ced in the	Description:	The conte one bit to Flag. If 'd' W register back in re	the right t is 0 the re r. If 'd' is 1	through the esult is pla	e Carry ced in the
Words:	1				Words:	1,00 1.	·MO	1.44	
Cycles:	1				Cycles:	x1100Y.			
Q Cycle Activity:	Q 1	Q2	Q3	Q4	Q Cycle Activity:	Q1	Q2	Q3	Q4
	Decode	Read register 'f'	Process data	Write to destination		Decode	Read register 'f'	Process data	Write to destination
Example	RLF	RE(G1,0	100 Y.CO	Example	RRF	00Y.C	REG1,0	N
M.In. CON	Before In	struction	NAM		TW	Before In	struction		
		REG1		0 0110			REG1		0 0110
	After Inst	C	= 0			After Inst	C	= 0	
		REG1	= 111	0 0110			REG1	= 111	0 0110
	VI.Ma	IVEO I					W		1 0011
	OMITY	W	= 110	0 1100			VV	- 011	_ 00
	OM.TV		= 110 = 1	0 1100			C	= 0	
	OMITY			0 1100				- 011	

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PIC16C6X

SLEEP

Syntax: SLEEP [label]

Operands: None

00h → WDT, Operation:

0 → WDT prescaler,

 $1 \rightarrow \overline{TO}$ $0 \rightarrow \overline{PD}$

Status Affected: TO, PD

Encoding: 0110 0011 00 0000

Description: The power-down status bit, PD is

cleared. Time-out status bit, TO is set. Watchdog Timer and its pres-

caler are cleared.

The processor is put into SLEEP mode with the oscillator stopped. See

Section 13.8 for more details.

Words: Cycles:

Q Cycle Activity: Q1 Q2 Q3 Q4

> Go to Decode No-No-Sleep Operation Operation

Example: SLEEP

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SUBLW Subtract W from Literal

Syntax: [label] SUBLW k

 $0 \le k \le 255$ Operands: Operation: $k - (W) \rightarrow (W)$

Status Affected: C, DC, Z

Encoding: 11 110x kkkk kkkk

The W register is subtracted (2's comple-Description: ment method) from the eight bit literal 'k'.

The result is placed in the W register.

Words: Cycles:

Q3 Q4 Q Cycle Activity: Q1 Q2

Decode Read Process Write to W literal 'k'

0x02Example 1: SUBLW

Before Instruction

W C 4 z =

After Instruction

W

1; result is positive С

Z 0

Example 2: Before Instruction

> W С Z

After Instruction

0

С 1; result is zero

Ζ

Before Instruction Example 3:

> W С

Z

After Instruction

0xFF W

C 0; result is negative

SUBWF	Subtract	W from f		
Syntax:	[label]	SUBWF	f,d	
Operands:	$0 \le f \le 127$ $d \in [0,1]$	0 1.C		
Operation:	(f) - (W) —	(destina	tion)	
Status Affected:	C, DC, Z			
Encoding:	00	0010	dfff	ffff
	stored in th	e W regist	er. If 'd' is 1	
Words:		e W regist	er. If 'd' is 1	1 the
Cycles:	stored in th result is sto	e W regist	er. If 'd' is 1	1 the
11/1	stored in the result is stored 1	e W registo pred back in	er. If 'd' is 1 n register '	1 the f'. Q4 Write to
Cycles:	stored in the result is stored in the result in the result in the result is stored in the result in	e W registored back in Q2	er. If 'd' is 1 n register ' Q3 Process	the f'.
Cycles: Q Cycle Activity:	stored in the result is stored in the result in the result in the result is stored in the result in	Q2 Read register 'f'	er. If 'd' is 1 n register ' Q3 Process	1 the f'. Q4 Write to
Cycles: Q Cycle Activity:	stored in the result is stored in the result in the result is stored in the result is stored in the result in the result is stored in the result in the result is stored in the result in	Q2 Read register 'f'	er. If 'd' is 1 n register ' Q3 Process	1 the f'. Q4 Write to

SWAPE	Swap Nib	bies in	I	
Syntax:	[label] S	SWAPF f	,d	
Operands:	$0 \le f \le 127$ $d \in [0,1]$	7		
Operation:	(f<3:0>) - (f<7:4>) -			
Status Affected:	None			
Encoding:	00	1110	dfff	ffff
Description:	The upper a 'f' are excha placed in W is placed in	anged. If / register.	'd' is 0 the If 'd' is 1 t	result is
Words:	Y CC			
Cycles:	1001			
Q Cycle Activity:	Q1	Q2	Q3	Q4
	Decode	Read register 'f'	Process data	Write to destination
Example	SWAPF F	REG,	0	

Before Instruction

After Instruction

REG1

REG1

0xA5

0xA5

Swan Nibbles in f

SWAPE

	VV	(i =	2
	C	=	1; res
	CZ	=	0
Example 2:	Before Instru		
	REG1	7 =	2
	W	=	2
	Jun CON	_	?
			0

After Instruction

REG1

After Instruction

REG1 0 W 2

С 1: result is zero Z

Example 3: Before Instruction

> REG1 W 2 С Z

After Instruction

REG1 0xFF W 2

С 0; result is negative 0; = 0

Z

TRIS	Load TRIS Register
Syntax:	[label] TRIS f
Operands:	5 ≤ f ≤ 7
Operation:	(W) \rightarrow TRIS register f;
Status Affected:	None
Encoding:	00 0000 0110 Of
Description:	The instruction is supported for co- compatibility with the PIC16C5X p ucts. Since TRIS registers are rea- able and writable, the user can dir- address them.
Words:	M. I WW.
Cycles:	MITH WY
Example	
	To maintain upward compatibi with future PIC16CXX product

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XORLW	Exclusive OR Literal with W	XORWF	Exclusi	ve OR W	with f	
Syntax:	[<i>label</i>] XORLW k	Syntax:	[label]	XORWE	f,d	
Operands:	0 ≤ k ≤ 255	Operands:	$0 \le f \le 1$			
Operation:	(W) .XOR. $k \rightarrow (W)$		$d \in [0,1]$			
Status Affected:	ZWWW.100Y.CO.M.TW	Operation:		$R. (f) \rightarrow (f)$	destinati	on)
Encoding:	11 1010 kkkk kkkk	Status Affected:	Z.CO	TW		
Description:	The contents of the W register are	Encoding:	00	0110	dfff	ffff
Y.COM.TW	XOR'ed with the eight bit literal 'k'. The result is placed in the W register.	Description:	register v	OR the continuity of the conti	er 'f'. If 'd' i ne W regis	s 0 the ter. If 'd' is
Words:	1 COM.	Words:	N 1			3
Cycles:	1 W 1001. COM.	Cycles:	M.100.			
Q Cycle Activity:	Q1 Q2 Q3 Q4	Q Cycle Activity:	Q1	Q2	Q3	Q4
	Decode Read Process Write to data W	VITWO , IN W	Decode	Read register	Process data	Write to
Example:	XORLW 0xAF		LIVI.	T	OM	
W 100Y.CC	Before Instruction	Example	XORWF	REG	1011	
	W = 0xB5	CON.TW		nstruction	COM	
	After Instruction		MA.	REG		xAF
	W = 0x1A			W		xB5
			After Ins	truction		
				REG		x1A
				W	= 0:	xB5

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15.0 DEVELOPMENT SUPPORT

15.1 <u>Development Tools</u>

The PIC16/17 microcontrollers are supported with a full range of hardware and software development tools:

- PICMASTER/PICMASTER CE Real-Time In-Circuit Emulator
- ICEPIC Low-Cost PIC16C5X and PIC16CXXX In-Circuit Emulator
- PRO MATE[®] II Universal Programmer
- PICSTART® Plus Entry-Level Prototype Programmer
- PICDEM-1 Low-Cost Demonstration Board
- PICDEM-2 Low-Cost Demonstration Board
- PICDEM-3 Low-Cost Demonstration Board
- MPASM Assembler
- MPLAB-SIM Software Simulator
- MPLAB-C (C Compiler)
- Fuzzy logic development system (fuzzyTECH®-MP)

15.2 <u>PICMASTER: High Performance</u> <u>Universal In-Circuit Emulator with</u> MPLAB IDE

The PICMASTER Universal In-Circuit Emulator is intended to provide the product development engineer with a complete microcontroller design tool set for all microcontrollers in the PIC12C5XX, PIC14C000, PIC16C5X, PIC16CXXX and PIC17CXX families. PICMASTER is supplied with the MPLAB™ Integrated Development Environment (IDE), which allows editing, "make" and download, and source debugging from a single environment.

Interchangeable target probes allow the system to be easily reconfigured for emulation of different processors. The universal architecture of the PICMASTER allows expansion to support all new Microchip microcontrollers.

The PICMASTER Emulator System has been designed as a real-time emulation system with advanced features that are generally found on more expensive development tools. The PC compatible 386 (and higher) machine platform and Microsoft Windows® 3.x environment were chosen to best make these features available to you, the end user.

A CE compliant version of PICMASTER is available for European Union (EU) countries.

15.3 <u>ICEPIC: Low-cost PIC16CXXX</u> In-Circuit Emulator

ICEPIC is a low-cost in-circuit emulator solution for the Microchip PIC16C5X and PIC16CXXX families of 8-bit OTP microcontrollers.

ICEPIC is designed to operate on PC-compatible machines ranging from 286-AT[®] through Pentium™ based machines under Windows 3.x environment. ICEPIC features real time, non-intrusive emulation.

15.4 PRO MATE II: Universal Programmer

The PRO MATE II Universal Programmer is a full-featured programmer capable of operating in stand-alone mode as well as PC-hosted mode.

The PRO MATE II has programmable VDD and VPP supplies which allows it to verify programmed memory at VDD min and VDD max for maximum reliability. It has an LCD display for displaying error messages, keys to enter commands and a modular detachable socket assembly to support various package types. In standalone mode the PRO MATE II can read, verify or program PIC16C5X, PIC16CXXX, PIC17CXX and PIC14000 devices. It can also set configuration and code-protect bits in this mode.

15.5 <u>PICSTART Plus Entry Level</u> <u>Development System</u>

The PICSTART programmer is an easy-to-use, low-cost prototype programmer. It connects to the PC via one of the COM (RS-232) ports. MPLAB Integrated Development Environment software makes using the programmer simple and efficient. PICSTART Plus is not recommended for production programming.

PICSTART Plus supports all PIC12C5XX, PIC14000, PIC16C5X, PIC16CXXX and PIC17CXX devices with up to 40 pins. Larger pin count devices such as the PIC16C923 and PIC16C924 may be supported with an adapter socket.

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15.6 PICDEM-1 Low-Cost PIC16/17 Demonstration Board

The PICDEM-1 is a simple board which demonstrates the capabilities of several of Microchip's microcontrollers. The microcontrollers supported are: PIC16C5X (PIC16C54 to PIC16C58A), PIC16C61, PIC16C62X, PIC16C71, PIC16C8X, PIC17C42, PIC17C43 and PIC17C44. All necessary hardware and software is included to run basic demo programs. The users can program the sample microcontrollers provided with the PICDEM-1 board, on a PRO MATE II or PICSTART-16B programmer, and easily test firmware. The user can also connect the PICDEM-1 board to the PICMASTER emulator and download the firmware to the emulator for testing. Additional prototype area is available for the user to build some additional hardware and connect it to the microcontroller socket(s). Some of the features include an RS-232 interface, a potentiometer for simulated analog input, push-button switches and eight LEDs connected to PORTB.

15.7 PICDEM-2 Low-Cost PIC16CXX Demonstration Board

The PICDEM-2 is a simple demonstration board that supports the PIC16C62, PIC16C64, PIC16C65, PIC16C73 and PIC16C74 microcontrollers. All the necessary hardware and software is included to run the basic demonstration programs. The user can program the sample microcontrollers provided with the PICDEM-2 board, on a PRO MATE II programmer or PICSTART-16C, and easily test firmware. The PICMASTER emulator may also be used with the PICDEM-2 board to test firmware. Additional prototype area has been provided to the user for adding additional hardware and connecting it to the microcontroller socket(s). Some of the features include a RS-232 interface, push-button switches, a potentiometer for simulated analog input, a Serial EEPROM to demonstrate usage of the I2C bus and separate headers for connection to an LCD module and a keypad.

15.8 PICDEM-3 Low-Cost PIC16CXXX Demonstration Board

The PICDEM-3 is a simple demonstration board that supports the PIC16C923 and PIC16C924 in the PLCC package. It will also support future 44-pin PLCC microcontrollers with a LCD Module. All the necessary hardware and software is included to run the basic demonstration programs. The user can program the sample microcontrollers provided with the PICDEM-3 board, on a PRO MATE II programmer or PICSTART Plus with an adapter socket, and easily test firmware. The PICMASTER emulator may also be used with the PICDEM-3 board to test firmware. Additional prototype area has been provided to the user for adding hardware and connecting it to the microcontroller socket(s). Some of the features include

an RS-232 interface, push-button switches, a potentiometer for simulated analog input, a thermistor and separate headers for connection to an external LCD module and a keypad. Also provided on the PICDEM-3 board is an LCD panel, with 4 commons and 12 segments, that is capable of displaying time, temperature and day of the week. The PICDEM-3 provides an additional RS-232 interface and Windows 3.1 software for showing the demultiplexed LCD signals on a PC. A simple serial interface allows the user to construct a hardware demultiplexer for the LCD signals.

15.9 MPLAB Integrated Development Environment Software

The MPLAB IDE Software brings an ease of software development previously unseen in the 8-bit microcontroller market. MPLAB is a windows based application which contains:

- · A full featured editor
- · Three operating modes
 - editor
 - emulator
 - simulator
- A project manager
- Customizable tool bar and key mapping
- · A status bar with project information
- · Extensive on-line help

MPLAB allows you to:

- · Edit your source files (either assembly or 'C')
- One touch assemble (or compile) and download to PIC16/17 tools (automatically updates all project information)
- Debug using:
 - source files
 - absolute listing file
- Transfer data dynamically via DDE (soon to be replaced by OLE)
- · Run up to four emulators on the same PC

The ability to use MPLAB with Microchip's simulator allows a consistent platform and the ability to easily switch from the low cost simulator to the full featured emulator with minimal retraining due to development tools.

15.10 Assembler (MPASM)

The MPASM Universal Macro Assembler is a PC-hosted symbolic assembler. It supports all microcontroller series including the PIC12C5XX, PIC14000, PIC16C5X, PIC16CXXX, and PIC17CXX families.

MPASM offers full featured Macro capabilities, conditional assembly, and several source and listing formats. It generates various object code formats to support Microchip's development tools as well as third party programmers.

MPASM allows full symbolic debugging from PICMASTER, Microchip's Universal Emulator System.

MPASM has the following features to assist in developing software for specific use applications.

- Provides translation of Assembler source code to object code for all Microchip microcontrollers.
- · Macro assembly capability.
- Produces all the files (Object, Listing, Symbol, and special) required for symbolic debug with Microchip's emulator systems.
- Supports Hex (default), Decimal and Octal source and listing formats.

MPASM provides a rich directive language to support programming of the PIC16/17. Directives are helpful in making the development of your assemble source code shorter and more maintainable.

15.11 Software Simulator (MPLAB-SIM)

The MPLAB-SIM Software Simulator allows code development in a PC host environment. It allows the user to simulate the PIC16/17 series microcontrollers on an instruction level. On any given instruction, the user may examine or modify any of the data areas or provide external stimulus to any of the pins. The input/output radix can be set by the user and the execution can be performed in; single step, execute until break, or in a trace mode.

MPLAB-SIM fully supports symbolic debugging using MPLAB-C and MPASM. The Software Simulator offers the low cost flexibility to develop and debug code outside of the laboratory environment making it an excellent multi-project software development tool.

15.12 C Compiler (MPLAB-C)

The MPLAB-C Code Development System is a complete 'C' compiler and integrated development environment for Microchip's PIC16/17 family of microcontrollers. The compiler provides powerful integration capabilities and ease of use not found with other compilers.

For easier source level debugging, the compiler provides symbol information that is compatible with the MPLAB IDE memory display (PICMASTER emulator software versions 1.13 and later).

15.13 <u>Fuzzy Logic Development System</u> (fuzzyTECH-MP)

fuzzyTECH-MP fuzzy logic development tool is available in two versions - a low cost introductory version, MP Explorer, for designers to gain a comprehensive working knowledge of fuzzy logic system design; and a full-featured version, fuzzyTECH-MP, edition for implementing more complex systems.

Both versions include Microchip's $fuzzyLAB^{\text{TM}}$ demonstration board for hands-on experience with fuzzy logic systems implementation.

15.14 <u>MP-DriveWay™ – Application Code</u> Generator

MP-DriveWay is an easy-to-use Windows-based Application Code Generator. With MP-DriveWay you can visually configure all the peripherals in a PIC16/17 device and, with a click of the mouse, generate all the initialization and many functional code modules in C language. The output is fully compatible with Microchip's MPLAB-C C compiler. The code produced is highly modular and allows easy integration of your own code. MP-DriveWay is intelligent enough to maintain your code through subsequent code generation.

15.15 <u>SEEVAL® Evaluation and Programming System</u>

The SEEVAL SEEPROM Designer's Kit supports all Microchip 2-wire and 3-wire Serial EEPROMs. The kit includes everything necessary to read, write, erase or program special features of any Microchip SEEPROM product including Smart Serials™ and secure serials. The Total Endurance™ Disk is included to aid in trade-off analysis and reliability calculations. The total kit can significantly reduce time-to-market and result in an optimized system.

15.16 <u>TrueGauge® Intelligent Battery</u> Management

The TrueGauge development tool supports system development with the MTA11200B TrueGauge Intelligent Battery Management IC. System design verification can be accomplished before hardware prototypes are built. User interface is graphically-oriented and measured data can be saved in a file for exporting to Microsoft Excel.

15.17 <u>KeeLoq® Evaluation and</u> <u>Programming Tools</u>

KEELOQ evaluation and programming tools support Microchips HCS Secure Data Products. The HCS evaluation kit includes an LCD display to show changing codes, a decoder to decode transmissions, and a programming interface to program test transmitters.

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TABLE 15-1: DEVELOPMENT TOOLS FROM MICROCHIP

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	PIC12C5XX	PIC14000	PIC16C5X	PIC16CXXX	PIC16C6X	PIC16C7XX	PIC16C8X	PIC16C9XX	PIC17C4X	PIC17C75X	24CXX 25CXX 93CXX	HCS200 HCS300
PICMASTER®/ PICMASTER-CE In-Circuit Emulator	7	2	1 7 1.	MMA MMA	^{LM} . 7 0, M:700	.10031 10031	10X.C	CO) CO Z I	^{DM} 7 . W.T.A	Available 3Q97		
ICEPIC Low-Cost In-Circuit Emulator	WY WW	WWW.	WW.100	7 100 Z 100 Z 100 Z	00X.COV	COM.	M.TV M.TY M.TY	I.TW	N	1	W	
MPLAB™ Integrated Development Environment	(A) 100 (A) 100 (A) 100 A)	100X.CC	0X.CON	COMY.	MIN MIN	LM 7	7	7	MAN	VVVVV	W.100	V.100Y.
MPLAB™ C Compiler	. 5 ° y.c	201 07 ₁	TV	CAN N	7	7	N		M.50	100. 002	Y.C	CO
fuzzyTECH®-MP Explorer/Edition Fuzzy Logic Dev. Tool	M.TW OM.TV	LIN 7	W 7	7	WW	MAIA MAA'I	WW.100°	A:100.7.	104.CO	COM.	OM.TV	MTW
MP-DriveWay™ Applications Code Generator	I .	,	47	MM.	7.10° 71.20° 71.10°	100 7 00X.c	07.00 7.00	COM:	W.Z.	TW.	(N	
Total Endurance™ Software Model	N	NW	N.1	1.10 100 100	Y.C	.CO	M.	TW.	N		7	W
PICSTART® Lite Ultra Low-Cost Dev. Kit	WW.	W.100	1007. 1007.	Y.CO	ON.	MT.I MT.I	TW.	N		WW	MAIA	NW.1
PICSTART® Plus Low-Cost Universal Dev. Kit	1002; 1002;	V.CO	COM:	M.Y M.Y	ZWT.	7	7	121 M.W.	MAN	M.70	100 ^X	1007.C
PRO MATE® II Universal Programmer	COM:	OW.I	EN EVI ETV	W 7	7	1 7 .	MAN	MM.) LM.70	100 5 10 3 3 100	00X) 0X'Cr	Y.C.P.I	ON
KEELOQ® Programmer	TV 1.T	V			W	W	100 (1.10)	00Y.	CO V.C	OM	1.T	TH
SEEVAL® Designers Kit	N		1	W	N.Y	100)4.C	7.CC	OM: NT:	TW	7	
PICDEM-1		N	7	7.	.10°	V.C		M.T	7 F.			
PICDEM-2	1 2 4		N.I	700 700	7	S	W.	3 2 2				
PICDEM-3	NV NV		10°	Y.C	70 70 0	W.	TY.	\				
KEELOQ® Evaluation Kit	N.Y	100	7. K	CO	M.T	TW	N					7

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16.0 ELECTRICAL CHARACTERISTICS FOR PIC16C61

Absolute Maximum Ratings †

Ambient temperature under bias	55°C to +125°C
Storage temperature	65°C to +150°C
Voltage on any pin with respect to Vss (except VDD, MCLR, and RA4)	0.3V to (VDD + 0.3V)
Voltage on VDD with respect to Vss	0.3V to +7.5V
Voltage on MCLR with respect to Vss (Note 2)	
Voltage on RA4 pin with respect to Vss	0V to +14V
Total power dissipation (Note 1)	
Maximum current out of Vss pin	150 mA
Maximum current into VDD pin	100 mA
Input clamp current, liκ (Vi < 0 or Vi > VDD)	
Output clamp current, loκ (Vo < 0 or Vo > VDD)	
Maximum output current sunk by any I/O pin	25 mA
Maximum output current sourced by any I/O pin	20 mA
Maximum current sunk by PORTA	80 mA
Maximum current sourced by PORTA	
Maximum current sunk by PORTB	150 mA
Maximum current sourced by PORTB	

Note 1: Power dissipation is calculated as follows: Pdis = VDD x {IDD - Σ IOH} + Σ {(VDD-VOH) x IOH} + Σ (Vol x IOL)

Note 2: Voltage spikes below Vss at the \overline{MCLR} pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100 Ω should be used when applying a "low" level to the \overline{MCLR} pin rather than pulling this pin directly to Vss.

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 16-1: CROSS REFERENCE OF DEVICE SPECS FOR OSCILLATOR CONFIGURATIONS AND FREQUENCIES OF OPERATION (COMMERCIAL DEVICES)

osc	PIC16C61-04	PIC16C61-20	PIC16LC61-04	JW Devices
RC	VDD: 4.0V to 6.0V IDD: 3.3 mA max. at 5.5V IPD: 14 μA max. at 4V Freq: 4 MHz max.	VDD: 4.5V to 5.5V IDD: 1.8 mA typ. at 5.5V IPD: 1.0 μA typ. at 4V Freq: 4 MHz max.	VDD: 3.0V to 6.0V IDD: 1.4 mA typ. at 3.0V IPD: 0.6 μA typ. at 3V Freq: 4 MHz max.	VDD: 4.0V to 6.0V IDD: 3.3 mA max. at 5.5V IPD: 14 μA max. at 4V Freq: 4 MHz max.
XT	VDD: 4.0V to 6.0V IDD: 3.3 mA max. at 5.5V IPD: 14 μA max. at 4V Freq: 4 MHz max.	VDD: 4.5V to 5.5V IDD: 1.8 mA typ. at 5.5V IPD: 1.0 μA typ. at 4V Freq: 4 MHz max.	VDD: 3.0V to 6.0V IDD: 1.4 mA typ. at 3.0V IPD: 0.6 μA typ. at 3V Freq: 4 MHz max.	VDD: 4.0V to 6.0V IDD: 3.3 mA max. at 5.5V IPD: 14 μA max. at 4V Freq: 4 MHz max.
HS	VDD: 4.5V to 5.5V IDD: 13.5 mA typ. at 5.5V IPD: 1.0 μA typ. at 4.5V Freq: 4 MHz max.	VDD: 4.5V to 5.5V IDD: 30 mA max. at 5.5V IPD: 1.0 μA typ. at 4.5V Freq: 20 MHz max.	Not recommended for use in HS mode	VDD: 4.5V to 5.5V IDD: 30 mA max. at 5.5V IPD: 1.0 μA typ. at 4.5V Freq: 20 MHz max.
LP	VDD: 4.0V to 6.0V IDD: 15 μA typ. at 32 kHz, 4.0V IPD: 0.6 μA typ. at 4.0V Freq: 200 kHz max.	Not recommended for use in LP mode	VDD: 3.0V to 6.0V IDD: 32 μA max. at 32 kHz, 3.0V IPD: 9 μA max. at 3.0V Freq: 200 kHz max.	VDD: 3.0V to 6.0V IDD: 32 μA max. at 32 kHz, 3.0V IPD: 9 μA max. at 3.0V Freq: 200 kHz max.

The shaded sections indicate oscillator selections which are tested for functionality, but not for MIN/MAX specifications. It is recommended that the user select the device type that ensures the specifications required.

16.1 DC Characteristics: PIC16C61-04 (Commercial, Industrial, Extended) PIC16C61-20 (Commercial, Industrial, Extended)

DC CHARACTERISTICS Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C $\leq \text{TA} \leq +125^{\circ}\text{C}$ for extended, -40°C $\leq \text{TA} \leq +85^{\circ}\text{C}$ for industrial and 0°C $\leq \text{TA} \leq +70^{\circ}\text{C}$ for commercial

Param No.	Characteristic	Sym	Min	Typ†	Max	Units	Conditions
D001 D001A	Supply Voltage	VDD	4.0 4.5	TW	6.0 5.5	V	XT, RC and LP osc configuration HS osc configuration
D002*	RAM Data Retention Voltage (Note 1)	VDR	CO	1.5	-	>	NWW.100X.COM.TW
D003	VDD start voltage to ensure internal Power- on Reset signal	VPOR	N.EC	Vss	W TW	>	See section on Power-on Reset for details
D004*	VDD rise rate to ensure internal Power-on Reset signal	SVDD	0.05	CO_{N}	T.T.	V/ms	See section on Power-on Reset for details
D010 D013	Supply Current (Note 2)	lDD	N.100	1.8 13.5	3.3	mA mA	FOSC = 4 MHz, VDD = 5.5V (Note 4) HS osc configuration
D020	Down down Current	Inn	11.70	7	000		Fosc = 20 MHz, VDD = 5.5V
D020 D021 D021A	Power-down Current (Note 3)	IPD	$N_{M'}$	1.0 1.0	28 14 16	μΑ μΑ μΑ	VDD = 4.0V, WDT enabled, -40°C to +85°C VDD = 4.0V, WDT disabled, -0°C to +70°C VDD = 4.0V, WDT disabled, -40°C to +85°C
D021B	WT.V.	V	111	1.0	20	μΑ	VDD = 4.0V, WDT disabled, -40°C to +125°C

- * These parameters are characterized but not tested.
- † Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.
- Note 1: This is the limit to which VDD can be lowered without losing RAM data.
 - 2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
 - The test conditions for all IDD measurements in active operation mode are:
 - OSC1 = external square wave, from rail to rail; all I/O pins tristated, pulled to VDD,
 - MCLR = VDD; WDT enabled/disabled as specified.
 - 3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and Vss.
 - 4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kOhm.

16.2 DC Characteristics: PIC16LC61-04 (Commercial, Industrial)

DC CHA	ARACTERISTICS	Standa Operati	- 1			°C ≤	less otherwise stated) A ≤ +85°C for industrial and A ≤ +70°C for commercial		
Param No.	Characteristic	Sym	Min	Тур†	Max	Units	Conditions		
D001	Supply Voltage	VDD	3.0	-	6.0	V	XT, RC, and LP osc configuration		
D002*	RAM Data Retention Voltage (Note 1)	VDR	M.T	1.5	- <	V	V.100Y.COM.TW		
D003	VDD start voltage to ensure internal Power-on Reset signal	VPOR	OM.T	Vss	-	V	See section on Power-on Reset for details		
D004*	VDD rise rate to ensure internal Power-on Reset signal	SVDD	0.05	T.I	-	V/ms	See section on Power-on Reset for details		
D010	Supply Current (Note 2)	IDD	Y.CO	1.4	2.5	mA	Fosc = 4 MHz, VDD = 3.0V (Note 4)		
D010A	OM.TW WW	W.10	ov.C	15	32	μΑ	Fosc = 32 kHz, VDD = 3.0V, WDT disabled, LP osc configuration		
D020 D021 D021A	Power-down Current (Note 3)	IPD	109X	5 0.6 0.6	20 9 12	μΑ μΑ μΑ	VDD = 3.0V, WDT enabled, -40°C to +85°C VDD = 3.0V, WDT disabled, 0°C to +70°C VDD = 3.0V, WDT disabled, -40°C to +85°C		

- * These parameters are characterized but not tested.
- † Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.
- Note 1: This is the limit to which VDD can be lowered without losing RAM data.
 - 2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
 - The test conditions for all IDD measurements in active operation mode are:
 - OSC1 = external square wave, from rail to rail; all I/O pins tristated, pulled to VDD,
 - MCLR = VDD; WDT enabled/disabled as specified.
 - 3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and Vss.
 - 4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kOhm.

PIC16C6X

DC CHARACTERISTICS

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Applicable Devices 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

16.3 DC Characteristics: PIC16C61-04 (Commercial, Industrial, Extended) PIC16C61-20 (Commercial, Industrial, Extended)

PIC16LC61-04 (Commercial, Industrial)

Standard Operating Conditions (unless otherwise stated)

Operating temperature $-40^{\circ}\text{C} \leq \text{TA} \leq +125^{\circ}\text{C}$ for extended,

-40°C ≤ Ta ≤ +85°C for industrial and 0°C ≤ Ta ≤ +70°C for commercial

Operating voltage VDD range as described in DC spec Section 16.1 and

Section 16.2.

Param No.	Characteristic	Sym	Min	Тур†	Max	Units	Conditions
N.CO	Input Low Voltage	Co	WIN		11/11	- x 1 1 0	DY. COM. TW
	I/O ports	VIL	TW		WW		ONY.COMETW
D030	with TTL buffer	-7 C	Vss	. -	0.15VDD	V	For entire VDD range
D030A	M.TW WWW.	01.	Vss	-	0.8V	V	$4.5V \le VDD \le 5.5V$
D031	with Schmitt Trigger buffer	OOY.C	Vss	N -	0.2VDD	V	100Y.Cont.TW
D032	MCLR, OSC1 (in RC mode)	- 0V	Vss	αĪ	0.2VDD	V	V. CONTRACTIVE
D033	OSC1 (in XT, HS and LP)	100 r	Vss) Y	0.3VDD	V	Note1
	Input High Voltage	CI 100					WIOON. COM.TW
	I/O ports	VIH	V.COn	-	V		TW TW
D040	with TTL buffer	M.Jo.	2.0	11-	VDD	V	$4.5V \le VDD \le 5.5V$
D040A	100X.COM.TW WY	NW.19	0.25VDD + 0.8V	M.J	VDD	V	For entire VDD range
D041	with Schmitt Trigger buffer	MM.	0.85VDD	<u>-</u> 27	VDD	V	For entire VDD range
D042	MCLR	NWW	0.85VDD	$Car{\mathbf{o}}_{h}$	VDD	V	MANA TOOX CO.
D042A	OSC1 (XT, HS and LP)	-TXV	0.7VDD	<u>(4</u> 0	VDD	V	Note1
D043	OSC1 (in RC mode)	111.	0.9VDD	-	VDD	V	W.100 COM
D070	PORTB weak pull-up current	IPURB	50	250	† 400	μΑ	VDD = 5V, VPIN = VSS
4 1	Input Leakage Current (Notes 2, 3)		MAN.	nV.	JOE A	W	MM
D060	I/O ports	lıL.	MAN'I	00X	(±1)	μА	Vss ≤ VPIN ≤ VDD, Pin at hi- impedance
D061	MCLR, RA4/T0CKI	-	$M_{M_{*}}$		±5	μΑ	Vss ≤ VPIN ≤ VDD
D063	OSC1		MAM	7.70	±5	μА	$\label{eq:VSS} \mbox{$VPIN} \le \mbox{VDD, XT, HS and} \\ \mbox{LP osc configuration}$
	Output Low Voltage		MM	1	10 Y.Co	TIL	N 1100
D080	I/O ports	VOL	WW	W.I	0.6	V	IOL = 8.5 mA , VDD = 4.5V , -40°C to $+85^{\circ}\text{C}$
D080A	WWW.100Y.COM.T	W	-W	MA.	0.6	V	IOL = 7.0 mA, VDD = 4.5V, -40°C to +125°C
D083	OSC2/CLKOUT (RC osc config)	TW	- 1	NW	0.6	, Vo	IOL = 1.6 mA, VDD = 4.5V, -40°C to +85°C
D083A	WWW.Inc. CON	M.TW	-	WV	0.6	V	IOL = 1.2 mA, VDD = 4.5V, -40°C to +125°C

^{*} The parameters are characterized but not tested.

[†] Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C6X be driven with external clock in RC mode.

The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

^{3:} Negative current is defined as current sourced by the pin.

Standard Operating Conditions (unless otherwise stated)

Operating temperature $-40^{\circ}\text{C} \leq \text{TA} \leq +125^{\circ}\text{C}$ for extended,

-40°C ≤ TA ≤ +85°C for industrial and

 0° C $\leq TA \leq +70^{\circ}$ C for commercial

Operating voltage VDD range as described in DC spec Section 16.1 and

Param	Characteristic	Section		Trend	Max	Units	Conditions
No.	Characteristic	Sym	Min	Typ†	Max	Units	Conditions
MIT	Output High Voltage			- 111	11.700	V C	NA.
D090	I/O ports (Note 3)	Vон	VDD-0.7	41.1	VVI-10	V	IOH = -3.0 mA, VDD = 4.5V, -40°C to +85°C
D090A	TW WWW.100Y.CO	$^{ m OM}_{ m M}$	VDD-0.7	-4	M.M.	ooy.	IOH = -2.5 mA, VDD = 4.5V, -40°C to +125°C
D092	OSC2/CLKOUT (RC osc config)	co_{M}	VDD-0.7	-		1V)	IOH = -1.3 mA, VDD = 4.5V, -40°C to +85°C
D092A	M.TW WW.100X	I.COJ	VDD-0.7	-	MM	V	IOH = -1.0 mA, VDD = 4.5V, -40°C to +125°C
D150*	Open-Drain High Voltage	Vod	- 11	-	14	V	RA4 pin
00X.	Capacitive Loading Specs on Output Pins	oy.C	MIT	V	W	WW.	100X.COM.TW
D100	OSC2 pin	Cosc ₂	COM'	TW TW	15	pF	In XT, HS and LP modes when external clock is used to drive OSC1.
D101	All I/O pins and OSC2 (in RC mode)	Cio	1 CO $_{M_{T}}$	TV	50	pF	W.T. COM. TW

* The parameters are characterized but not tested.

DC CHARACTERISTICS

- † Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.
- Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C6X be driven with external clock in RC mode.
 - 2: The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

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3: Negative current is defined as current sourced by the pin.

PIC16C6X

Applicable Devices 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

16.4 <u>Timing Parameter Symbology</u>

The timing parameter symbols have been created following one of the following formats:

1. TppS2ppS3. Tcc:st(I²C specifications only)2. TppS4. Ts(I²C specifications only)

T Time

Lowercase letters (pp) and their meanings:

pp	M MI 100X.C OM.TH		W. 1001.
СС	CCP1	osc	OSC1
ck	CLKOUT	rd	RD
cs	CS	rw	RD or WR
di	SDI	sc	SCK
do CO	SDO	SS	SS
dt	Data in	tO	TOCKI CONTRACTOR OF THE PROPERTY OF THE PROPER
io	I/O port	t1	T1CKI
mc	MCLR	wr	WR

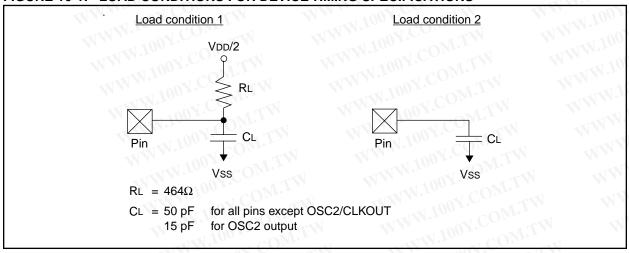
Uppercase letters and their meanings:

S		$O_{M^{*}}$	COM.
F 100	Fall	P	Period
H	High	R	Rise
WW.10	Invalid (Hi-impedance)	(A)	Valid
L 71/10	Low	ZOM	Hi-impedance Control of the Hi-impedance
I ² C only		Moon	IN M. 1001. COWIT.
AA	output access	High	High
BUF	Bus free	Low	Low

Tcc:st (I²C specifications only)

CC	31 100x. CM.TW	100 .	ON: I COL
HD	Hold	SU	Setup
ST		V. I	
DAT	DATA input hold	STO	STOP condition
STA	START condition	100	

FIGURE 16-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS



16.5 <u>Timing Diagrams and Specifications</u>

FIGURE 16-2: EXTERNAL CLOCK TIMING

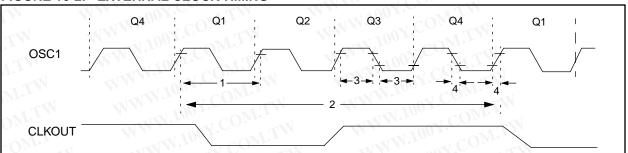


TABLE 16-2: EXTERNAL CLOCK TIMING REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Тур†	Max	Units	Conditions
V.Co	Fosc	External CLKIN Frequency	DC	_	4	MHz	XT and RC osc mode
	TW	(Note 1)	DC	_	4	MHz	HS osc mode (-04)
	1.1	I TWW.Incox.CO	DC	N —	20	MHz	HS osc mode (-20)
	$M_{J,J,A}$	W.100 2	DC	T	200	kHz	LP osc mode
	MI	Oscillator Frequency	DC	1.1.1.	4	MHz	RC osc mode
	771-	(Note 1)	0.1	TW	4	MHz	XT osc mode
	OM	WWW.IOOY	C4	N ew	4	MHz	HS osc mode (-04)
W.100 1	coM	11. M. 100	(10)	1. <u>-</u>	20	MHz	HS osc mode (-20)
1001	Tosc	External CLKIN Period	250	M	_	ns	XT and RC osc mode
MM.1001	I.Co.	(Note 1)	250	ONA T	Y -	ns	HS osc mode (-04)
	N.CU	WWW.	50	- X 1	W-	ns	HS osc mode (-20)
	N.C	OM.	5	$CO_{\overline{N}r}$.	rv l	μs	LP osc mode
)U 1.	Oscillator Period	250	ce_{M}	- T	ns	RC osc mode
	$100 \chi_{\odot}$	(Note 1)	250	(OD)	10,000	ns	XT osc mode
	1007	WITH WITH	250	Y. <u>—</u>	1,000	ns	HS osc mode (-04)
	1.10	K.COM. TW WW.	50	ON-CU	1,000	ns	HS osc mode (-20)
	W.700	TCOM.	5	~ √ .C	ON-	μs	LP osc mode
2	Tcy	Instruction Cycle Time (Note 1)	1.0	Tcy	DC	μs	Tcy = 4/Fosc
3	TosL,	External Clock in (OSC1) High or	50	$70\overline{\sigma}_{J_{\perp}}$	COM	ns	XT oscillator
	TosH	Low Time	2.5	100Y	-	μs	LP oscillator
	WW	. CON.	10	7. 2 00.	$V \subset \overline{\Omega}_{p_{r}}$	ns	HS oscillator
4	TosR,	External Clock in (OSC1) Rise or	25	11700	V.CO	ns	XT oscillator
	TosF	Fall Time	50	4.10	2 TCC	ns	LP oscillator
	WW	TOOY	15		007	ns	HS oscillator

[†] Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (TCY) equals four times the input oscillator time-base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1/CLKIN pin. When an external clock input is used, the "Max." cycle time limit is "DC" (no clock) for all devices.

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FIGURE 16-3: CLKOUT AND I/O TIMING

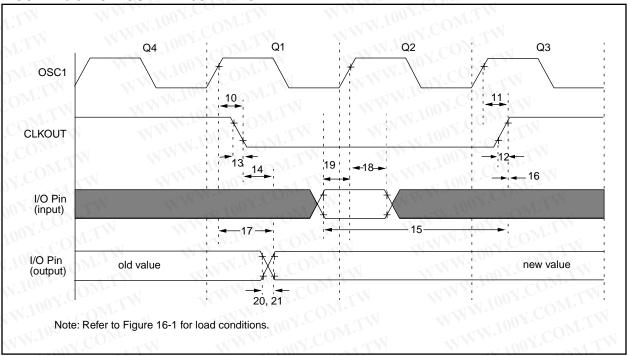


TABLE 16-3: CLKOUT AND I/O TIMING REQUIREMENTS

Parameter No.	Sym	Characteristic	W.100Y.C	Min	Тур†	Max	Units	Conditions
10*	TosH2ckL	OSC1↑ to CLKOUT↓	OSC1↑ to CLKOUT↓		15	30	ns	Note 1
11*	TosH2ckH	OSC1↑ to CLKOUT↑	OSC1↑ to CLKOUT↑		15	30	ns	Note 1
12*	TckR	CLKOUT rise time	1003	TITY	5	15	ns	Note 1
13*	TckF	CLKOUT fall time	CLKOUT fall time		5	15	ns	Note 1
14*	TckL2ioV	CLKOUT ↓ to Port out valid		V.COM.	r W	0.5Tcy + 20	ns	Note 1
15*	TioV2ckH	Port in valid before CLKOUT ↑ 0		0.25Tcy + 25		-	ns	Note 1
16*	TckH2ioI	Port in hold after CLKOUT ↑		0-0	I.E.	. –	ns	Note 1
17*	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid		1007	17	80 - 100	ns	W.100.
18*	TosH2iol	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)		TBD	n t T		ns	MN.100
19*	TioV2osH	Port input valid to OSC1 time)	↑ (I/O in setup	TBD	$O_{\overline{D}_{\overline{I}}}$	TW	ns	WWI
20*	TioR	Port output rise time	PIC16 C 61	100X	10	25	ns	MM
	WWW	VION COMP.	PIC16 LC 61	M. John		60	ns	MAIN
21*	TioF	Port output fall time	PIC16 C 61	MA Jan	10	25	ns	WWW
	W.	M.100x.COM.	PIC16 LC 61	10 N. 10	<u>*</u> (60	ns	
22††*	Tinp	RB0/INT pin high or low	time	20	10 x.	COMITY	ns	77
23††*	Trbp	RB7:RB4 change int hig	h or low time	20	007	-1.T	ns	1/1/1

Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

These parameters are asynchronous events not related to any internal clock edges. ††

Note 1: Measurements are taken in RC Mode where CLKOUT output is 4 x Tosc.

FIGURE 16-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING

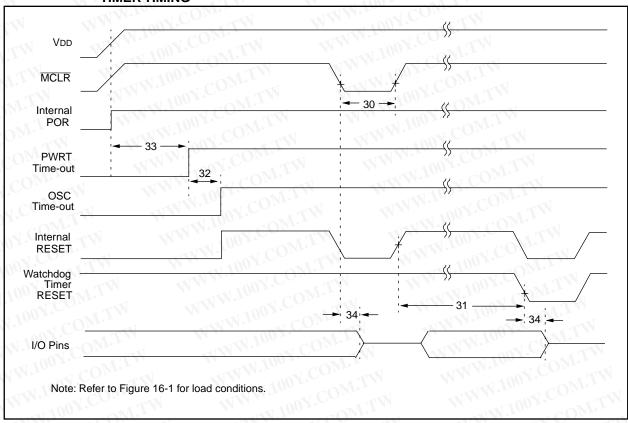


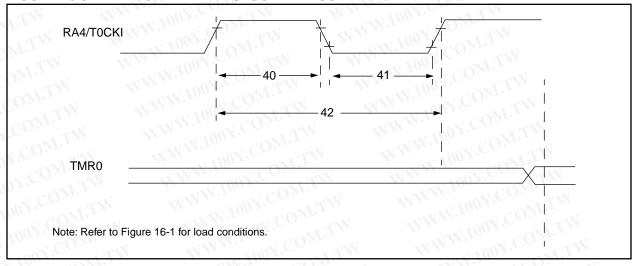
TABLE 16-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
30*	TmcL	MCLR Pulse Width (low)	200	MOM.	1.4.	ns	VDD = 5V, -40°C to +125°C
31*	Twdt	Watchdog Timer Time-out Period (No Prescaler)	710	18	33	ms	$VDD = 5V, -40^{\circ}C \text{ to } +125^{\circ}C$
32	Tost	Oscillation Start-up Timer Period	$M_{\overline{M}^{-1}}$	1024Tosc		N	Tosc = OSC1 period
33*	Tpwrt	Power-up Timer Period	28	72	132	ms	VDD = 5V, -40°C to +125°C
34*	Tıoz	I/O Hi-impedance from MCLR Low		1.100	100	ns	MIN'IOU

^{*} These parameters are characterized but not tested.

[†] Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 16-5: TIMERO EXTERNAL CLOCK TIMINGS



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TABLE 16-5: TIMERO EXTERNAL CLOCK REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Тур†	Max	Units	Conditions	
40*	TtOH	T0CKI High Pulse Width	No Prescaler	0.5Tcy + 20	=	N I N	ns	Must also meet parameter 42
	1.0	M.T.N.	With Prescaler	10		-31	ns	
41* T	Tt0L	T0CKI Low Pulse Width	No Prescaler	0.5Tcy + 20	_1	NY	ns	Must also meet parameter 42
			With Prescaler	10	_	VAN	ns	
42*	Tt0P	T0CKI Period	No Prescaler	Tcy + 40	_	- T	ns	N = prescale value (2, 4,, 256)
	1.700 1002	V.COM.TW	With Prescaler	Greater of: 20 ns or TCY + 40 N	_		ns	

^{*} These parameters are characterized but not tested.

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[†] Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

17.0 DC AND AC CHARACTERISTICS GRAPHS AND TABLES FOR PIC16C61

The graphs and tables provided in this section are for design guidance and are not tested or guaranteed.

In some graphs or tables the data presented are outside specified operating range (i.e., outside specified VDD range). This is for information only and devices are guaranteed to operate properly only within the specified range.

Note: The data presented in this section is a statistical summary of data collected on units from different lots over a period of time and matrix samples. 'Typical' represents the mean of the distribution while 'max' or 'min' represents (mean +3σ) and (mean -3σ) respectively where σ is standard deviation.

FIGURE 17-1: TYPICAL RC OSCILLATOR FREQUENCY vs. TEMPERATURE

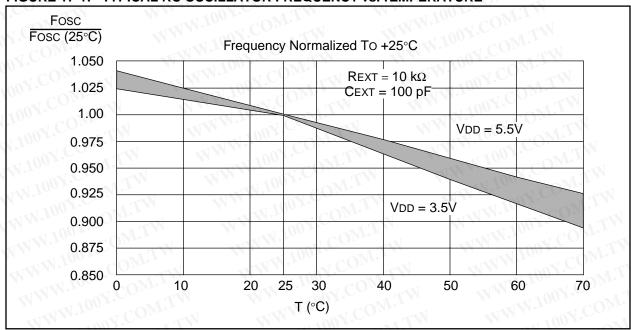


TABLE 17-1: RC OSCILLATOR FREQUENCIES

Cext 20 pF	Rext 4.7k	Average Fosc @ 5V, 25°C	
		4.52 MHz	± 17.35%
	10k	2.47 MHz	± 10.10%
	100k	290.86 kHz	± 11.90%
100 pF	3.3k	1.92 MHz	± 9.43%
	4.7k	1.48 MHz	± 9.83%
	10k	788.77 kHz	± 10.92%
WW.	100k	88.11 kHz	± 16.03%
300 pF	3.3k	726.89 kHz	± 10.97%
	4.7k	573.95 kHz	± 10.14%
	10k	307.31 kHz	± 10.43%
	100k	33.82 kHz	± 11.24%

The percentage variation indicated here is part to part variation due to normal process distribution. The variation indicated is ± 3 standard deviation from average value for VDD = 5V.

FIGURE 17-2: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD

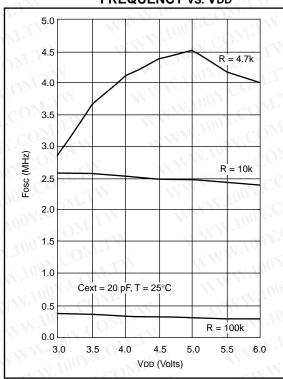


FIGURE 17-3: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD

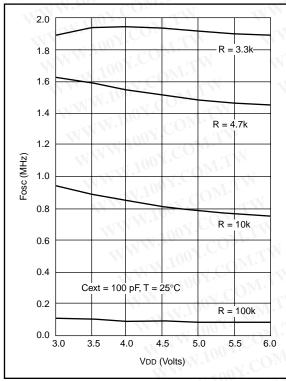


FIGURE 17-4: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD

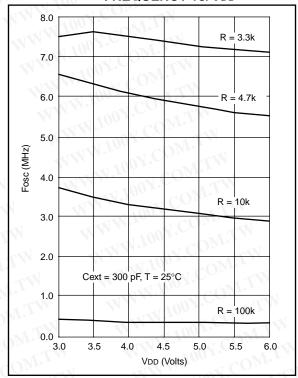
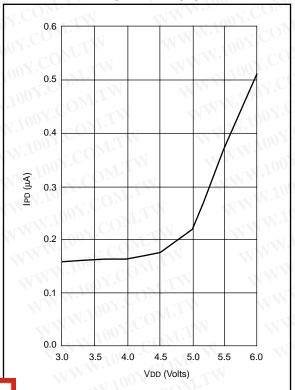


FIGURE 17-5: TYPICAL IPD VS. VDD WATCHDOG TIMER DISABLED 25°C

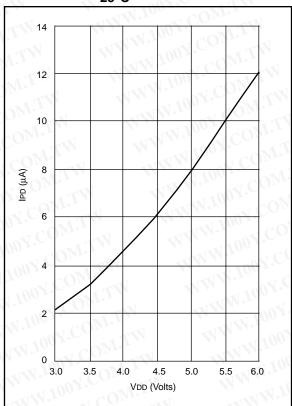


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Data based on matrix samples. See first page of this section for details.

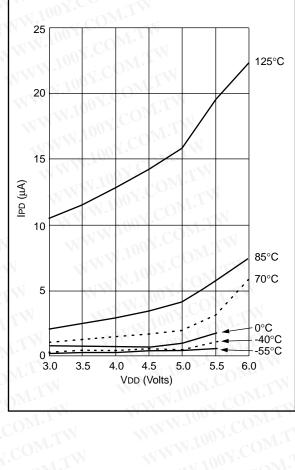
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FIGURE 17-6: TYPICAL IPD vs. VDD **WATCHDOGTIMER ENABLED** 25°C



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FIGURE 17-7: MAXIMUM IPD vs. VDD WATCHDOG DISABLED



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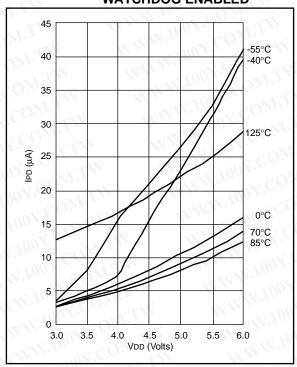
samples.

matrix

o based

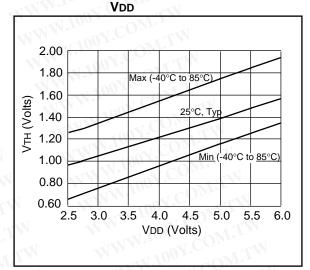
Data

FIGURE 17-8: MAXIMUM IPD vs. VDD WATCHDOG ENABLED*



*IPD, with Watchdog Timer enabled, has two components: The leakage current which increases with higher temperature and the operating current of the Watchdog Timer logic which increases with lower temperature. At -40°C, the latter dominates explaining the apparently anomalous behavior.

FIGURE 17-9: VTH (INPUT THRESHOLD VOLTAGE) OF I/O PINS vs.



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FIGURE 17-10: VIH, VIL OF MCLR, TOCKI AND OSC1 (IN RC MODE) vs. VDD

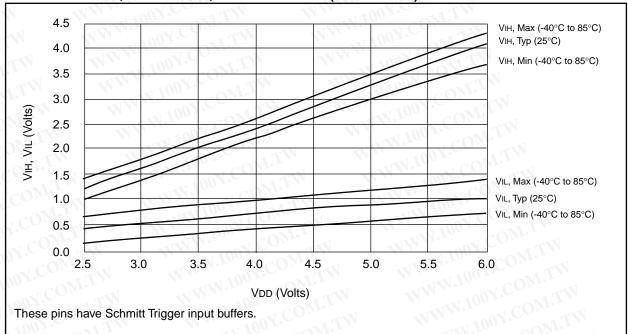


FIGURE 17-11: VTH (INPUT THRESHOLD VOLTAGE) OF OSC1 INPUT (IN XT, HS, AND LP MODES) vs. Vdd

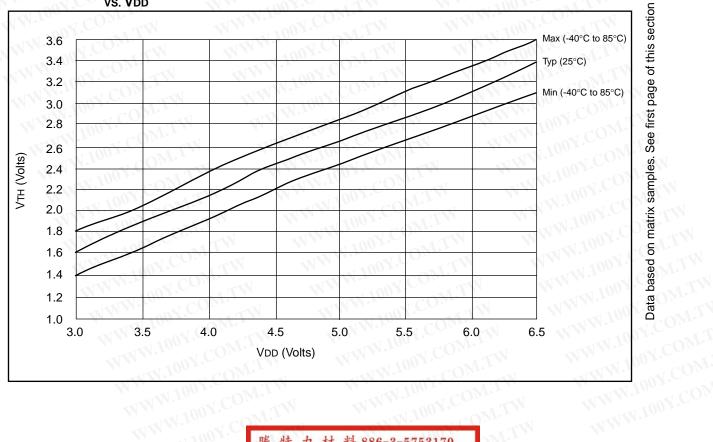


FIGURE 17-12: TYPICAL IDD vs. FREQUENCY (EXTERNAL CLOCK, 25°C)

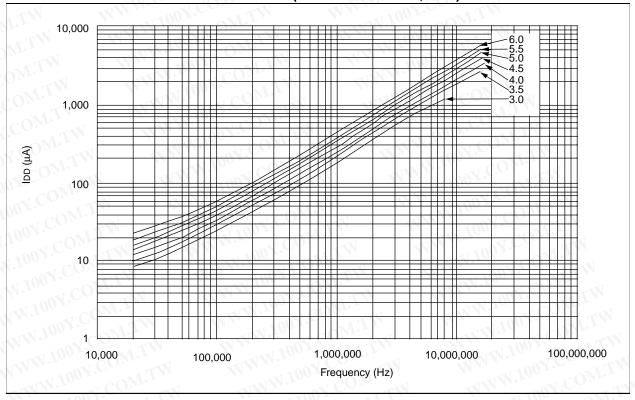


FIGURE 17-13: MAXIMUM IDD vs. FREQUENCY (EXTERNAL CLOCK, -40° TO +85°C)

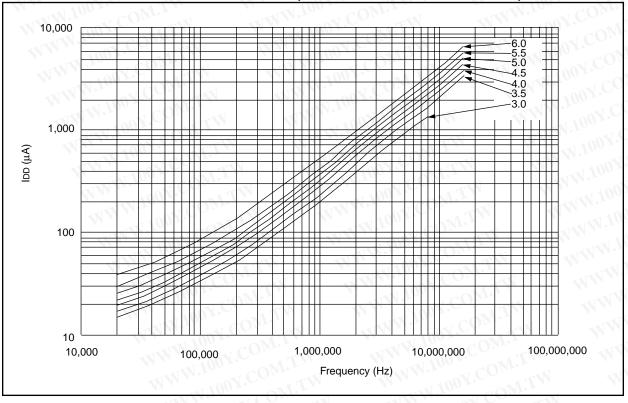


FIGURE 17-14: MAXIMUM IDD VS. FREQUENCY (EXTERNAL CLOCK, -55° TO +125°C)

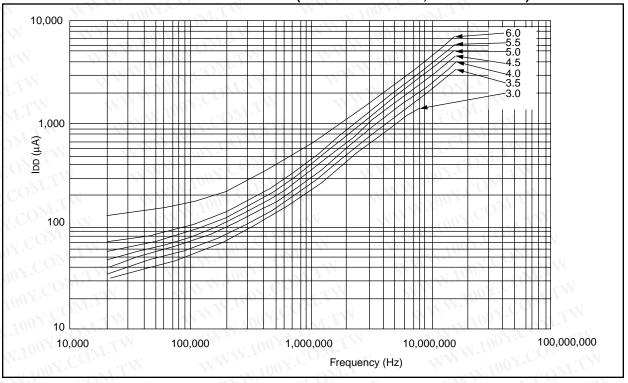


FIGURE 17-15: WDT TIMER TIME-OUT PERIOD vs. VDD

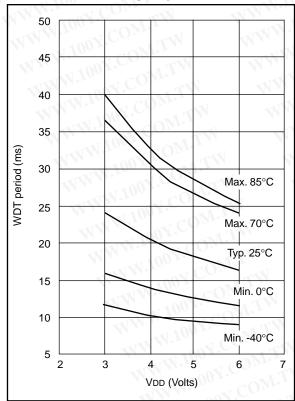
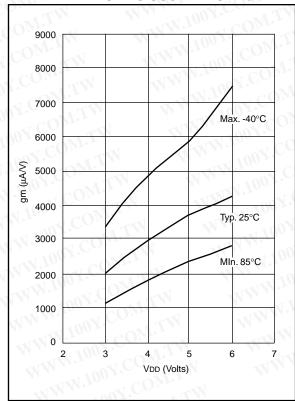


FIGURE 17-16: TRANSCONDUCTANCE (gm)
OF HS OSCILLATOR vs. VDD



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FIGURE 17-17: TRANSCONDUCTANCE (gm) OF LP OSCILLATOR vs. VDD

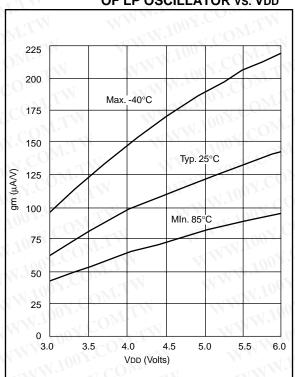


FIGURE 17-18: TRANSCONDUCTANCE (gm)
OF XT OSCILLATOR vs. VdD

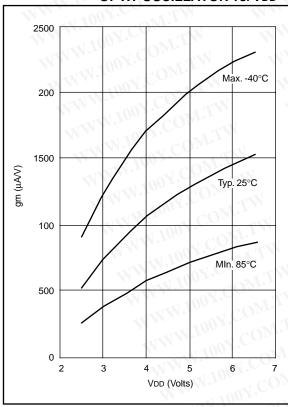


FIGURE 17-19: IOH VS. VOH, VDD = 3V

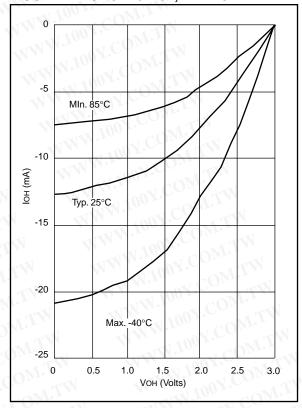


FIGURE 17-20: IOH VS. VOH, VDD = 5V

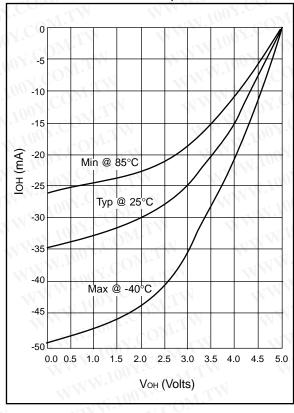


FIGURE 17-21: IOL VS. VOL, VDD = 3V

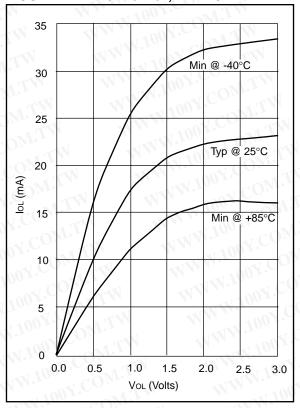


FIGURE 17-22: IOL VS. VOL, VDD = 5V

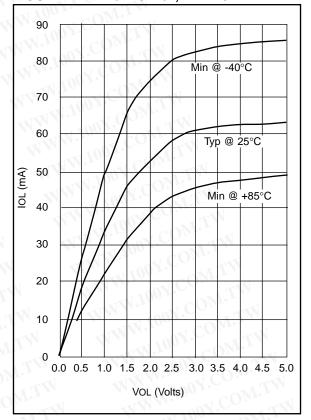


TABLE 17-2: INPUT CAPACITANCE*

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Pin Name	Typical Capacitance (pF)						
	18L PDIP	18L SOIC					
RA port	5.0	4.3					
RB port	5.0	4.3					
MCLR	17.0	17.0					
OSC1/CLKIN	4.0	3.5					
OSC2/CLKOUT	4.3	3.5					
TOCKI	3.2	2.8					

^{*}All capacitance values are typical at 25° C. A part to part variation of $\pm 25\%$ (three standard deviations) should be taken into account.

Data based on matrix samples. See first page of this section for details.

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WWW.100Y.COM.TW

MMM:100

100Y.COM.TW

TIMEN 100X.COM.

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18.0 ELECTRICAL CHARACTERISTICS FOR PIC16C62/64

Absolute Maximum Ratings †

Ambient temperature under bias	55°C to +85°C
Storage temperature	65°C to +150°C
Voltage on any pin with respect to Vss (except VDD, MCLR, and RA4)	
Voltage on VDD with respect to Vss	-0.3V to +7.5V
Voltage on MCLR with respect to Vss (Note 2)	
Voltage on RA4 with respect to Vss	0V to +14V
Total power dissipation (Note 1)	1.0W
Maximum current out of Vss pin	
Maximum current into VDD pin	250 mA
Input clamp current, lik (Vi < 0 or Vi > VDD)	±20 mA
Output clamp current, lok (Vo < 0 or Vo > VDD)	±20 mA
Maximum output current sunk by any I/O pin	
Maximum output current sourced by any I/O pin	25 mA
Maximum current sunk by PORTA, PORTB, and PORTE* (combined)	200 mA
Maximum current sourced by PORTA, PORTB, and PORTE* (combined)	200 mA
Maximum current sunk by PORTC and PORTD* (combined)	200 mA
Maximum current sourced by PORTC and PORTD* (combined)	200 mA
* PORTD and PORTE not available on the PIC16C62.	

Note 1: Power dissipation is calculated as follows: Pdis = VDD x {IDD - Σ IOH} + Σ {(VDD-VOH) x IOH} + Σ (VOI x IOL)

Note 2: Voltage spikes below Vss at the \overline{MCLR} pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100 Ω should be used when applying a "low" level to the \overline{MCLR} pin rather than pulling this pin directly to Vss.

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 18-1: CROSS REFERENCE OF DEVICE SPECS FOR OSCILLATOR CONFIGURATIONS AND FREQUENCIES OF OPERATION (COMMERCIAL DEVICES)

osc	PIC16C62-04 PIC16C64-04	PIC16C62-10 PIC16C64-10	PIC16C62-20 PIC16C64-20	PIC16LC62-04 PIC16LC64-04	JW Devices
RC	VDD: 4.0V to 6.0V IDD: 3.8 mA max. at 5.5V IPD: 21 µA max. at 4V Freq:4 MHz max.	VDD: 4.5V to 5.5V IDD: 2.0 mA typ. at 5.5V IPD: 1.5 μA typ. at 4V Freq:4 MHz max.	VDD: 4.5V to 5.5V IDD: 2.0 mA typ. at 5.5V IPD: 1.5 μA typ. at 4V Freq:4 MHz max.	VDD: 3.0V to 6.0V IDD: 3.8 mA max. at 3.0V IPD: 13.5 μA max. at 3V Freq: 4 MHz max.	VDD: 4.0V to 6.0V IDD: 3.8 mA max. at 5.5V IPD: 21 μA max. at 4V Freq:4 MHz max.
XT	VDD: 4.0V to 6.0V IDD: 3.8 mA max. at 5.5V IPD: 21 μA max. at 4V Freq:4 MHz max.	VDD: 4.5V to 5.5V IDD: 2.0 mA typ. at 5.5V IPD: 1.5 μA typ. at 4V Freq:4 MHz max.	VDD: 4.5V to 5.5V IDD: 2.0 mA typ. at 5.5V IPD: 1.5 μA typ. at 4V Freq:4 MHz max.	VDD: 3.0V to 6.0V IDD: 3.8 mA max. at 3.0V IPD: 13.5 μA max. at 3.0V Freq: 4 MHz max.	VDD: 4.0V to 6.0V IDD: 3.8 mA max. at 5.5V IPD: 21 μA max. at 4V Freq:4 MHz max.
HS	VDD: 4.5V to 5.5V IDD: 13.5 mA typ. at 5.5V IPD: 1.5 μA typ. at 4.5V Freq:4 MHz max.	VDD: 4.5V to 5.5V IDD: 15 mA max. at 5.5V IPD: 1.5 μA typ. at 4.5V Freq: 10 MHz max.	VDD: 4.5V to 5.5V IDD: 30 mA max. at 5.5V IPD: 1.5 μA typ. at 4.5V Freq: 20 MHz max.	Not recommended for use in HS mode	VDD: $4.5V$ to $5.5V$ IDD: 30 mA max. at $5.5V$ IPD: 1.5 μ A typ. at $4.5V$ Freq: 20 MHz max.
LP	VDD: 4.0V to 6.0V IDD: 52.5 μA typ. at 32 kHz, 4.0V IPD: 0.9 μA typ. at 4.0V Freq:200 kHz max.	Not recommended for use in LP mode	Not recommended for use in LP mode	VDD: 3.0V to 6.0V IDD: 48 μA max. at 32 kHz, 3.0V IPD: 13.5 μA max. at 3.0V Freq:200 kHz max.	VDD: 3.0V to 6.0V IDD: 48 μA max. at 32 kHz, 3.0V IPD:13.5 μA max. at 3.0V Freq:200 kHz max.

The shaded sections indicate oscillator selections which are tested for functionality, but not for MIN/MAX specifications. It is recommended that the user select the device type that ensures the specifications required.

Applicable Devices 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

PIC16C62/64-04 (Commercial, Industrial) DC Characteristics:

> PIC16C62/64-10 (Commercial, Industrial) PIC16C62/64-20 (Commercial, Industrial)

Standard Operating Conditions (unless otherwise stated) DC CHARACTERISTICS Operating temperature -40°C ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial Characteristic Min Max Units **Conditions Param** Sym Typ† No. D001 XT, RC and LP osc configuration Supply Voltage VDD 4.0 6.0 ٧ D001A HS osc configuration 4.5 5.5 V V D002* RAM Data Retention **VDR** 1.5 Voltage (Note 1) D003 VDD start voltage to **VPOR** V Vss See section on Power-on Reset for details ensure internal Poweron Reset signal D004* VDD rise rate to ensure SVDD 0.05 V/ms See section on Power-on Reset for details internal Power-on Reset signal D010 Supply Current XT, RC, osc configuration IDD 2.7 5.0 mΑ (Note 2, 5) FOSC = 4 MHz, VDD = 5.5V (Note 4) D013 13.5 30 mA HS osc configuration Fosc = 20 MHz. VDD = 5.5VD020 Power-down Current 10.5 42 μΑ VDD = 4.0V, WDT enabled, -40°C to +85°C μΑ D021 (Note 3, 5) 1.5 21 VDD = 4.0V. WDT disabled. $-0^{\circ}C$ to $+70^{\circ}C$ μΑ D021A 24 VDD = 4.0V, WDT disabled, -40°C to +85°C

- These parameters are characterized but not tested.
- Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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Note 1: This is the limit to which VDD can be lowered without losing RAM data.

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- The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
 - The test conditions for all IDD measurements in active operation mode are:
 - OSC1 = external square wave, from rail to rail; all I/O pins tristated, pulled to VDD
 - MCLR = VDD; WDT enabled/disabled as specified.
- 3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and Vss.
- 4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kOhm.
- Timer1 oscillator (when enabled) adds approximately 20 µA to the specification. This value is from characterization and is for design guidance only. This is not tested.

18.2 DC Characteristics: PIC16LC62/64-04 (Commercial, Industrial)

DC CHA	RACTERISTICS	Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq \text{TA} \leq +85^{\circ}\text{C}$ for industrial and $0^{\circ}\text{C} \leq \text{TA} \leq +70^{\circ}\text{C}$ for commercial								
Param No.	Characteristic	Sym	Min	Тур†	Max	Units	Conditions LP, XT, RC osc configuration (DC - 4 MHz)			
D001	Supply Voltage	VDD	3.0	V -	6.0	V				
D002*	RAM Data Retention Voltage (Note 1)	VDR	W.	1.5	-	V	W.100Y.COMITW			
D003	VDD start voltage to ensure internal Power- on Reset signal	VPOR	COM	Vss	-	V	See section on Power-on Reset for details			
D004*	VDD rise rate to ensure internal Power-on Reset signal	SVDD	0.05	YI.IV	-	V/ms	See section on Power-on Reset for details			
D010	Supply Current (Note 2, 5)	IDD	07 <u>-</u> C	2.0	3.8	mA	XT, RC osc configuration FOSC = 4 MHz, VDD = 3.0V (Note 4)			
D010A	OW.TW W	MM')	1001	22.5	48	μΑ	LP osc configuration Fosc = 32 kHz, VDD = 3.0V, WDT disabled			
D020 D021 D021A	Power-down Current (Note 3, 5)	IPD	(1.100° (01.10	7.5 0.9 0.9	30 13.5 18	μΑ μΑ μΑ	VDD = 3.0V, WDT enabled, -40°C to +85°C VDD = 3.0V, WDT disabled, 0°C to +70°C VDD = 3.0V, WDT disabled, -40°C to +85°C			

- * These parameters are characterized but not tested.
- † Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.
- Note 1: This is the limit to which VDD can be lowered without losing RAM data.
 - 2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
 - The test conditions for all IDD measurements in active operation mode are:
 - OSC1 = external square wave, from rail to rail; all I/O pins tristated, pulled to VDD MCLR = VDD; WDT enabled/disabled as specified.
 - 3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and Vss.
 - 4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kOhm.
 - 5: Timer1 oscillator (when enabled) adds approximately 20 μA to the specification. This value is from characterization and is for design guidance only. This is not tested.

DC CHARACTERISTICS

Applicable Devices 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

18.3 DC Characteristics: PIC16C62/64-04 (Commercial, Industrial)

PIC16C62/64-10 (Commercial, Industrial) PIC16C62/64-20 (Commercial, Industrial) PIC16LC62/64-04 (Commercial, Industrial)

Standard Operating Conditions (unless otherwise stated)

Operating temperature $-40^{\circ}\text{C} \le \text{TA} \le +85^{\circ}\text{C}$ for industrial and

 0° C $\leq TA \leq +70^{\circ}$ C for commercial

Operating voltage VDD range as described in DC spec Section 18.1

and Section 18.2

Param No.	Characteristic	Sym	Min	Typ †	Max	Units	Conditions
N.CO	Input Low Voltage I/O ports	VIL	CM.		WWW.	1001	CONSTA
D030	with TTL buffer	COM.	Vss	_	0.15VDD	V	For entire VDD range
D030A	OM.11/1 = 2010 /1 /100 /	COM	Vss	_	0.8V	V	4.5V ≤ VDD ≤ 5.5V
D031	with Schmitt Trigger buffer	Y.C.	Vss	-	0.2VDD	VO	DY.
D032	MCLR, OSC1 (in RC mode)	V.CO	Vss	-	0.2VDD	V	MY.COTTY
D033	OSC1 (in XT, HS and LP)	- CC	Vss	-	0.3VDD	V	Note1
-1100	Input High Voltage	003.			- 1	TXV	Too ON
	I/O ports	VIH	Or.	N		Mari	TOOY.CO. TY
D040	with TTL buffer	100	2.0	-3	VDD	V	4.5V ≤ VDD ≤ 5.5V
D040A	OY.CO TITTO	1007.	0.25VDD		VDD	V	For entire VDD range
	OOY.COME WWY	1005	+ 0.8V	TV		WW	WI.100Y.COM.TW
D041	with Schmitt Trigger buffer	100	0.8VDD	T	VDD	WV	For entire VDD range
D042	MCLR	MN.	0.8VDD	- 1	VDD	V	WW. OOX.CO. STW
D042A	OSC1 (XT, HS and LP)	W.W.	0.7VDD	M	VDD	V	Note1
D043	OSC1 (in RC mode)	1	0.9VDD	1.5	VDD	V	1007. COM.TI
D070	PORTB weak pull-up current	IPURB	50	200	400	μΑ	VDD = 5V, VPIN = VSS
D060	Input Leakage Current (Notes 2, 3) I/O ports	liL V	1.100Y.		±1 ^N	μА	Vss ≤ VPIN ≤ VDD, Pin at himpedance
D061	MCLR, RA4/T0CKI	N ·	$\sqrt{100}$		±5	μA	Vss ≤ VPIN ≤ VDD
D063	OSC1	WW	1.W.700	V.	±5	μΑ	Vss ≤ VPIN ≤ VDD, XT, HS and LP osc configuration
	Output Low Voltage		WW.10	- <1	COM.,		MAN TO ON CO
D080	I/O ports	Vol	WW.1	00.	0.6	V	IOL = 8.5 mA , VDD = 4.5V , -40°C to $+85^{\circ}\text{C}$
D083	OSC2/CLKOUT (RC osc config)		WWW	70 700	0.6	V	IOL = 1.6 mA, VDD = 4.5V, -40°C to +85°C
	Output High Voltage	si .		1.3	CO.	NI.	M MMM.
D090	I/O ports (Note 3)	Vон	VDD-0.7	(1. 1	00 Y.C.	V	IOH = -3.0 mA, VDD = 4.5V, -40°C to +85°C
D092	OSC2/CLKOUT (RC osc config)	TW	VDD-0.7	W	1100Y.C	OV	IOH = -1.3 mA, VDD = 4.5V, -40°C to +85°C
D150*	Open-Drain High Voltage	Vod	- 🕠	41	14	V	RA4 pin

^{*} These parameters are characterized but not tested.

- 2: The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.
- 3: Negative current is defined as current sourced by the pin.

[†] Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C6X be driven with external clock in RC mode.

Standard Operating Conditions (unless otherwise stated)
Operating temperature -40°C ≤ TA ≤ +85°C for industrial and
0°C ≤ TA ≤ +70°C for commercial
Operating voltage VDD range as described in DC spec Section 18.1
and Section 18.2

Param Characteristic Sym Min Typ Max Units Conditions

Param No.	Characteristic	Sym	Min	Typ †	Max	Units	Conditions
WT.IV	Capacitive Loading Specs on Output	t	W		100X.	COM	IN
D100	OSC2 pin	Cosc ₂	- 1	WW	15	pF	In XT, HS and LP modes when external clock is used to drive OSC1.
D101 D102	All I/O pins and OSC2 (in RC mode) SCL, SDA in I ² C mode	Cio Cb	-	41	50 400	pF pF	OM.TW

- * These parameters are characterized but not tested.
- † Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.
- Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C6X be driven with external clock in RC mode.
 - 2: The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.
 - 3: Negative current is defined as current sourced by the pin.

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Timing Parameter Symbology

The timing parameter symbols have been created following one of the following formats:

1. TppS2ppS	3. Tcc:st (I ² C specifications only)
2. TppS	4. Ts (I ² C specifications only)
T TW WWW. 100Y. CO. TW	WWW. TIOOX. COLITY
F Frequency	T Time

Lowercase letters (pp) and their meanings:

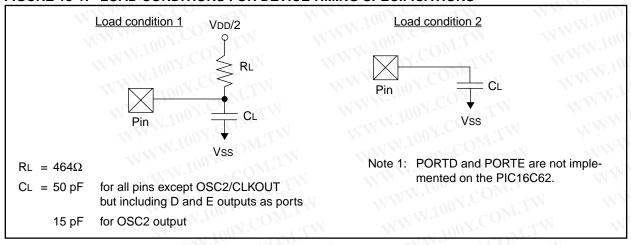
p			
CC	CCP1	osc	OSC1
ck	CLKOUT	rd	RD COM
cs	√ CS NY 100 ° COM	rw	RD or WR
di	SDI	sc	SCK
do	SDO	SS	SS
dt	Data in	tO	TOCKI COMMON TOCKI
io	I/O port	t1	T1CKI
mc	MCLR	wr	WR W

Uppercase letters and their meanings:

S. 100	COMIT	COM.	COM.
F 100	Fall	P	Period
H	High	R	Rise
M.10	Invalid (Hi-impedance)	COM.	Valid
L VI	Low	OU ZOM.	Hi-impedance
I ² C only		100 Y. COM	
AA	output access	High	High
BUF	Bus free	Low	Low

CC	100x. CM.TW	1700 7.	OWIT	WW.Inn COV
HD	Hold	SU	Setup	MM. 1007.0
ST		W.I		MMM. TOUN CO
DAT	DATA input hold	STO	STOP condition	TWW.In av Co
STA	START condition	100		11,100,100,100

FIGURE 18-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS



18.5 <u>Timing Diagrams and Specifications</u>

FIGURE 18-2: EXTERNAL CLOCK TIMING

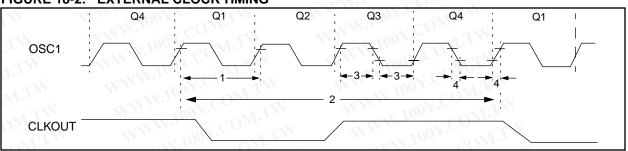


TABLE 18-2: EXTERNAL CLOCK TIMING REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Тур†	Max	Units	Conditions
COMP.	Fosc	External CLKIN Frequency	DC	N —	4	MHz	XT and RC osc mode
	7.7.	(Note 1)	DC		4	MHz	HS osc mode (-04)
	WT	WW. 1007.C	DC		10	MHz	HS osc mode (-10)
	T. T.	D.V.O	DC	T 4	20 <	MHz	HS osc mode (-20)
	$M_{i,I}$	W.100	DC	- 1 - T	200	kHz	LP osc mode
	TI	Oscillator Frequency	DC	V. II	4	MHz	RC osc mode
	Divi	(Note 1)	0.1	T/1	4	MHz	XT osc mode
	OM	WW.100	4	M.	20	MHz	HS osc mode
	- 11	IN 100	5	ON T	200	kHz	LP osc mode
1	Tosc	Oscillator Period (Note 1)	250	- 1	W-	ns	XT and RC osc mode
			250	$CO_{\overline{D}/V}$	_	ns	HS osc mode (-04)
			100	N n ,	7.7	ns	HS osc mode (-10)
			50	CA	CT Y	ns	HS osc mode (-20)
			5	4 (4 0]	-XX	μs	LP osc mode
			250	<u></u>	$M_{\overline{I}_{A}}$	ns	RC osc mode
			250	UX T C	10,000	ns	XT osc mode
	100 -		250	~ √ C	250	ns ns	HS osc mode (-04)
	1003	-OM.TW	100	$00\overline{\tau}$.	250	ns	HS osc mode (-10)
		V.CO. TW W	50	Ana Y.V	1,000	ns	HS osc mode (-20)
	N. Jac	- CONL.	5	.10 <u>-</u> 01	CG,	μs	LP osc mode
2	Tcy	Instruction Cycle Time (Note 1)	200	TCY	DC	ns	Tcy = 4/Fosc
3	TosL,	External Clock in (OSC1) High	100	700	V	ns	XT oscillator
	TosH	or Low Time	2.5	115	$\sim \in O_1$	μs	LP oscillator
	1	1001. ONT.I.A.	15		0 ×	ns	HS oscillator
4	TosR,	External Clock in (OSC1) Rise	4	11	25	ns	XT oscillator
	TosF	or Fall Time	-	$M_{\overline{A}N}$,	50	ns	LP oscillator
	Mar.	1001.	-1	-TAM	15	ns	HS oscillator

[†] Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (TCY) equals four times the input oscillator time-base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1/CLKIN pin. When an external clock input is used, the "Max." cycle time limit is "DC" (no clock) for all devices.

FIGURE 18-3: CLKOUT AND I/O TIMING

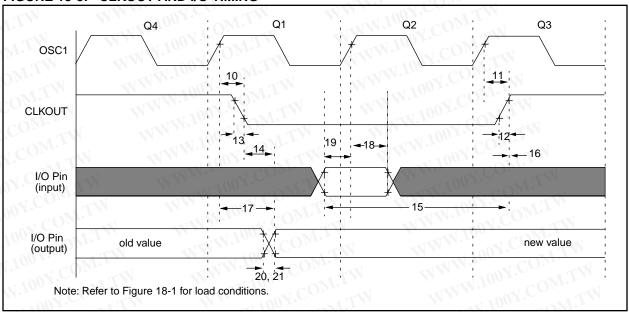


TABLE 18-3: CLKOUT AND I/O TIMING REQUIREMENTS

Parameters	Sym	Characteristic	1007.	Min	Typ†	Max	Units	Conditions
10*	TosH2ckL	OSC1↑ to CLKOUT↓	TYL	75	200	ns	Note 1	
11*	TosH2ckH	OSC1↑ to CLKOUT↑	THE STATE OF THE S	75	200	ns	Note 1	
12*	TckR	CLKOUT rise time	DAY. TO	35	100	ns	Note 1	
13*	TckF	CLKOUT fall time	OM-	35	100	ns	Note 1	
14*	TckL2ioV	CLKOUT ↓ to Port out valid	CONTIN	_	0.5Tcy + 20	ns	Note 1	
15*	TioV2ckH	Port in valid before CLKOUT	Port in valid before CLKOUT ↑			7//	ns	Note 1
16*	TckH2ioI	Port in hold after CLKOUT ↑		0		-4/1/	ns	Note 1
17*	TosH2ioV	OSC1↑ (Q1 cycle) to Port out	V.COm	50	150	ns	100 Y.C.	
18*	TosH2ioI		PIC16 C 62/64	100	N.	- 4	ns	· OUT.C
	WW.10	input invalid (I/O in hold time)	PIC16 LC 62/64	200	_ X	ı —	ns	V.In.
19*	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)	WWW.	OOY.CO	M.2 M.3	N -	ns	W.100
20*	TioR	Port output rise time	PIC16 C 62/64	· AT.C	10	40	ns	V /4.
	TAN V	TOWN COM.	PIC16 LC 62/64	1.10 - C	$O_{Z_{I'}}$	80	ns	MW.I
21*	TioF	Port output fall time	PIC16 C 62/64	W.100	10	40	ns	MW.I
	11/11	W.100Y.COM.TW	PIC16 LC 62/64	W. 100 Y		80	ns	W.
22††*	Tinp	INT pin high or low time	INT pin high or low time			M.T.W	ns	W TO THE
23††*	Trbp	RB7:RB4 change INT high or	low time	Tcy	V.C.		ns	MAL

^{*} These parameters are characterized but not tested.

Note 1: Measurements are taken in RC Mode where CLKOUT output is 4 x Tosc.

[†] Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

^{††} These parameters are asynchronous events not related to any internal clock edge.

FIGURE 18-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING

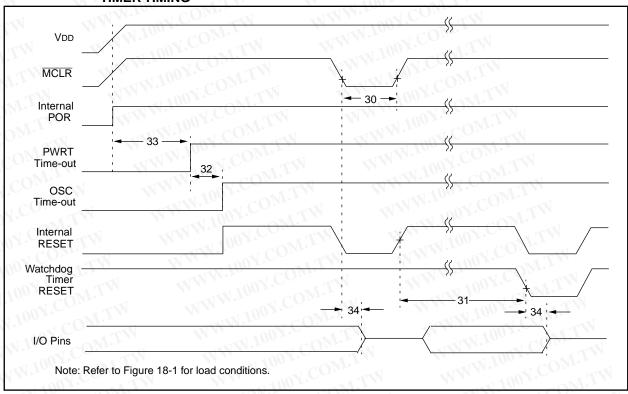


TABLE 18-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
30*	TmcL	MCLR Pulse Width (low)	100	N.7	W	ns	VDD = 5V, -40°C to +85°C
31*	Twdt	Watchdog Timer Time-out Period (No Prescaler)	N.700	18	33	ms	$VDD = 5V, -40^{\circ}C \text{ to } +85^{\circ}C$
32	Tost	Oscillation Start-up Timer Period	V+10	1024Tosc		_	Tosc = OSC1 period
33*	Tpwrt	Power-up Timer Period	28	72	132	ms	$VDD = 5V, -40^{\circ}C \text{ to } +85^{\circ}C$
34*	Tioz	I/O Hi-impedance from MCLR Low	- 7 X	1007.	100	ns	A. 1003.

^{*} These parameters are characterized but not tested.

[†] Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Applicable Devices 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

FIGURE 18-5: TIMERO AND TIMER1 EXTERNAL CLOCK TIMINGS

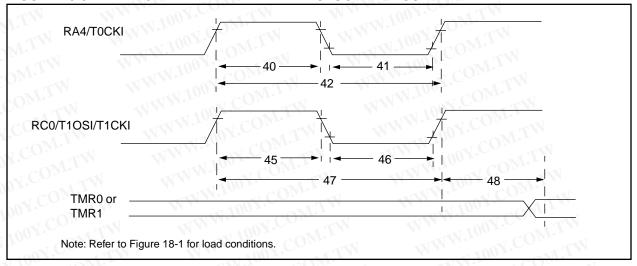


TABLE 18-5: TIMERO AND TIMER1 EXTERNAL CLOCK REQUIREMENTS

Param No.	Sym	Characteristic	WW.1	OOY.COM	Min	Typ†	Max	Units	Conditions	
40*	Tt0H	T0CKI High Pulse V	Vidth	No Prescaler	0.5Tcy + 20	W.	aπ1	ns	Must also meet	
	~ CC) Nr.	TW WWW.		10	- IV	1.4.	ns	parameter 42	
41*	Tt0L	T0CKI Low Pulse W	/idth	No Prescaler	0.5Tcy + 20		(A)	ns	Must also meet	
	LOOY.C			With Prescaler	10	7	*	ns	parameter 42	
42*	Tt0P	T0CKI Period	TATAN	No Prescaler	Tcy + 40	_		ns	W.Con	
	N.1007	COM.TW		With Prescaler	Greater of: 20 or <u>TcY + 40</u> N	+ 40		ns	N = prescale value (2, 4,, 256)	
45*	Tt1H	T1CKI High Time	Synchronous, F	Prescaler = 1	0.5Tcy + 20	† —	4	ns	Must also meet	
	W.100	COMIT	Synchronous,	PIC16 C 6X	15	T —	_	ns	parameter 47	
	N 10	OY.COM.TV	Prescaler = 2,4,8	PIC16LC6X	25	_		ns	1.100 1. CO	
			Asynchronous	PIC16 C 6X	30	_	_ `	ns	W 100 1.	
		COM	OVN	PIC16LC6X	50	W-	_	ns	M. Co	
46*	Tt1L	T1CKI Low Time	Synchronous, F	Prescaler = 1	0.5Tcy + 20	-7	_	ns	Must also meet	
	WWW	. OUX.CO.	Synchronous, PIC16 C 6X		15	114	_	ns	parameter 47	
	WW	V.100X.CON	Prescaler = 2,4,8	PIC16 LC 6X	25	W	_	ns	WW.100Y.	
		W.100	Asynchronous	PIC16 C 6X	30	_	_	ns	WWW.	
	4/1/1	1007.	TIM	PIC16LC6X	50	(<u>+</u>	_	ns	100	
47*	Tt1P	T1CKI input period	Synchronous	PIC16 C 6X	Greater of: 30 OR TCY + 40 N	M.T		ns	N = prescale value (1, 2, 4, 8)	
		MM.100X	COM.TV	PIC16LC6X	Greater of: 50 OR TCY + 40 N	O_{M}	TW	LT.	N = prescale value (1, 2, 4, 8)	
		WW TOO	Asynchronous	PIC16C6X	60		(#)	ns	Al I	
		I IN W. IO	COMP.	PIC16LC6X	100	Cr.	_	ns	AN WAY	
	Ft1	Timer1 oscillator inp (oscillator enabled by			DC	1. <u>C</u> C	200	kHz	WW	
48	TCKEZtmr	1 Delay from external	clock edge to tir	mer increment	2Tosc	T	7Tosc	_	-1	

^{*} These parameters are characterized but not tested.

[†] Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 18-6: CAPTURE/COMPARE/PWM TIMINGS (CCP1)

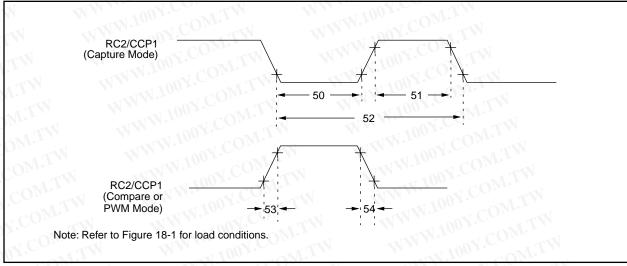


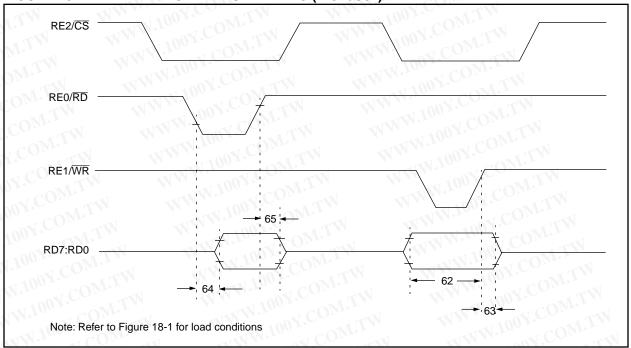
TABLE 18-6: CAPTURE/COMPARE/PWM REQUIREMENTS (CCP1)

Parameter No.	Sym	Characteristic	WW.1001.	M.M.1001.COW.IA		Тур†	Max	Units	Conditions
50*	TccL		No Prescaler		0.5Tcy + 20		-	ns	OMITW
	COI	input low time	With Prescaler	PIC16 C 62/64	10		$d\overline{V}_{L}$	ns	COMP
	- CC	W.L.	WW.10	PIC16 LC 62/64	20	-31 1	W.	ns	COM
51*	TccH	1 1 2 2	No Prescaler	OM	0.5Tcy + 20	_	WAN	ns	A COMP.
	21.0	input high time	With Prescaler	PIC16 C 62/64	10		TAN Y	ns	*I COM:
	00 X.	TOM:TW	MM	PIC16 LC 62/64	20	_	N T	ns	ON.
52*	TccP	CCP1 input period	MM	W.100Y.C	3Tcy + 40 N	_		ns	N = prescale value (1,4 or 16)
53	TccR	CCP1 output rise ti	me	PIC16 C 62/64	OM-	10	25	ns	· LOW COM
	W.10	Dr. COM.TV		PIC16 LC 62/64	$co_{\overline{M}_{-1}}$	25	45	ns	N. Ing COL
54	TccF	CCP1 output fall tin	ne	PIC16 C 62/64	COMITY	10	25	ns	W.100
	N N	1007.COM.		PIC16 LC 62/64	TMT	25	45	ns	VW.1003

^{*} These parameters are characterized but not tested.

[†] Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 18-7: PARALLEL SLAVE PORT TIMING (PIC16C64)



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TABLE 18-7: PARALLEL SLAVE PORT REQUIREMENTS (PIC16C64)

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions	
62	TdtV2wrH	Data in valid before WR↑ or CS	5↑ (setup time)	20	_ `	N -	ns	. M.
63*	TwrH2dtl	WR↑ or CS↑ to data–in invalid	PIC16 C 64	20	_	ATA.	ns	N.C.
	CO	(hold time)	PIC16 LC 64	35	_	4	ns	MY.CO
64	TrdL2dtV	RD↓ and CS↓ to data–out valid	TO COL	1	1 -	80	ns	CO
65	TrdH2dtl	RD↑ or CS↑ to data–out invalid	N.1003	10		30	ns	100 -

^{*} These parameters are characterized but not tested.

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[†] Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 18-8: SPI MODE TIMING

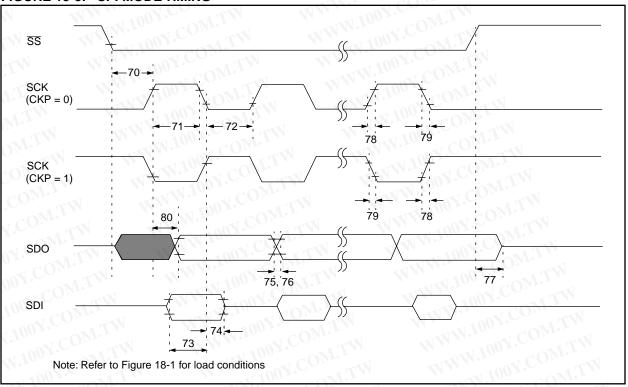
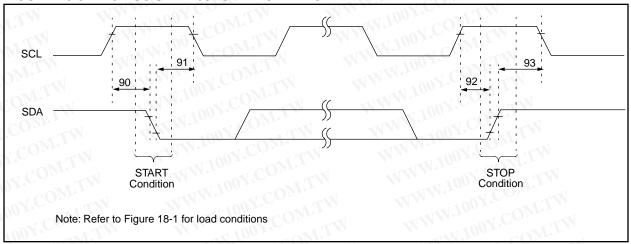


TABLE 18-8: SPI MODE REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Тур†	Max	Units	Conditions
70	TssL2scH, TssL2scL	Tcy	_	MM	ns	M.COM.	
71	TscH	SCK input high time (slave mode)	Tcy + 20	N —	_N	ns	OY.Co
72	TscL	SCK input low time (slave mode)	Tcy + 20	cas i		ns	WY.COM
73	TdiV2scH, TdiV2scL	Setup time of SDI data input to SCK edge	50	TW	_	ns	100X.CO
74	TscH2diL, TscL2diL	Hold time of SDI data input to SCK edge	50	T.TN	_	ns	N.100Y.C
75	TdoR	SDO data output rise time	100 7	10	25	ns	W.1001.
76	TdoF	SDO data output fall time	100×1.00	10	25	ns	11001
77	TssH2doZ	SS↑ to SDO output hi-impedance	10	$O^{\overline{M_{P_{i}}}}$	50	ns	NW 002
78	TscR	SCK output rise time (master mode)	N.100	10	25	ns	MAIN
79	TscF	SCK output fall time (master mode)	W. 100 r.	10	25	ns	WW.100
80 TscH2doV, SDO data output valid after SCK edge			M.1007		50	ns	WWW.10

[†] Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 18-9: 12C BUS START/STOP BITS TIMING



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TABLE 18-9: I²C BUS START/STOP BITS REQUIREMENTS

Parameter No.	Sym	Characteristic	M.100 F.CO.	Min	Тур	Max	Units	Conditions		
90	Tsu:sta	START condition	100 kHz mode	4700		_		Only relevant for repeated START		
	Mon	Setup time	400 kHz mode	600		_	ns	condition		
91	THD:STA	START condition	100 kHz mode	4000	Z.V	_		After this period the first clock		
	V.COM	Hold time	400 kHz mode	600	T	l —	ns	pulse is generated		
92	Tsu:sto	STOP condition	100 kHz mode	4700		OV-		WWW. CON. CO.		
	001.	Setup time	400 kHz mode	600	Mr.	- XI	ns	COM.		
93	THD:STO	STOP condition	100 kHz mode	4000	A	1.4		1, 100 COW		
	ON.C	Hold time	400 kHz mode	600		47/	ns	11001.		

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FIGURE 18-10: I²C BUS DATA TIMING

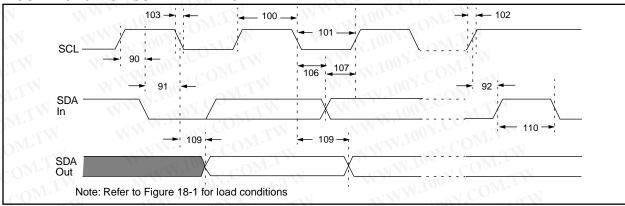


TABLE 18-10: I²C BUS DATA REQUIREMENTS

Parameter No.	Sym	Characteristic	OX.COM.TY	Min	Max	Units	Conditions
100	THIGH	Clock high time	100 kHz mode	4.0		μs	Device must operate at a minimum of 1.5 MHz
1001.C		N WWW	400 kHz mode	0.6	11/	μѕ	Device must operate at a minimum of 10 MHz
1.100 1.			SSP Module	1.5TcY		WW.	COM
101	TLOW	Clock low time	100 kHz mode	4.7	-1	μs	Device must operate at a minimum of 1.5 MHz
VV.1003		TAN MA	400 kHz mode	1.3	_	μs	Device must operate at a minimum of 10 MHz
M.IUV			SSP Module	1.5Tcy	_	TAI VI	M. COP
102	TR	SDA and SCL rise	100 kHz mode	ONE	1000	ns	M.100.
NAM.		time	400 kHz mode	20 + 0.1Cb	300	ns	Cb is specified to be from 10 to 400 pF
103	10 TE	SDA and SCL fall time	100 kHz mode	T. John T.	300	ns	131.100 COM. 1
MMM		ON.TW	400 kHz mode	20 + 0.1Cb	300	ns	Cb is specified to be from 10 to 400 pF
90	Tsu:sta	START condition	100 kHz mode	4.7	17	μs	Only relevant for repeated
		setup time	400 kHz mode	0.6	- 	μs	START condition
91	THD:STA	START condition hold	100 kHz mode	4.0	17-5	μs	After this period the first clock
W		time	400 kHz mode	0.6		μs	pulse is generated
106	THD:DAT	Data input hold time	100 kHz mode	0	- T	ns	MM. 100X.CC
		dor. COWII	400 kHz mode	0.100	0.9	μs	TWW.Io
107	TSU:DAT	Data input setup time	100 kHz mode	250	No.	ns	Note 2
		. CON COM	400 kHz mode	100		ns	WW 100X.
92	Tsu:sto	STOP condition setup	100 kHz mode	4.7	CON	μs	WWW.E
		time	400 kHz mode	0.6		μs	W 100 x
109	TAA	Output valid from	100 kHz mode	1111-10	3500	ns	Note 1
		clock	400 kHz mode	A in	- ₹ C.	ns	WWW.E
110	TBUF	Bus free time	100 kHz mode	4.7	07.	μs	Time the bus must be free
		WW. 100Y.COP	400 kHz mode	1.3	002.	μs	before a new transmission can start
	Cb	Bus capacitive loading		M. T.	400	pF	IN W

Note 1: As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (min. 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

2: A fast-mode (400 kHz) I²C-bus device can be used in a standard-mode (100 kHz) I²C-bus system, but the requirement tsu;DAT ≥ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line TR max. + tsu;DAT = 1000 + 250 = 1250 ns (according to the standard-mode I²C bus specification) before the SCL line is released.

Applicable Devices 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67 WWW.100Y.COM.TW WWW.100Y WWW.1007 WWW.100Y.COM.T NOTES: W.100Y.COM.TW

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19.0 ELECTRICAL CHARACTERISTICS FOR PIC16C62A/R62/64A/R64

Absolute Maximum Ratings †

Ambient temperature under bias	55°C to +125°C
Storage temperature	65°C to +150°C
Voltage on any pin with respect to Vss (except VDD, MCLR, and RA4)	
Voltage on VDD with respect to Vss	0.3V to +7.5V
Voltage on MCLR with respect to Vss (Note 2)	0V to +14V
Voltage on RA4 with respect to Vss	
Total power dissipation (Note 1)	1.0W
Maximum current out of Vss pin	300 mA
Maximum current into VDD pin	250 mA
Input clamp current, lik (VI < 0 or VI > VDD)	±20 mA
Output clamp current, lox (Vo < 0 or Vo > VDD)	
Maximum output current sunk by any I/O pin	25 mA
Maximum output current sourced by any I/O pin	25 mA
Maximum current sunk by PORTA, PORTB, and PORTE (combined)	200 mA
Maximum current sourced by PORTA, PORTB, and PORTE (combined)	200 mA
Maximum current sunk by PORTC and PORTD (combined)	
Maximum current sourced by PORTC and PORTD (combined)	

Note 1: Power dissipation is calculated as follows: Pdis = VDD x {IDD - Σ IOH} + Σ {(VDD-VOH) x IOH} + Σ (Vol x IOL)

Note 2: Voltage spikes below Vss at the MCLR pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a "low" level to the MCLR pin rather than pulling this pin directly to Vss.

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 19-1: CROSS REFERENCE OF DEVICE SPECS FOR OSCILLATOR CONFIGURATIONS AND FREQUENCIES OF OPERATION (COMMERCIAL DEVICES)

osc	PIC16C62A-04 PIC16CR62-04 PIC16C64A-04 PIC16CR64-04	PIC16C62A-10 PIC16CR62-10 PIC16C64A-10 PIC16CR64-10	PIC16C62A-20 PIC16CR62-20 PIC16C64A-20 PIC16CR64-20	PIC16LC62A-04 PIC16LCR62-04 PIC16LC64A-04 PIC16LCR64-04	JW Devices
RC	VDD: 4.0V to 6.0V IDD: 5 mA max. at 5.5V IPD: 16 μA max. at 4V Freq:4 MHz max.	VDD: 4.5V to 5.5V IDD: 2.0 mA typ. at 5.5V IPD: 1.5 μA typ. at 4V Freq: 4 MHz max.	VDD: 4.5V to 5.5V IDD: 2.0 mA typ. at 5.5V IPD: 1.5 μA typ. at 4V Freq: 4 MHz max.	VDD: 2.5V to 6.0V IDD: 3.8 mA max. at 3.0V IPD: 5 μA max. at 3V Freq: 4 MHz max.	VDD: 4.0V to 6.0V IDD: 5 mA max. at 5.5V IPD: 16 μA max. at 4V Freq:4 MHz max.
XT	VDD: 4.0V to 6.0V IDD: 5 mA max. at 5.5V IPD: 16 µA max. at 4V Freq: 4 MHz max.	VDD: 4.5V to 5.5V IDD: 2.0 mA typ. at 5.5V IPD: 1.5 μA typ. at 4V Freq: 4 MHz max.	VDD: 4.5V to 5.5V IDD: 2.0 mA typ. at 5.5V IPD: 1.5 μA typ. at 4V Freq: 4 MHz max.	VDD: 2.5V to 6.0V IDD: 3.8 mA max. at 3.0V IPD: 5 µA max. at 3.0V Freq: 4 MHz max.	VDD: 4.0V to 6.0V IDD: 5 mA max. at 5.5V IPD: 16 µA max. at 4V Freq: 4 MHz max.
HS	VDD: 4.5V to 5.5V IDD: 13.5 mA typ. at 5.5V IPD: 1.5 μA typ. at 4.5V Freq: 4 MHz max.	-1 CON -1	VDD: 4.5V to 5.5V IDD: 20 mA max. at 5.5V IPD: 1.5 μA typ. at 4.5V Freq: 20 MHz max.	Not recommended for use in HS mode	VDD: 4.5V to 5.5V IDD: 20 mA max. at 5.5V IPD: 1.5 μA typ. at 4.5V Freq: 20 MHz max.
LP	VDD: 4.0V to 6.0V IDD: 52.5 μA typ. at 32 kHz, 4.0V IPD: 0.9 μA typ. at 4.0V Freq: 200 kHz max.	Not recommended for use in LP mode	Not recommended for use in LP mode	VDD: 2.5V to 6.0V IDD: 48 μA max. at 32 kHz, 3.0V IPD: 5 μA max. at 3.0V Freq: 200 kHz max.	VDD: 2.5V to 6.0V IDD: 48 μA max. at 32 kHz, 3.0V IPD: 5 μA max. at 3.0V Freq: 200 kHz max.

The shaded sections indicate oscillator selections which are tested for functionality, but not for MIN/MAX specifications. It is recommended that the user select the device type that ensures the specifications required.

19.1 DC Characteristics: PIC16C62A/R62/64A/R64-04 (Commercial, Industrial, Extended)

PIC16C62A/R62/64A/R64-10 (Commercial, Industrial, Extended)

PIC16C62A/R62/64A/R64-20 (Commercial, Industrial, Extended)

Standard Operating Conditions (unless otherwise stated)

DC CHARACTERISTICS

Operating temperature $-40^{\circ}\text{C} \leq \text{TA} \leq +125^{\circ}\text{C}$ for extended,

-40°C \leq TA \leq +85°C for industrial and

					0°(≤ TA ≤ +63 C for industrial and ≤ TA ≤ +70°C for commercial
Param No.	Characteristic	Sym	Min	Тур†	Max	Units	Conditions
D001 D001A	Supply Voltage	VDD	4.0 4.5	1.1.	6.0 5.5	V	XT, RC and LP osc configuration HS osc configuration
D002*	RAM Data Retention Voltage (Note 1)	VDR	y.EO	1.5	W.	V	WWW.100Y.COM.TW
D003	VDD start voltage to ensure internal Power-on Reset signal	VPOR	001.C	Vss	TW TW	V	See section on Power-on Reset for details
D004*	VDD rise rate to ensure internal Power-on Reset signal	SVDD	0.05	1.CO	M.T	V/ms	See section on Power-on Reset for details
D005	Brown-out Reset Voltage	BVDD	3.7 3.7	4.0 4.0	4.3 4.4	V	BODEN bit in configuration word enabled Extended Range Only
D010 D013	Supply Current (Note 2, 5)	IDD	NAN	2.7	5 20	mA mA	XT, RC, osc configuration Fosc = 4 MHz, VDD = 5.5V (Note 4) HS osc configuration Fosc = 20 MHz, VDD = 5.5V
D015*	Brown-out Reset Current (Note 6)	Δ IBOR	W-W	350	425	μА	BOR enabled, VDD = 5.0V
D020 D021 D021A D021B	Power-down Current (Note 3, 5)	IPD N	- 4N	10.5 1.5 1.5 2.5	42 16 19 19	μΑ μΑ μΑ μΑ	VDD = 4.0V, WDT enabled, -40°C to +85°C VDD = 4.0V, WDT disabled, -0°C to +70°C VDD = 4.0V, WDT disabled, -40°C to +85°C VDD = 4.0V, WDT disabled, -40°C to +125°C
D023*	Brown-out Reset Current (Note 6)	Δ IBOR	-	350	425	μА	BOR enabled, VDD = 5.0V

- * These parameters are characterized but not tested.
- † Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.
- Note 1: This is the limit to which VDD can be lowered without losing RAM data.
 - 2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.

The test conditions for all IDD measurements in active operation mode are:

OSC1 = external square wave, from rail to rail; all I/O pins tristated, pulled to VDD

MCLR = VDD; WDT enabled/disabled as specified.

- 3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and Vss.
- 4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kOhm.
- 5: Timer1 oscillator (when enabled) adds approximately 20 μA to the specification. This value is from characterization and is for design guidance only. This is not tested.
- 6: The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

19.2 DC Characteristics: PIC16LC62A/R62/64A/R64-04 (Commercial, Industrial)

DC CHA	RACTERISTICS	Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq \text{TA} \leq +85^{\circ}\text{C}$ for industrial and $0^{\circ}\text{C} \leq \text{TA} \leq +70^{\circ}\text{C}$ for commercial										
Param No.	Characteristic	Sym	Min	Тур†	Max	Units	Conditions					
D001	Supply Voltage	VDD	2.5	-	6.0	V	LP, XT, RC osc configuration (DC - 4 MHz)					
D002*	RAM Data Retention Voltage (Note 1)	VDR	T.IV	1.5	-41	V	100Y.COM.TW					
D003	VDD start voltage to ensure internal Power-on Reset signal	VPOR	M-T OM.	Vss	-	V	See section on Power-on Reset for details					
D004*	VDD rise rate to ensure internal Power-on Reset signal	SVDD	0.05	T.TW	-	V/ms	See section on Power-on Reset for details					
D005	Brown-out Reset Voltage	BVDD	3.7	4.0	4.3	٧	BODEN bit in configuration word enabled					
D010	Supply Current (Note 2, 5)	IDD	y.CO	2.0	3.8	mA	XT, RC osc configuration FOSC = 4 MHz, VDD = 3.0V (Note 4)					
D010A	COM.TW W	NW.1	007.	22.5	48	μΑ	LP osc configuration Fosc = 32 kHz, VDD = 3.0V, WDT disabled					
D015*	Brown-out Reset Current (Note 6)	Δlbor	1 100. 1 1 1 0 0 1	350	425	μА	BOR enabled, VDD = 5.0V					
D020	Power-down Current	IPD		7.5	30	μΑ	VDD = 3.0V, WDT enabled, -40°C to +85°C					
D021	(Note 3, 5)	-TXX	M-In	0.9	5	μΑ	VDD = 3.0V, WDT disabled, 0°C to +70°C					
D021A	DOY. COM.TW	N. V.	W.1	0.9	5	μΑ	VDD = 3.0V, WDT disabled, -40°C to +85°C					
D023*	Brown-out Reset Current (Note 6)	Δlbor	WW.	350	425	μА	BOR enabled, VDD = 5.0V					

- * These parameters are characterized but not tested.
- † Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.
- Note 1: This is the limit to which VDD can be lowered without losing RAM data.
 - 2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
 - The test conditions for all IDD measurements in active operation mode are:
 - OSC1 = external square wave, from rail to rail; all I/O pins tristated, pulled to VDD
 - MCLR = VDD; WDT enabled/disabled as specified.
 - 3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and Vss.
 - 4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kOhm.
 - 5: Timer1 oscillator (when enabled) adds approximately 20 μA to the specification. This value is from characterization and is for design guidance only. This is not tested.
 - 6: The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

DC CHARACTERISTICS

Applicable Devices 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

19.3 DC Characteristics: PIC16C62A/R62/64A/R64-04 (Commercial, Industrial, Extended)

PIC16C62A/R62/64A/R64-10 (Commercial, Industrial, Extended)

PIC16C62A/R62/64A/R64-20 (Commercial, Industrial, Extended)

PIC16LC62A/R62/64A/R64-04 (Commercial, Industrial)

Standard Operating Conditions (unless otherwise stated)

Operating temperature $-40^{\circ}\text{C} \le \text{TA} \le +125^{\circ}\text{C}$ for extended,

-40°C \leq TA \leq +85°C for industrial and 0°C \leq TA \leq +70°C for commercial

Operating voltage VDD range as described in DC spec Section 19.1 and

Section 19.2

Param	Characteristic	Section	Min	Tim	Max	Units	Conditions
No.	Characteristic	Sym	7 IVIII	Typ †	IVIAX	Units	Conditions
	Input Low Voltage	1 CO	1.			111.7	COM.
	I/O ports	VIL	WIN			-TXN	1001. CM.I.A.
D030	with TTL buffer	V.C.	Vss	-	0.15VDD	V	For entire VDD range
D030A	COM: 1	-7 C	Vss	- -	V8.0	V	$4.5V \le VDD \le 5.5V$
D031	with Schmitt Trigger buffer	001.	Vss	N	0.2VDD	V	N.100 1. COM: 1
D032	MCLR, OSC1 (in RC mode)	. NO.	Vss	-	0.2Vdd	V	1001.001
D033	OSC1 (in XT, HS and LP)	Inc	Vss	-	0.3VDD	V	Note1
	Input High Voltage	0.700_{2}	Mod	T		N.	M.100 F. COW.I
	I/O ports	VIH	Y.Co	CTC		W	W. 100Y.Com.TW
D040	with TTL buffer	M.In.	2.0	17-5	Vdd	V	$4.5V \le VDD \le 5.5V$
D040A	1001. OM.TW	TXV 10	0.25VDD	M.	VDD	V	For entire VDD range
	100Y.COTTY W	1	+ 0.8V				WW. TIOOY.
D041	with Schmitt Trigger buffer	MM.	0.8VDD	O_{M}	VDD	V	For entire VDD range
D041	MCLR	WW	0.8VDD	10.	VDD	V	Tor chare VBB range
D042A	OSC1 (XT, HS and LP)	1	0.7VDD	C	VDD	V	Note1
D043	OSC1 (in RC mode)	WW	0.9VDD	.C	VDD	V	T. Mariantina
D070	PORTB weak pull-up current	IPURB	50	250	400	μΑ	VDD = 5V, VPIN = VSS
- 14	Input Leakage Current (Notes 2, 3)		111.100	- 7	COMP.	- 1	TANN TON COMP
D060	I/O ports	IIL	T 10	07.	±1	μΑ	Vss ≤ VPIN ≤ VDD, Pin at hi-imped
	NWW.ICON.COM. TW	11	M.W.	003		TW	ance
D061	MCLR, RA4/T0CKI		WW.	05	±5	μΑ	Vss ≤ Vpin ≤ Vdd
D063	OSC1		W * '-	190	±5	μΑ	Vss ≤ VPIN ≤ VDD, XT, HS and LP
	Output Low Voltage		WWW	110	07.00	MIT	osc configuration
D080	I/O ports	VOL	WW	1.2	0.6	V	IOL = 8.5 mA, VDD = 4.5V,
D000	I/O ports	VOL	- XX	vi.1	0.6	O.V.	-40°C to +85°C
D080A	WW 100Y.Com.TI	N	1/1/1/	-1	0.6	V	IOL = 7.0 mA, VDD = 4.5 V,
2000, (MAM. TOW. COM.	W	W		. 100Y	COL	-40°C to +125°C
D083	OSC2/CLKOUT (RC osc config)	XXI		vi-	0.6	(V)	IOL = 1.6 mA, VDD = 4.5V,
	M 1, 21 100 X. COM	1.11	111				-40°C to +85°C
D083A	MMM. OOX.CO.	TW	- <	1/2/	0.6	V	IOL = 1.2 mA, VDD = 4.5V,
	TANNING TON	1. F		- 11	MM.To	V C	-40°C to +125°C

^{*} These parameters are characterized but not tested.

- 2: The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.
- 3: Negative current is defined as current sourced by the pin.

[†] Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C6X be driven with external clock in RC mode.

Standard Operating Conditions (unless otherwise stated)

Operating temperature $-40^{\circ}\text{C} \le \text{TA} \le +125^{\circ}\text{C}$ for extended,

-40°C ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial

Operating voltage VDD range as described in DC spec Section 19.1 and

Section 19.2

Param No.	Characteristic	Sym	Min	Typ †	Max	Units	Conditions
M	Output High Voltage	- 1		- 111	111.50	of C	
D090	I/O ports (Note 3)	Vон	VDD-0.7	11	WW.1	V	IOH = -3.0 mA, VDD = 4.5 V, -40 °C to $+85$ °C
D090A	TW WWW.100Y.CC	M.T	VDD-0.7	-	W-W.	V	IOH = -2.5 mA, VDD = 4.5 V, -40 °C to $+125$ °C
D092	OSC2/CLKOUT (RC osc config)	OM.	VDD-0.7	-	N IN	V.1V0	IOH = -1.3 mA, VDD = 4.5 V, -40 °C to $+85$ °C
D092A	W.TW WWW.100X.	COM	VDD-0.7	-	W.	VO.	IOH = -1.0 mA, VDD = 4.5 V, -40 °C to $+125$ °C
D150*	Open-Drain High Voltage	Vod	1	-	14	V	RA4 pin
007.0	Capacitive Loading Specs on Output Pins	V.CC	MITW		11	WW.	TOO TOOM TW
D100	OSC2 pin	Cosc ₂	$co_{W,T}$	VI VV	15	pF	In XT, HS and LP modes when external clock is used to drive OSC1.
D101	All I/O pins and OSC2 (in RC mode)	Cio	COM.	1.7	50	pF	W.100 COM.1
D102	SCL, SDA in I ² C mode	Cb	1.00	F	400	pF	100Y OM.TW

^{*} These parameters are characterized but not tested.

DC CHARACTERISTICS

- Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C6X be driven with external clock in RC mode.
 - 2: The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.
 - 3: Negative current is defined as current sourced by the pin.

[†] Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Timing Parameter Symbology

The timing parameter symbols have been created following one of the following formats:

1. TppS2ppS	3. Tcc:st (I ² C specifications	only)
2. TppS	4. Ts (I ² C specifications	only)

T	MM	100 Y.CO	TW	MA	1100Y.	MIIN	
CF	Frequency			T	Time		

Lowercase letters (pp) and their meanings:

pp	M. 100x. C.W.IM		W.1001.
cc	CCP1	osc	OSC1
ck	CLKOUT	√ rd	RD
cs	CS	rw	RD or WR
di	SDI	sc	SCK
do CO	SDO	SS	SS
dt	Data in	t0	TOCKI COMPANY
io	I/O port	t1	T1CKI
mc	MCLR	wr	WR

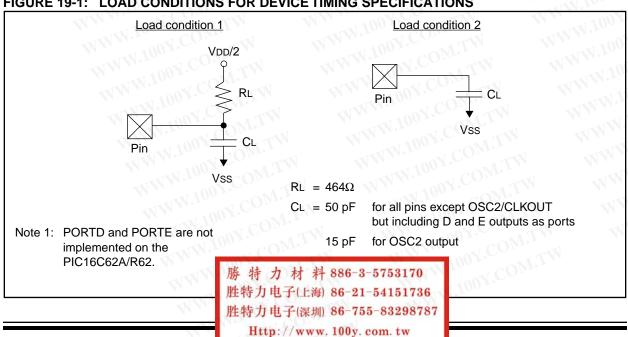
Uppercase letters and their meanings:

S		$O_{M^{*}}$	COM.
F 100	Fall	P	Period
H	High	R	Rise
WW.10	Invalid (Hi-impedance)	(A)	Valid
L 71/10	Low	ZOM	Hi-impedance Control
I ² C only		Moon	IN M. 1001. COWIT.
AA	output access	High	High
BUF	Bus free	Low	Low

Tcc:st (I²C specifications only)

CC	31 100x. CM.TW	100 .	ON: I COL
HD	Hold	SU	Setup
ST		V. I	
DAT	DATA input hold	STO	STOP condition
STA	START condition	100	

FIGURE 19-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS



19.5 <u>Timing Diagrams and Specifications</u>

FIGURE 19-2: EXTERNAL CLOCK TIMING

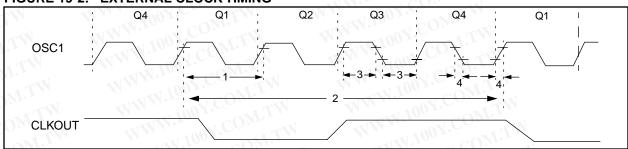


TABLE 19-2: EXTERNAL CLOCK TIMING REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Тур†	Max	Units	Conditions
1 CONT.	Fosc	External CLKIN Frequency	-XXI		TINY	- 0	V.CO
Mo.		(Note 1)	DC	_	4	MHz	XT and RC osc mode
M.Con.		MAN TOOK CO.	DC	_	4	MHz	HS osc mode (-04)
-1 CON		CO,	DC	_N –	10	MHz	HS osc mode (-10)
001.		W. 1001.	DC	_	20	MHz	HS osc mode (-20)
. and CU		MAN TOOK C	DC	W-	200	kHz	LP osc mode
100 - 1 C		Oscillator Frequency	DC	- N	4	MHz	RC osc mode
1007.		(Note 1)	0.1	7.7.	4	MHz	XT osc mode
.V.o		TW WY TOOK	4	(A)	20	MHz	HS osc mode
		TWW.Io	5	- X	200	kHz	LP osc mode
1,007	Tosc	External CLKIN Period	250	WT.	_	ns	XT and RC osc mode
N.N. 100		(Note 1)	250	11	N _	ns	HS osc mode (-04)
		N1.1	100	$0\bar{M}_{I}$.	-XI —	ns	HS osc mode (-10)
		M.TW WY	50	1.1 /4 0.	_	ns	HS osc mode (-20)
MM.		WWW.	5			μs	LP osc mode
WW.1		Oscillator Period	250	$C_{\overline{\Omega}_{j_{A}}}$		ns	RC osc mode
W W		(Note 1)	250	 1	10,000	ns	XT osc mode
MW.		CO. TA MAN	250	Y.Co.	250	ns	HS osc mode (-04)
		COM	100	~ _ C0	250	ns	HS osc mode (-10)
M. A.		T. OWITH	50	0 . ~	250	ns	HS osc mode (-20)
WW		W.Co. TW WW	5	005°	- T	μs	LP osc mode
2	Tcy	Instruction Cycle Time (Note 1)	200	Tcy	DC	ns	Tcy = 4/Fosc
3	TosL,	External Clock in (OSC1) High or	100	10 <u>n</u> ,	COM.	ns	XT oscillator
W	TosH	Low Time	2.5	1407	= 1	μs	LP oscillator
		COM	15	1.1	$^{\Lambda}$. $\mathbb{C}_{\overline{\mathbb{O}}_{N}}$,	ns	HS oscillator
4	TosR,	External Clock in (OSC1) Rise or	"	W.700	25	ns	XT oscillator
	TosF	Fall Time	1/N	-10	50	ns	LP oscillator
		N.In COM.	11	Min	15	ns	HS oscillator

[†] Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (TCY) equals four times the input oscillator time-base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1/CLKIN pin. When an external clock input is used, the "Max." cycle time limit is "DC" (no clock) for all devices.

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FIGURE 19-3: CLKOUT AND I/O TIMING

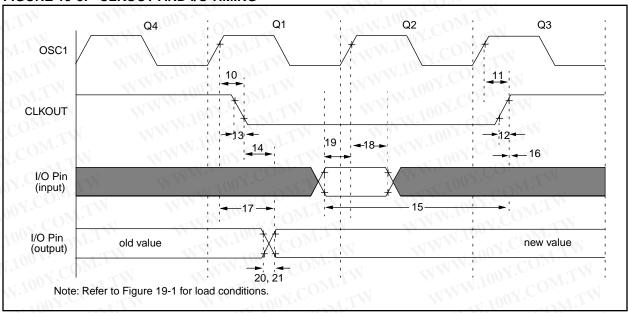


TABLE 19-3: CLKOUT AND I/O TIMING REQUIREMENTS

Parameters	Sym	Characteristic	OY.	Min	Typ†	Max	Units	Conditions
10*	TosH2ckL	OSC1↑ to CLKOUT↓	WA'CO		75	200	ns	Note 1
11*	TosH2ckH	OSC1↑ to CLKOUT↑		TH	75	200	ns	Note 1
12*	TckR	CLKOUT rise time	Ton CO		35	100	ns	Note 1
13*	TckF	CLKOUT fall time	V.100 - 1 CC	W.F.	35	100	ns	Note 1
14*	TckL2ioV	CLKOUT ↓ to Port out valid	W.1001.	OM_{TLA}	_	0.5Tcy + 20	ns	Note 1
15*	TioV2ckH	Port in valid before CLKOUT ↑	100Y.C	Tosc + 200	_	77.	ns	Note 1
16*	TckH2iol	Port in hold after CLKOUT ↑	0 1	N_	4/1/1	ns	Note 1	
17*	TosH2ioV	OSC1↑ (Q1 cycle) to Port out va	COM	50	150	ns	1007.CC	
18*	TosH2iol	OSC1 [†] (Q2 cycle) to Port input invalid (I/O in hold time)	PIC16 C 62A/ R62/64A/R64	100	T	- 1	ns	V.100Y.C
	NWW.	100Y.COM.TW	PIC16 LC 62A/ R62/64A/R64	200	V.Ŧ.	_ 1	ns	M.100X.
19*	TioV2osH	Port input valid to OSC1 [↑] (I/O in	setup time)	0 00	$\overline{M_r}$		ns	Miran
20*	TioR	Port output rise time	PIC16 C 62A/ R62/64A/R64	1007.C	10	40	ns	MM:100
	WW	W.100Y.COM.TW	PIC16 LC 62A/ R62/64A/R64	N.100Y.	<u>70</u> 24	80	ns	NWW.1
21*	TioF	Port output fall time	PIC16 C 62A/ R62/64A/R64	1. 1007	10	40	ns	MMM
		WW.1003.COM.1	PIC16 LC 62A/ R62/64A/R64	11/1/100	80	80	ns	WWV
22††*	Tinp	RB0/INT pin high or low time	W	TCY	n os i.		ns	MM
23††*	Trbp	RB7:RB4 change int high or low	time	Tcy	-T/	COA	ns	W

^{*} These parameters are characterized but not tested.

Note 1: Measurements are taken in RC Mode where CLKOUT output is 4 x Tosc.

[†] Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

^{††} These parameters are asynchronous events not related to any internal clock edge.

FIGURE 19-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING

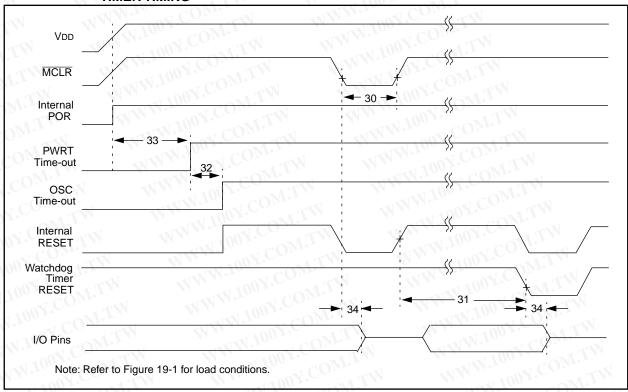


FIGURE 19-5: BROWN-OUT RESETTIMING

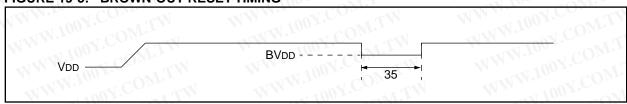


TABLE 19-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER, AND BROWN-OUT RESET REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
30	TmcL	MCLR Pulse Width (low)	2	1.1007	OM.	μs	VDD = 5V, -40°C to +125°C
31*	Twdt	Watchdog Timer Time-out Period (No Prescaler)	7	18	33	ms	VDD = 5V, -40°C to +125°C
32	Tost	Oscillation Start-up Timer Period		1024Tosc		-	Tosc = OSC1 period
33*	Tpwrt	Power-up Timer Period	28	72	132	ms	VDD = 5V, -40°C to +125°C
34	Tıoz	I/O Hi-impedance from MCLR Low or WDT Reset		11/N 100	2.1	μs	CM MMM.
35	TBOR	Brown-out Reset Pulse Width	100	WINE WALL	<u>√√</u> .	μs	VDD ≤ BVDD (param. D005)

^{*} These parameters are characterized but not tested.

[†] Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 19-6: TIMERO AND TIMER1 EXTERNAL CLOCK TIMINGS

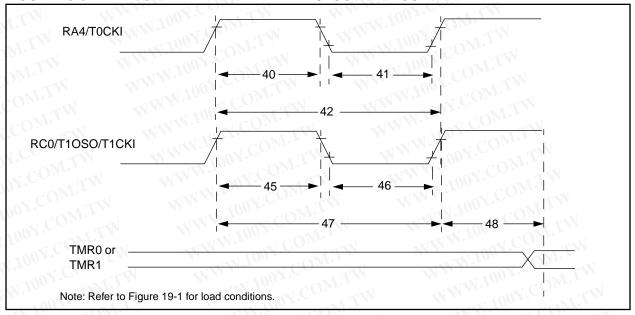


TABLE 19-5: TIMERO AND TIMER1 EXTERNAL CLOCK REQUIREMENTS

Param No.	Sym	Characteristic	WWW	1.100Y.	Min	Тур†	Max	Units	Conditions
40*	Tt0H	T0CKI High Pulse V	Vidth	No Prescaler	0.5Tcy + 20		-315	ns	Must also meet
	. Voo.	TON		With Prescaler	10	-1	— ns	ns	parameter 42
41*	TtOL	T0CKI Low Pulse V	/idth	No Prescaler	0.5Tcy + 20	I —	a T N	ns	Must also meet
	11007	TIME		With Prescaler	10	I —	47	ns	parameter 42
42*	Tt0P	TOCKI Period		No Prescaler	Tcy + 40	I —	4	ns	1007.00
	WW.100			With Prescaler	Greater of: 20 or <u>Tcy + 40</u> N	_	-1/	ns	N = prescale value (2, 4,, 256)
45*	Tt1H	T1CKI High Time	Synchronous, F	Prescaler = 1	0.5Tcy + 20	_	-	ns	Must also meet parameter 47
	L.WW.	o COM.	Synchronous,	PIC16 C 6X	15	da —	_	ns	
	NV	100 J. COM	Prescaler = 2,4,8	PIC16LC6X	25		_	ns	
	MAI	100 Y.	Asynchronous	PIC16 C 6X	30	Y -	_	ns	-XIXI.100
		L. COL	W	PIC16LC6X	50	4	_	ns	1007.
46*	Tt1L	T1CKI Low Time	Synchronous, F	Prescaler = 1	0.5Tcy + 20	_	_	ns	Must also meet
	WW	1007.00	Synchronous,	PIC16 C 6X	15	TV	<u> </u>	ns	parameter 47
	W	MAN TOO Y.C.	Prescaler = 2,4,8	PIC16LC6X	25		N-	ns	WWW. 100
		WW.IO	Asynchronous	PIC16 C 6X	30) - ·	AV.	ns	WWW
		1007.		PIC16 LC 6X	50	JA.	F	ns	W.10
47*	Tt1P	T1CKI input period	Synchronous	PIC16 C 6X	Greater of: 30 OR TCY + 40 N	coM		ns	N = prescale value (1, 2, 4, 8)
		M.M.100	Y.COM.	PIC16 LC 6X	Greater of: 50 OR TCY + 40 N		M.T	W	N = prescale value (1, 2, 4, 8)
		WW	Asynchronous	PIC16 C 6X	60	F	\ <u>#</u> [ns	1
		TWW.L	COM	PIC16LC6X	100	A+C	Ož	ns	W.W.
	Ft1	Timer1 oscillator in (oscillator enabled l			DC		200	kHz	I W
48	TCKEZtmr1	Delay from external	clock edge to tir	mer increment	2Tosc	- J	7Tosc	47.	

These parameters are characterized but not tested.

[†] Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 19-7: CAPTURE/COMPARE/PWM TIMINGS (CCP1)

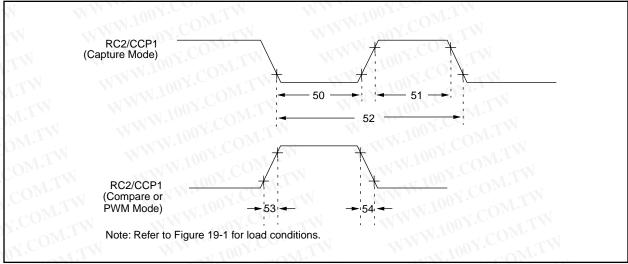


TABLE 19-6: CAPTURE/COMPARE/PWM REQUIREMENTS (CCP1)

Parameter No.	Sym	Characteristic	WWW.100	Y.COM.TW	Min	Тур†	Max	Units	Conditions
50*	TccL	CCP1	No Prescaler	No Prescaler		VIII		ns	TW
	CO	input low time	With Prescaler	PIC16 C 62A/R62/ 64A/R64	10		4170	ns	OM.TW
VW.100	V.CC	OWIN	WWW.	PIC16 LC 62A/R62/ 64A/R64	20	NT.		ns	COM.TW
51*	TccH	CCP1	No Prescaler	N.1001.	0.5Tcy + 20	7		ns	COM
WWW.10	00 Y	input high time	With Prescaler	PIC16 C 62A/R62/ 64A/R64	10	=1)		ns	N.COM.TV
	700 x	Y.COM.TW	W.	PIC16 LC 62A/R62/ 64A/R64	20	_	W	ns	OOX.COM.
52*	TccP	CCP1 input period	N N	WW.100Y.C	3Tcy + 40 N	_	4	ns	N = prescale value (1,4 or 16)
53*	TccR	CCP1 output rise	time	PIC16 C 62A/R62/ 64A/R64	CONTTY	10	25	ns	N.1001.CO
	MAM TOOX COW L			PIC16 LC 62A/R62/ 64A/R64	Y.COM.	25	45	ns	M.Toox.CC
54*	TccF			PIC16 C 62A/R62/ 64A/R64	$^{0.7}$ C $^{0.0}$	10	25	ns	MAN. TOOX.C
	WW	VW.100X.CO		PIC16 LC 62A/R62/ 64A/R64	OOX.COM	25	45	ns	MM.1007.

^{*} These parameters are characterized but not tested.

[†] Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 19-8: PARALLEL SLAVE PORT TIMING (PIC16C64A/R64)

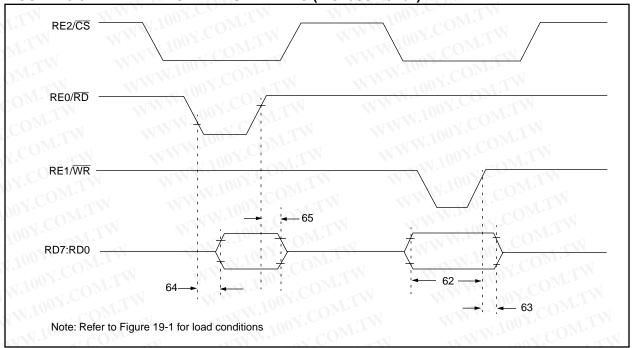


TABLE 19-7: PARALLEL SLAVE PORT REQUIREMENTS (PIC16C64A/R64)

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions	
62	TdtV2wrH	Data in valid before WR↑ or CS↑ (setup time)		20		N T	ns	COM
	N.100Y.	COM.TW WWW	100X.COM	25	_	MN.	ns	Extended Range Only
63*	TwrH2dtl	WR↑ or CS↑ to data–in invalid (hold	PIC16 C 64A/R64	20	i —	= 1	ns	CO
	100	time)	PIC16 LC 64A/R64	35			ns	100
64	TrdL2dtV	RD↓ and CS↓ to data–out valid	1007.00	TT	W	80	ns	1007
	WW.10	OX.COM.TW W	MM.100X.Co	OM:	4	90	ns	Extended Range Only
65*	TrdH2dtl	RD↑ or CS↑ to data–out invalid	1001.	10	1.17	30	ns	W.100

^{*} These parameters are characterized but not tested.

[†] Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 19-9: SPI MODE TIMING

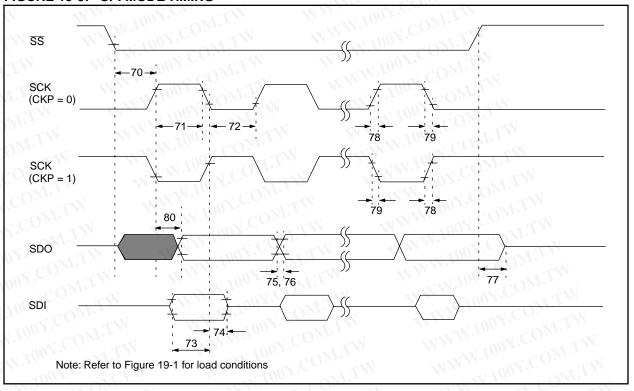


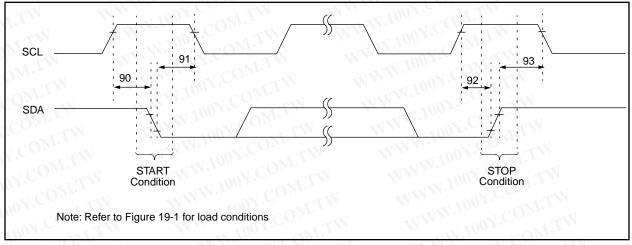
TABLE 19-8: SPI MODE REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Тур†	Max	Units	Conditions	
70*	TssL2scH, TssL2scL	SS↓ to SCK↓ or SCK↑ input	Tcy	_	MM	ns	N.COM.	
71*	TscH	SCK input high time (slave mode)	Tcy + 20	N —	_N	ns	OY.Co	
72*	TscL	SCK input low time (slave mode)	Tcy + 20	cal—		ns	ON COM	
73*	50	TW	_	ns	100X'CO			
74*	50	I.TN	_	ns	N.100 A.C.			
75*	100 7	10	25	ns	W.1001.			
76*	100¥.C	10	25	ns	11001			
77* TssH2doZ SS↑ to SDO output hi-impedance			10	01/12	50	ns	MAN.	
78*	N.100	10	25	ns	WW.IO			
79*	TscF	SCK output fall time (master mode)	10^{100}	10	25	ns	W.10	
80*	M.1001		50	ns	WWW.10			

^{*} These parameters are characterized but not tested.

[†] Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 19-10: I²C BUS START/STOP BITS TIMING



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I²C BUS START/STOP BITS REQUIREMENTS **TABLE 19-9:**

Parameter No.	Sym	Characteristic	W.100 1. CO	Min	Тур	Max	Units	Conditions
90*	Tsu:sta	START condition	100 kHz mode	4700			ns	Only relevant for repeated START condition
		Setup time	400 kHz mode	600	44	_		
91*	THD:STA START condition 100 kHz mode 4000 — —		201	After this period the first clock				
	CON	Hold time	400 kHz mode	600	_	1 —	ns	pulse is generated
92*		STOP condition Setup time	100 kHz mode	4700	1	_	ns	111,100 COM: 1
			400 kHz mode	600	7	W-		WWW TOOK.COM.TY
93*	THD:STO	STOP condition Hold time	100 kHz mode	4000	NE.	N.		MM. COB
			400 kHz mode	600	Æ.	1 4	ns	W. 100 F. COM.

^{*}These parameters are characterized but not tested.

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FIGURE 19-11: I²C BUS DATA TIMING

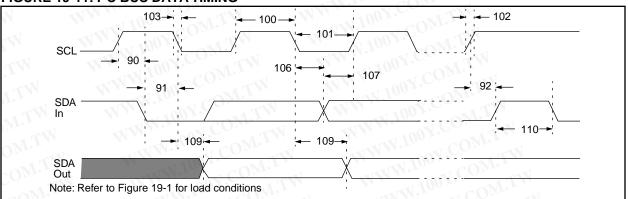


TABLE 19-10: I²C BUS DATA REQUIREMENTS

Parameter No.	Sym	Characteristic	NY.COM.TY	Min	Max	Units	Conditions
100*	THIGH	Clock high time	100 kHz mode	4.0	WAN	μs	Device must operate at a minimum of 1.5 MHz
100Y.CC		N WWW.	400 kHz mode	0.6	A W	μs	Device must operate at a minimum of 10 MHz
O.V.C			SSP Module	1.5TcY	7//	-11	101.
101*	TLOW	Clock low time	100 kHz mode	4.7	-41	μs	Device must operate at a minimum of 1.5 MHz
1007		IN MA	400 kHz mode	1.3	- <	μs	Device must operate at a minimum of 10 MHz
1 11.		TW W	SSP Module	1.5TcY	_	111 4.	11001.
102*	TR	SDA and SCL rise	100 kHz mode	DIV-	1000	ns	W. CO. TV
WW.10		time	400 kHz mode	20 + 0.1Cb	300	ns	Cb is specified to be from 10-400 pF
103*	TF	SDA and SCL fall time	100 kHz mode	COM	300	ns	MIN. TO COM.
MM		OM.TW	400 kHz mode	20 + 0.1Cb	300	ns	Cb is specified to be from 10-400 pF
90*	Tsu:sta	START condition	100 kHz mode	4.7	7.47	μs	Only relevant for repeated
		setup time	400 kHz mode	0.6	T = 1	μs	START condition
91*	THD:STA	START condition hold	100 kHz mode	4.0	· • •	μs	After this period the first clock
WW		time	400 kHz mode	0.6	TY	μs	pulse is generated
106* THD:DA		Data input hold time	100 kHz mode	0 0		ns	MAN CON CO.
		ON.TW	400 kHz mode	1000	0.9	μs	W.100 CO
107*	TSU:DAT	Data input setup time	100 kHz mode	250	-17	ns	Note 2
~ 1		An COM.	400 kHz mode	100	$0_{\overline{m}}$.	ns	TWW.IC
92*	Tsu:sto	J:STO STOP condition setup time	100 kHz mode	4.7	. 	μs	100°
			400 kHz mode	0.6		μs	WWW.
109*	TAA	Output valid from	100 kHz mode	TIN .	3500	ns	Note 1
		clock	400 kHz mode	7 700		ns	1003
110*	TBUF	Bus free time	100 kHz mode	4.7	√ € 0	μs	Time the bus must be free
		W.100X.COM.	400 kHz mode	1.3	V.C	μs	before a new transmission can start
	Cb	Bus capacitive loading	.1.	7. 1. 1V	400	pF	1 .10

These parameters are characterized but not tested.

- Note 1: As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (min. 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.
 - 2: A fast-mode (400 kHz) I²C-bus device can be used in a standard-mode (100 kHz) I²C-bus system, but the requirement tsu;DAT ≥ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line TR max.+tsu;DAT = 1000 + 250 = 1250 ns (according to the standard-mode I²C bus specification) before the SCL line is released.

Applicable Devices 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67 W.100Y.COM.TW

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20.0 ELECTRICAL CHARACTERISTICS FOR PIC16C65

Absolute Maximum Ratings † Ambient temperature under bias.....-55°C to +85°C Voltage on any pin with respect to Vss (except VDD, MCLR, and RA4)-0.3V to (VDD + 0.3V) Voltage on VDD with respect to Vss-0.3V to +7.5V Input clamp current, IIK (VI < 0 or VI > VDD)±20 mA Output clamp current, lok (Vo < 0 or Vo > VDD)......±20 mA

Note 1: Power dissipation is calculated as follows: Pdis = VDD x {IDD - Σ IOH} + Σ {(VDD-VOH) x IOH} + Σ (Vol x IOL)

Note 2: Voltage spikes below Vss at the \overline{MCLR} pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100 Ω should be used when applying a "low" level to the \overline{MCLR} pin rather than pulling this pin directly to Vss.

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 20-1: CROSS REFERENCE OF DEVICE SPECS FOR OSCILLATOR CONFIGURATIONS AND FREQUENCIES OF OPERATION (COMMERCIAL DEVICES)

osc	PIC16C65-04	PIC16C65-10	PIC16C65-20	PIC16LC65-04	JW Devices
RC	VDD: 4.0V to 6.0V IDD: 5 mA max. at 5.5V IPD: 21 µA max. at 4V Freq: 4 MHz max.	VDD: 4.5V to 5.5V IDD: 2.7 mA typ. at 5.5V IPD: 1.5 μA typ. at 4V Freq: 4 MHz max.	VDD: 4.5V to 5.5V IDD: 2.7 mA typ. at 5.5V IPD: 1.5 μA typ. at 4V Freq: 4 MHz max.	VDD: 3.0V to 6.0V IDD: 3.8 mA max. at 3V IPD: 800 µA max. at 3V Freq: 4 MHz max.	VDD: 4.0V to 6.0V IDD: 5 mA max. at 5.5V IPD: 21 µA max. at 4V Freq: 4 MHz max.
XT	VDD: 4.0V to 6.0V IDD: 5 mA max. at 5.5V IPD: 21 µA max. at 4V Freq: 4 MHz max.	VDD: 4.5V to 5.5V IDD: 2.7 mA typ. at 5.5V IPD: 1.5 μA typ. at 4V Freq: 4 MHz max.	VDD: 4.5V to 5.5V IDD: 2.7 mA typ. at 5.5V IPD: 1.5 μA typ. at 4V Freq: 4 MHz max.	VDD: 3.0V to 6.0V IDD: 3.8 mA max. at 3V IPD: 800 µA max. at 3V Freq: 4 MHz max.	VDD: 4.0V to 6.0V IDD: 5 mA max. at 5.5V IPD: 21 µA max. at 4V Freq: 4 MHz max.
HS	VDD: 4.5V to 5.5V IDD: 13.5 mA typ. at 5.5V	VDD: 4.5V to 5.5V IDD: 15 mA max. at 5.5V	5.5V	Not recommended for use in HS mode	VDD: 4.5V to 5.5V IDD: 30 mA max. at 5.5V
	IPD: 1.5 μA typ. at 4.5V Freq: 4 MHz max.	IPD 1.0 μA typ. at 4.5V Freq: 10 MHz max.	IPD: 1.5 μA typ. at 4.5V Freq: 20 MHz max.	OY.COM.TW	IPD: 1.5 μA typ. at 4.5V Freq: 20 MHz max.
LP	VDD: 4.0V to 6.0V IDD: 52.5 μA typ. at 32 kHz, 4.0V IPD: 0.9 μA typ. at 4.0V Freq: 200 kHz max.	Not recommended for use in LP mode	Not recommended for use in LP mode	VDD: 3.0V to 6.0V IDD: 105 μA max. at 32 kHz, 3.0V IPD: 800 μA max. at 3.0V Freq: 200 kHz max.	VDD: 3.0V to 6.0V IDD: 105 μA max. at 32 kHz, 3.0V IPD: 800 μA max. at 3.0V Freq: 200 kHz max.

The shaded sections indicate oscillator selections which are tested for functionality, but not for MIN/MAX specifications. It is recommended that the user select the device type that ensures the specifications required.

Applicable Devices 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

20.1 DC Characteristics: PIC16C65-04 (Commercial, Industrial)

PIC16C65-10 (Commercial, Industrial)

PIC16C65-20 (Commercial, Industrial)

DC CHA	RACTERISTICS	Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C $\leq \text{TA} \leq +85^{\circ}\text{C}$ for industrial and 0°C $\leq \text{TA} \leq +70^{\circ}\text{C}$ for commercial							
Param No.			Min	Typ†	Max	Units	Conditions		
D001 D001A	Supply Voltage	VDD	4.0 4.5	TW	6.0 5.5	V	XT, RC and LP osc configuration HS osc configuration		
D002*	RAM Data Retention Voltage (Note 1)	VDR		1.5	V -	V	NWW.100Y.COM.TW		
D003	VDD start voltage to ensure internal Power-on Reset signal	VPOR	10 Y.C.	Vss	LM M	V	See section on Power-on Reset for details		
D004*	VDD rise rate to ensure internal Power-on Reset signal	SVDD	0.05	COV	W.T.	V/ms	See section on Power-on Reset for details		
D010	Supply Current (Note 2, 5)	IDD	M.700	2.7	5	mA	XT, RC osc configuration FOSC = 4 MHz, VDD = 5.5V (Note 4)		
D013	OOY.COM.TW	WW	NN.	13.5	30	mA	HS osc configuration Fosc = 20 MHz, VDD = 5.5V		
D020 D021 D021A	Power-down Current (Note 3, 5)	IPD	WW.	10.5 1.5 1.5	800 800 800	μA μA uA	VDD = 4.0V, WDT enabled,-40°C to +85°C VDD = 4.0V, WDT disabled,-0°C to +70°C VDD = 4.0V, WDT disabled,-40°C to +85°C		

- These parameters are characterized but not tested.
- † Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.
- Note 1: This is the limit to which VDD can be lowered without losing RAM data.
 - 2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
 - The test conditions for all IDD measurements in active operation mode are:
 - OSC1 = external square wave, from rail to rail; all I/O pins tristated, pulled to VDD,
 - MCLR = VDD; WDT enabled/disabled as specified.
 - 3: The power down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and Vss.
 - 4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kOhm.
 - 5: Timer1 oscillator (when enabled) adds approximately 20 μA to the specification. This value is from characterization and is for design guidance only. This is not tested.

20.2 DC Characteristics: PIC16LC65-04 (Commercial, Industrial)

DC CH	ARACTERISTICS	Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq \text{TA} \leq +85^{\circ}\text{C}$ for industrial and $0^{\circ}\text{C} \leq \text{TA} \leq +70^{\circ}\text{C}$ for commercial							
Param No.	Characteristic	Sym	m Min	Тур†	Max	Units	Conditions		
D001	Supply Voltage	VDD	3.0	-	6.0	V	LP, XT, RC osc configuration (DC - 4 MHz)		
D002*	RAM Data Retention Voltage (Note 1)	VDR	M.	1.5	-	V	N TOOK COMETA		
D003	VDD start voltage to ensure internal Power-on Reset signal	VPOR	OM:	Vss	-	V	See section on Power-on Reset for details		
D004*	VDD rise rate to ensure internal Power-on Reset signal	SVDD	0.05	1.TV	-	V/ms	See section on Power-on Reset for details		
D010	Supply Current (Note 2, 5)	IDD	N.CC	2.0	3.8	mA	XT, RC osc configuration FOSC = 4 MHz, VDD = 3.0V (Note 4)		
D010A	OW.TAN M.	NW.	00Y.	22.5	105	μΑ	LP osc configuration Fosc = 32 kHz, VDD = 4.0V, WDT disabled		
D020 D021 D021A	Power-down Current (Note 3, 5)	IPD	1007	7.5 0.9 0.9	800 800 800	μΑ μΑ μΑ	VDD = 3.0V, WDT enabled, -40°C to +85°C VDD = 3.0V, WDT disabled, 0°C to +70°C VDD = 3.0V, WDT disabled, -40°C to +85°C		

- * These parameters are characterized but not tested.
- † Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.
- Note 1: This is the limit to which VDD can be lowered without losing RAM data.
 - 2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
 - The test conditions for all IDD measurements in active operation mode are:
 - OSC1 = external square wave, from rail to rail; all I/O pins tristated, pulled to VDD,
 - MCLR = VDD; WDT enabled/disabled as specified.
 - 3: The power down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and Vss.
 - 4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kOhm.
 - 5: Timer1 oscillator (when enabled) adds approximately 20 μA to the specification. This value is from characterization and is for design guidance only. This is not tested.

DC CHARACTERISTICS

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Applicable Devices 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

20.3 DC Characteristics: PIC16C65-04 (Commercial, Industrial)

PIC16C65-10 (Commercial, Industrial) PIC16C65-20 (Commercial, Industrial)

PIC16LC65-04 (Commercial, Industrial)

Standard Operating Conditions (unless otherwise stated)

Operating temperature $-40^{\circ}\text{C} \le \text{TA} \le +85^{\circ}\text{C}$ for industrial and $0^{\circ}\text{C} \le \text{TA} \le +70^{\circ}\text{C}$ for commercial

Operating voltage VDD range as described in DC spec Section 20.1 and

Param No.	Characteristic	Sym	Min	Typ †	Max	Units	Conditions
N.CO	Input Low Voltage	Y.Co.	WT		MM	110	DY.COS NITH
	I/O ports	VIL	TW		WW	W	OV.COM
D030	with TTL buffer	, cO	Vss	-	0.15VDD	V	For entire VDD range
D030A	W W	001.00	Vss	-	V8.0	V	$4.5V \le VDD \le 5.5V$
D031	with Schmitt Trigger buffer	N.C	Vss	V -	0.2VDD	V	TW.CO. TW
D032 D033	MCLR, OSC1(in RC mode) OSC1 (in XT, HS and LP)	100	Vss Vss	<u>-</u>	0.2VDD 0.3VDD	V	Note1
5	Input High Voltage	100 2.	700	N N	0.0 100	-731	N. COM
	I/O ports	VIH	·	L_{IM}		41.	M 100 Y. COM. TW
D040	with TTL buffer	W. 22	2.0	· (*)	VDD	V	4.5V ≤ VDD ≤ 5.5V
D040A	ON. COM.	M.100	0.25VDD	7 · 7	VDD	V	For entire VDD range
	OOY.COM.TW	W.10	+ 0.8V	M.T	N	10	MM:1001. COW:1
D041	with Schmitt Trigger buffer	W	0.8VDD	Λ_{II}	VDD		For entire VDD range
D041	MCLR	MMM	0.8VDD) 2- I	VDD	V	To entire VDD range
D042A	OSC1 (XT, HS and LP)	WW	0.7 VDD	OD	VDD	V	Note1
D043	OSC1 (in RC mode)	111	0.9VDD	ani	VDD	V	COM.
D070	PORTB weak pull-up current	IPURB	50	250	400	μΑ	VDD = 5V, VPIN = VSS
W	Input Leakage Current (Notes 2, 3)	MM	JW.100	[.C	OM.TY	- 1	WWW.100X.CON
D060 🕥	I/O ports	IIL 1	WW.10		±1.1	μΑ	Vss ≤ VPIN ≤ VDD, Pin at himpedance
D061	MCLR, RA4/T0CKI	111	- V.1)0 <u> </u>	±5	μΑ	Vss ≤ Vpin ≤ Vdd
D063	OSC1		MAN.	0-0	±5	μA	Vss ≤ VPIN ≤ VDD, XT, HS, and LP osc configuration
	Output Low Voltage	- T	TO NOT W	To	-1 CO	M	N. TOWN. 100 N
D080	I/O ports	VoL	W.N.	N.1	0.6	V	IOL = 8.5 mA , VDD = 4.5V , -40°C to $+85^{\circ}\text{C}$
D083	OSC2/CLKOUT (RC osc config)		17.	1	0.6	OV.	IOL = 1.6 mA, VDD = 4.5V, -40°C to +85°C
	Output High Voltage		***	WW	· V	CO_{2}	WWW.
D090	I/O ports (Note 3)	Voн	VDD-0.7	W	N.100	1.00	IOH = -3.0 mA, VDD = 4.5 V, -40 °C to $+85$ °C
D092	OSC2/CLKOUT (RC osc config)	MITW	VDD-0.7	WA	M.To.	V	IOH = -1.3 mA, VDD = 4.5V, -40°C to +85°C
D150*	Open-Drain High Voltage	Vod	-	4	14	V	RA4 pin

These parameters are characterized but not tested.

[†] Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C6X be driven with external clock in RC mode.

^{2:} The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

^{3:} Negative current is defined as current sourced by the pin.

DC CHA	ARACTERISTICS	Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq \text{TA} \leq +85^{\circ}\text{C}$ for industrial and $0^{\circ}\text{C} \leq \text{TA} \leq +70^{\circ}\text{C}$ for commercial Operating voltage VDD range as described in DC spec Section 20.1 and Section 20.2							
Param No.	Characteristic	Sym	Min	Typ †	Max	Units	Conditions		
M.TW	Capacitive Loading Specs on Output Pins	TW	4	N	W.100	I.C.	M.TW		
D100	OSC2 pin	Cosc ₂	-	41.0	15	pF	In XT, HS and LP modes when external clock is used to drive OSC1.		
D101 D102	All I/O pins and OSC2 (in RC mode) SCL, SDA in I ² C mode	Cio Cb	N -	- 1	50 400	pF pF	CONT.TW		

- These parameters are characterized but not tested.
- Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only +
- Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C6X be driven with external clock in RC mode
 - The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.
 - 3: Negative current is defined as current sourced by the pin.

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PIC16C6X

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Timing Parameter Symbology

The timing parameter symbols have been created following one of the following formats:

1. TppS2ppS		3. Tcc:st	(I ² C specifications only)
2. TppS	WW. 1001.	4. Ts	(I ² C specifications only)

T	MM	100 Y.Co	WTI		1007.0	WI.IV	
CF	Frequency			T	Time		

Lowercase letters (pp) and their meanings:

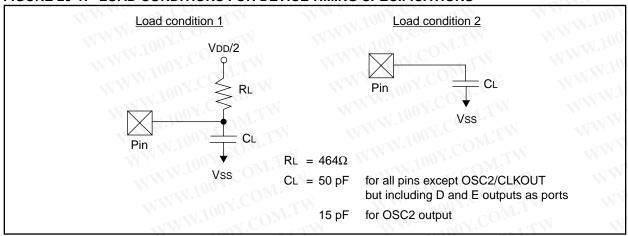
pp	M. 100x. C.W.IM		W.1001.
cc	CCP1	osc	OSC1
ck	CLKOUT	√ rd	RD
cs	CS	rw	RD or WR
di	SDI	sc	SCK
do CO	SDO	SS	SS
dt	Data in	t0	TOCKI COMPANY
io	I/O port	t1	T1CKI
mc	MCLR	wr	WR

Uppercase letters and their meanings:

S	CONTINUE	OWIT	I COM.
F	Fall	100 Y. P. T.	Period
Н	High	R	Rise
	Invalid (Hi-impedance)	N. TO.	Valid
L 1	Low	W.100 ZOM	Hi-impedance Control of the Hi-impedance
I ² C only		W.100 Y. COM	
AA	output access	High	High
BUF	Bus free	Low	Low

CC	7 100 X. TW	100 1.	OMIT	M.Ing. COJ
HD	Hold	SU	Setup	
ST		WWW.		
DAT	DATA input hold	STO	STOP condition	
STA	START condition	71 100		

FIGURE 20-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS



20.5 <u>Timing Diagrams and Specifications</u>

FIGURE 20-2: EXTERNAL CLOCK TIMING

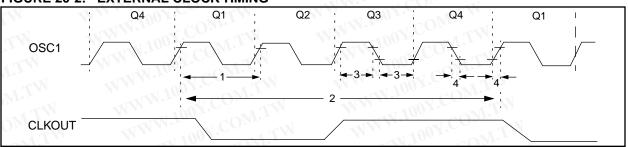


TABLE 20-2: EXTERNAL CLOCK TIMING REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Тур†	Max	Units	Conditions
COM.	Fosc	External CLKIN Frequency	DC	_	4	MHz	XT and RC osc mode
	In	(Note 1)	DC	_	4	MHz	HS osc mode (-04)
	WT	MM 1007.CO.	DC	_	10	MHz	HS osc mode (-10)
	7. 7	CO.	DC	× –	20	MHz	HS osc mode (-20)
	M.I.V	W. 100 1.	DC	_	200	kHz	LP osc mode
		Oscillator Frequency	DC	M	4	MHz	RC osc mode
	DIM.	(Note 1)	0.1		4	MHz	XT osc mode
	OM.	M. 100 F.	4	<u> </u>	20	MHz	HS osc mode
		LA MM, 100X	5		200	kHz	LP osc mode
M. 1007	Tosc	External CLKIN Period	250		_	ns	XT and RC osc mode
	100	(Note 1)	250	M <u>. </u>		ns	HS osc mode (-04)
	Y.Co.	WIT WITTON	100	ATT	N _	ns	HS osc mode (-10)
	< 1 CO	NI.	50	OME	N -	ns	HS osc mode (-20)
	7.	OM:I	5	~0 2 /• ;	<u> </u>	μs	LP osc mode
	OY.C	Oscillator Period	250		1.1.1.	ns	RC osc mode
		(Note 1)	250	Can	10,000	ns	XT osc mode
	700 7.	COMIT	250	-O1	250	ns	HS osc mode (-04)
	1007	NITH WIT	100	\ <u></u>	250	ns	HS osc mode (-10)
	1.10	COM, WAY	50	N .C U	250	ns	HS osc mode (-20)
	N.100	COM.	5	7 C	DNF.	μs	LP osc mode
2	Tcy	Instruction Cycle Time (Note 1)	200	TCY	DC	ns	Tcy = 4/Fosc
3	TosL,	External Clock in (OSC1) High or	50	· Kino	W= 1	ns	XT oscillator
	TosH	Low Time	2.5	Too V	CONT.	μs	LP oscillator
	VN	100Y. WITH	15	4.1 9 07	ME	ns	HS oscillator
4	TosR,	External Clock in (OSC1) Rise or	NAN	- 00	25	ns	XT oscillator
	TosF	Fall Time	-TXX	11700	50	ns	LP oscillator
	MM.	1100Y.	15 1	- 10	15	ns	HS oscillator

[†] Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (TCY) equals four times the input oscillator time-base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1/CLKIN pin. When an external clock input is used, the "Max." cycle time limit is "DC" (no clock) for all devices.

FIGURE 20-3: CLKOUT AND I/O TIMING

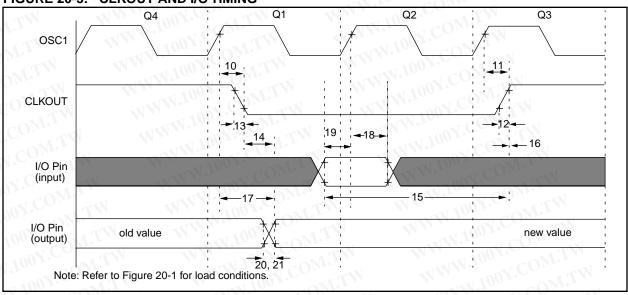


TABLE 20-3: CLKOUT AND I/O TIMING REQUIREMENTS

Parameter No.	Sym	Characteristic	OON.COM	Min	Typ†	Max	Units	Conditions
10*	TosH2ckL	OSC1↑ to CLKOUT↓	SC1↑ to CLKOUT↓		75	200	ns	Note 1
11*	TosH2ckH	OSC1↑ to CLKOUT↑	1.100 F. CC	M. I	75	200	ns	Note 1
12*	TckR	CLKOUT rise time	W.1007.	OW.T.	35	100	ns	Note 1
13*	TckF	CLKOUT fall time	CLKOUT fall time		35	100	ns	Note 1
14*	TckL2ioV	CLKOUT ↓ to Port out valid	CLKOUT ↓ to Port out valid		_	0.5Tcy + 20	ns	Note 1
15*	TioV2ckH	Port in valid before CLKOUT ↑		0.25Tcy + 25	(—	4111	ns	Note 1
16*	TckH2ioI	Port in hold after CLKOUT ↑	in hold after CLKOUT ↑		vi—	-111	ns	Note 1
17*	TosH2ioV	OSC1↑ (Q1 cycle) to Port out	OSC1↑ (Q1 cycle) to Port out valid		50	150	ns	LOS CC
18*	TosH2iol	OSC1↑ (Q2 cycle) to Port PIC16 C 65		100	1	_	ns	700 × C
		input invalid (I/O in hold time)	PIC16 LC 65	200	III	`	ns	N.100 1.
19*	TioV2osH	Port input valid to OSC1↑ (I/O	in setup time)	10070	1 T V		ns	W 100Y.
20*	TioR	Port output rise time	PIC16 C 65	100 1 .Co	10	1 25	ns	1003
	WWW	J. Tro COM.	PIC16 LC 65	N. P. O. T. C.C.) <u>.</u>	60	ns	NW
21*	TioF	Port output fall time	PIC16 C 65	M:10-	10	25	ns	MM
		W.100X.COM.TW	PIC16 LC 65	1/1/. <u>Mar</u>	c o N	60	ns	MW.In
22††*	Tinp	RB0/INT pin high or low time		Tcy	<u> </u>	1.77	ns	W.M.
23††*	Trbp 🕥	RB7:RB4 change int high or lo	w time	Tcy		M.TW	ns	W

^{*} These parameters are characterized but not tested.

Note 1: Measurements are taken in RC Mode where CLKOUT output is 4 x Tosc.

[†] Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

^{††} These parameters are asynchronous events not related to any internal clock edge.

FIGURE 20-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING

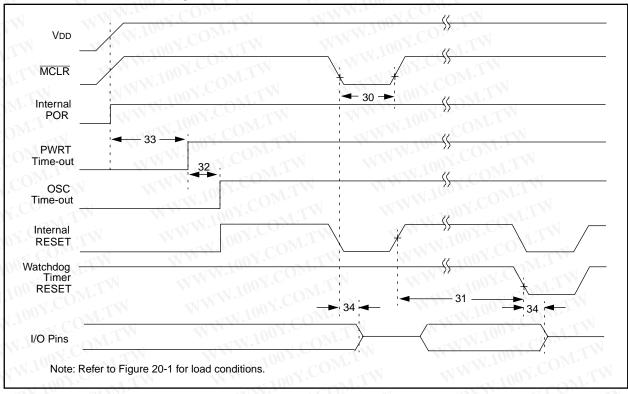


TABLE 20-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
30*	TmcL	MCLR Pulse Width (low)	100	T.M.T	W	ns	$VDD = 5V, -40^{\circ}C \text{ to } +85^{\circ}C$
31*	Twdt	Watchdog Timer Time-out Period (No Prescaler)	N.100	18	33	ms	$VDD = 5V, -40^{\circ}C \text{ to } +85^{\circ}C$
32	Tost	Oscillation Start-up Timer Period	11-10	1024Tosc	1.77	_	Tosc = OSC1 period
33*	Tpwrt	Power-up Timer Period or WDT reset	28	72	132	ms	$VDD = 5V, -40^{\circ}C \text{ to } +85^{\circ}C$
34	Tıoz	I/O Hi-impedance from MCLR Low	- 7 X	100 =	100	ns	W.100 x

^{*} These parameters are characterized but not tested.

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[†] Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 20-5: TIMERO AND TIMER1 EXTERNAL CLOCK TIMINGS

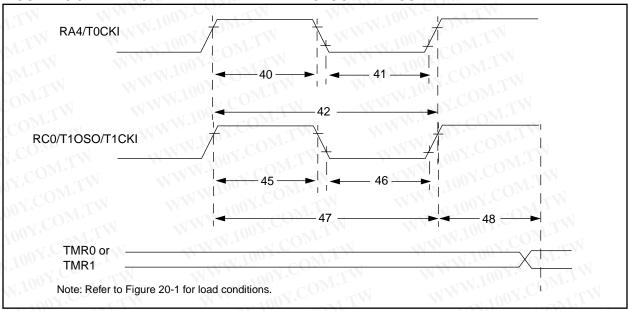


TABLE 20-5: TIMERO AND TIMER1 EXTERNAL CLOCK REQUIREMENTS

Param No.	Sym	Characteristic	WW	1.1007.	Min	Тур†	Max	Units	Conditions
40*	Tt0H	T0CKI High Pulse V	Vidth	No Prescaler	0.5Tcy + 20	3	=1	ns	Must also meet
		ON		With Prescaler	10	-1	11/11	ns	parameter 42
41*	TtOL	T0CKI Low Pulse W	Width No Prescaler		0.5Tcy + 20	 	-71	ns	Must also meet
	Y and Y			With Prescaler	10	 	AT.,	ns parameter 4	
42*	Tt0P	T0CKI Period	*X	No Prescaler	Tcy + 40	_	4/	ns	ON CO
	WW.100	ON.COM.TW W		With Prescaler	escaler Greater of: 20 or <u>Tcy + 40</u> N			ns	N = prescale value (2, 4,, 256)
45*	Tt1H	T1CKI High Time	Synchronous, F	Prescaler = 1	0.5Tcy + 20	<u> </u>	-1	ns	Must also meet
		M. Inc. COM.	Synchronous,	PIC16C6X	15		_	ns	parameter 47
	NN	100X.COM.	Prescaler = 2,4,8	PIC16 LC 6X	25	\ <u> </u>	_	ns	VV.100 1.
	MAN.	1007.	Asynchronous	PIC16C6X	30	1	_	ns	-TXV.100 1
		· LON CON	TW	PIC16LC6X	50	4	_	ns	TW LOOK
46*	Tt1L	T1CKI Low Time	Synchronous, F		0.5Tcy + 20	-	_	ns	Must also meet
		TOOY.CO	Synchronous,	PIC16 C 6X	15	T	_	ns	parameter 47
	WV	M.Ing.Y.Co	Prescaler = 2,4,8	PIC16LC6X	25		N-	ns	
		WWW.100Y.C	Asynchronous	PIC16 C 6X	30	P-	CAN	ns	
	1/1			PIC16LC6X	50	M.		ns	
47*	Tt1P	T1CKI input period Synchron	Synchronous	PIC16 C 6X	Greater of: 30 OR TCY + 40 N			ns	N = prescale value (1, 2, 4, 8)
		WWW.100	Y.COM.	PIC16 LC 6X	Greater of: 50 OR TCY + 40 N	CO	M.T	N	N = prescale value (1, 2, 4, 8)
		MM	Asynchronous	PIC16C6X	60			ns	NA .
		. WW. L	COM	PIC16LC6X	100	K+C	OF.	ns	WW
	Ft1	Timer1 oscillator inp (oscillator enabled by		0	DC		200	kHz	V W
48	TCKEZtmr1	Delay from external	clock edge to tir	mer increment	2Tosc	0	7Tosc	M-,	_1 .

These parameters are characterized but not tested.

[†] Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 20-6: CAPTURE/COMPARE/PWM TIMINGS (CCP1 AND CCP2)

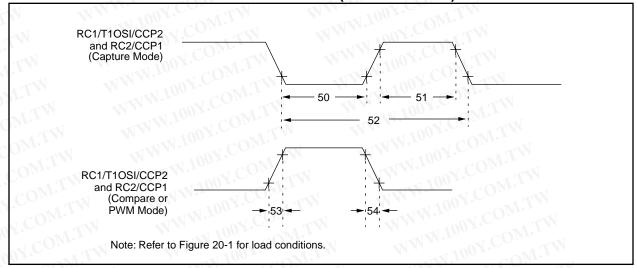


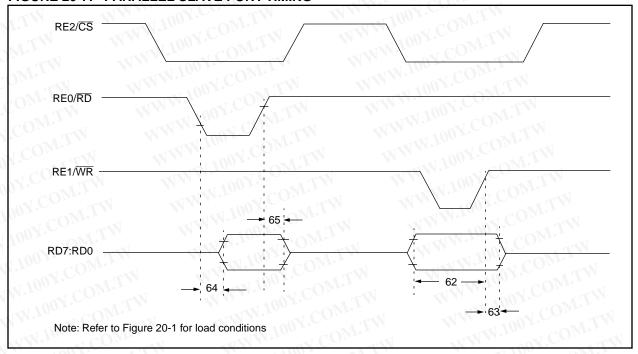
TABLE 20-6: CAPTURE/COMPARE/PWM REQUIREMENTS (CCP1 AND CCP2)

Parameter No.	Sym	Characteristic	MM.1007	COMITY	Min	Тур†	Max	Units	Conditions
50*	TccL	CCP1 and CCP2	No Prescaler	V.COM	0.5Tcy + 20	NAN	<u> </u>	ns	COM
	COM	input low time	With Prescaler	PIC16 C 65	10	- 	M	ns	COMP
		ATW	W 10	PIC16 LC 65	20	<u> </u>	N V	ns	COM
51*	TccH	CCP1 and CCP2	No Prescaler	001.	0.5Tcy + 20	7/	-1	ns	T. COM.TW
	V.CC	input high time	With Prescaler	PIC16 C 65	10	-	111	ns	OY.CO.TY
	- T C	OM	WWW.	PIC16 LC 65	20	_		ns	ON.COM
52*	TccP	CCP1 and CCP2 in	nput period	T.100Y.CC	3Tcy + 40 N		W	ns	N = prescale value (1,4, or 16)
53	TccR	CCP1 and CCP2 of	output rise time	PIC16 C 65	OF TAN	10	25	ns	-100 X.Co
	700.	COM.		PIC16 LC 65	$CO_{N\overline{P}}$	25	45	ns	A. T. CO.
54	TccF	CCP1 and CCP2 of	output fall time	PIC16 C 65	COMIT	10	25	ns	M. Jan T. CO.
	10	OY.COMITY		PIC16 LC 65	T.M.	25	45	ns	W.1003.

^{*} These parameters are characterized but not tested.

[†] Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 20-7: PARALLEL SLAVE PORT TIMING



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TABLE 20-7: PARALLEL SLAVE PORT REQUIREMENTS

Parameter No.	Sym	Characteristic	paracteristic				Units	Conditions
62	TdtV2wrH	Data in valid before WR↑ or CS↑ (setu	a in valid before WR↑ or CS↑ (setup time)		_	M	ns	M. COM
63*	TwrH2dtl	WR↑ or CS↑ to data–in invalid (hold	20	\ _	41	ns	007.00	
TIW!	N.Inc	time)	PIC16 LC 65	35	W-	-1	ns	TONY.CO.
64	TrdL2dtV	RD↓ and CS↓ to data–out valid	A Jan Co	Mr.	asN	80	ns	·r. CO
65	TrdH2dtl	RD↑ or CS↑ to data–out invalid					ns	N.100

These parameters are characterized but not tested.

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[†] Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not

FIGURE 20-8: SPI MODE TIMING

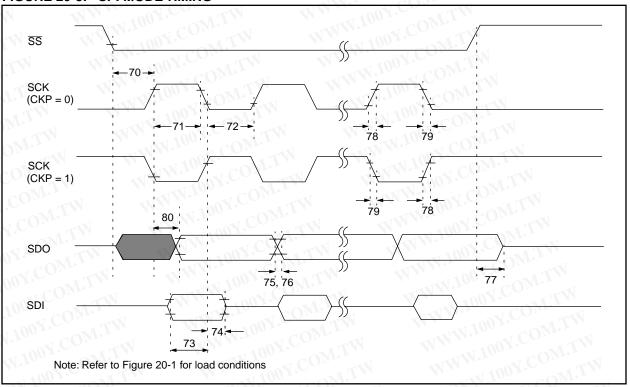
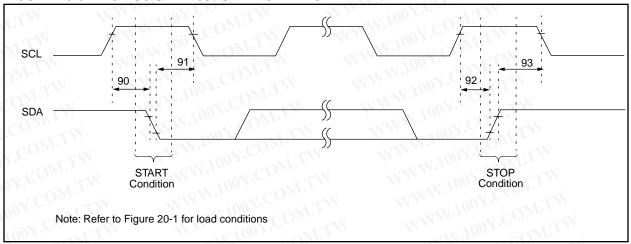


TABLE 20-8: SPI MODE REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Тур†	Max	Units	Conditions
70	TssL2scH, TssL2scL	SS↓ to SCK↓ or SCK↑ input	Tcy	_	MM	ns	M.COM.
71	TscH	SCK input high time (slave mode)	Tcy + 20	N —	_N	ns	OY.Co
72	TscL	SCK input low time (slave mode)	Tcy + 20	cas i		ns	WY.COM
73	TdiV2scH, TdiV2scL	Setup time of SDI data input to SCK edge	50	TW	_	ns	100X.CO
74	TscH2diL, TscL2diL	Hold time of SDI data input to SCK edge	50	T.TN	_	ns	N.100Y.C
75	TdoR	SDO data output rise time	100 7	10	25	ns	W.1001.
76	TdoF	SDO data output fall time	100×1.00	10	25	ns	11001
77	TssH2doZ	SS↑ to SDO output hi-impedance	10	$O^{\overline{M}_{2}}$	50	ns	NW 002
78	TscR	SCK output rise time (master mode)	N.100	10	25	ns	MAIN
79	TscF	SCK output fall time (master mode)	W. 100 r.	10	25	ns	WW.100
80	TscH2doV, TscL2doV	SDO data output valid after SCK edge	M.1007		50	ns	WWW.10

[†] Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 20-9: 12C BUS START/STOP BITS TIMING



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I²C BUS START/STOP BITS REQUIREMENTS **TABLE 20-9:**

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Parameter No.	Sym	Characteristic	M.100 x. CO.	Min	Тур	Max	Units	Conditions	
90	Tsu:sta	START condition	100 kHz mode	4700		_	no	Only relevant for repeated START	
	.00	Setup time	400 kHz mode	600	44	_	ns	condition	
91	THD:STA	START condition	100 kHz mode	4000	147	_	201	After this period the first clock	
	CON	Hold time	400 kHz mode	600	_	1 —	ns	pulse is generated	
92	Tsu:sto	STOP condition	100 kHz mode	4700	7	_			
	CO.	Setup time	400 kHz mode	600	T	W_	ns	WWW TOOY.CO	
93	THD:STO	STOP condition	100 kHz mode	4000	NE.	N.		TIMAN.	
	1007.	Hold time	400 kHz mode	600	A.	1 4	ns	100 x 0V.	

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FIGURE 20-10: I²C BUS DATA TIMING

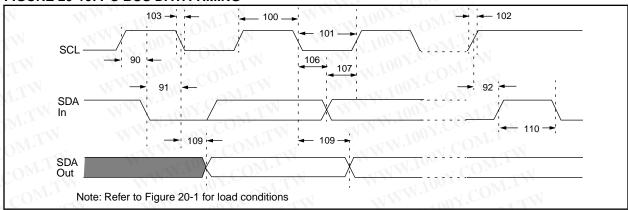


TABLE 20-10: I²C BUS DATA REQUIREMENTS

Parameter No.	Sym	Characteristic	OY.COM.TV	Min	Max	Units	Conditions
100	THIGH	Clock high time	100 kHz mode	4.0	W.	μs	Device must operate at a minimum of 1.5 MHz
100 X.C		N WWW	400 kHz mode	0.6	-	μs	Devce must operate at a minimum of 10 MHz
1.100		TI TIMY	SSP Module	1.5TcY		MM.	OV.CO
101	TLOW	Clock low time	100 kHz mode	4.7	- 1	μs	Device must operate at a minimum of 1.5 MHz
AN .100		W WI	400 kHz mode	1.3	_	μs	Device must operate at a minimum of 10 MHz
MM·IO			SSP Module	1.5TcY	_		TV
102	TR	SDA and SCL rise	100 kHz mode	ONT.	1000	ns	M. ro COM
WW.		time	400 kHz mode	20 + 0.1Cb	300	ns	Cb is specified to be from 10-400 pF
103	10 TF	SDA and SCL fall time	100 kHz mode	COM	300	ns	MAN. TO COM.
WWW		COM.TW	400 kHz mode	20 + 0.1Cb	300	ns	Cb is specified to be from 10-400 pF
90	Tsu:sta	START condition	100 kHz mode	4.7	37	μs	Only relevant for repeated
WW		setup time	400 kHz mode	0.6	(FW	μs	START condition
91	THD:STA	START condition hold	100 kHz mode	4.0	-	μs	After this period the first clock
		time	400 kHz mode	0.6	·	μs	pulse is generated
106	THD:DAT	Data input hold time	100 kHz mode	0	7.7	ns	W 1001.
		COM	400 kHz mode	0	0.9	μs	WWW. COV.C
107	TSU:DAT	Data input setup time	100 kHz mode	250	~() M.	ns	Note 2
		ANDY.CO. TY	400 kHz mode	100	_	ns	11 100%
92	Tsu:sto	STOP condition setup	100 kHz mode	4.7	Cop	μs	WWW
		time	400 kHz mode	0.6	ZO	μs	WW.100
109	TAA	Output valid from	100 kHz mode	100	3500	ns	Note 1
		clock	400 kHz mode	MA	T.C	ns	W WWW.
110	TBUF	Bus free time	100 kHz mode	4.7	V =	μs	Time the bus must be free
		N 1100 Y. CO.	400 kHz mode	1.3	00-	μs	before a new transmission can start
	Cb	Bus capacitive loading	WILL	MA	400	pF	T.T.

Note 1: As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (min. 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

2: A fast-mode (400 kHz) I²C-bus device can be used in a standard-mode (100 kHz) I²C-bus system, but the requirement tsu;DAT ≥ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line TR max.+tsu;DAT = 1000 + 250 = 1250 ns (according to the standard-mode I²C bus specification) before the SCL line is released.

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FIGURE 20-11: USART SYNCHRONOUS TRANSMISSION (MASTER/SLAVE) TIMING

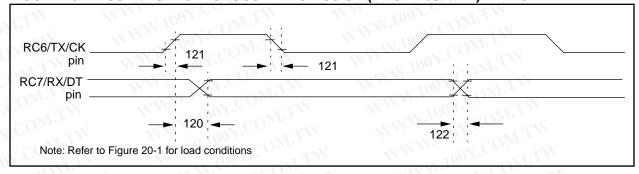


TABLE 20-11: USART SYNCHRONOUS TRANSMISSION REQUIREMENTS

Parameter No.	Sym	Characteristic	M.TW	Min	Typ†	Max	Units	Conditions
120	TckH2dtV	SYNC XMIT (MASTER & SLAVE)	PIC16 C 65	_	TOTAL D	80	ns	- 1
Anny.C		Clock high to data out valid	PIC16 LC 65	_ \	V = 1	100	ns	L.A.
121	Tckrf	Clock out rise time and fall time	PIC16 C 65	_	MAN AL	45	ns	TW
M.100 r.	COM.	(Master Mode)	PIC16 LC 65	_	ATN V	50	ns	
122	Tdtrf	Data out rise time and fall time	PIC16 C 65	_	<u> </u>	45	ns	V. F.
111.	V.COn.	TW WP 100	PIC16 LC 65	\ _	4	50	ns	MIN

^{†:} Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 20-12: USART SYNCHRONOUS RECEIVE (MASTER/SLAVE) TIMING

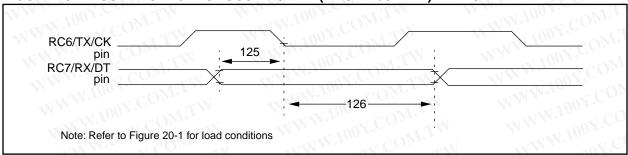


TABLE 20-12: USART SYNCHRONOUS RECEIVE REQUIREMENTS

Parameter No.	Sym	Characteristic	MinC	Тур†	Max	Units	Conditions
125	TdtV2ckL	SYNC RCV (MASTER & SLAVE) Data setup before CK ↓ (DT setup time)	15	OM	AN T	ns	WW.100
126	TckL2dtl	Data hold after CK ↓ (DT hold time)	15	- TV	<u> </u>	ns	. W.M.

^{†:} Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

ELECTRICAL CHARACTERISTICS FOR PIC16C63/65A

Absolute Maximum Ratings (†) Ambient temperature under bias	MAN COMPAN	55°C to +125°C
Storage temperature		65°C to +150°C
Voltage on any pin with respect to Vss (except VDD		
Voltage on VDD with respect to VSS		-0.3V to +7.5V
Voltage on MCLR with respect to Vss (Note 2)	COMPANY COMPANY	0V to +14V
Voltage on RA4 with respect to Vss	WWW. Too COM.	0V to +14V
Total power dissipation (Note 1)		1.0W
Maximum current out of Vss pin	胜特力电子(上海) 86-21-54151736	300 mA
Maximum current into VDD pin	胜特力电子(深圳) 86-755-83298787	250 mA
Input clamp current, IIK (VI < 0 or VI > VDD)	Http://www.100y.com.tw	±20 mA
Output clamp current, loκ (Vo < 0 or Vo > VDD)	Http://www.100y.com.tw	±20 mA
Maximum output current sunk by any I/O pin	o and Co	25 mA
Maximum output current sourced by any I/O pin		
Maximum current sunk by PORTA, PORTB, and PO	ORTE (Note 3) (combined)	200 mA
Maximum current sourced by PORTA, PORTB, and		
Maximum current sunk by PORTC and PORTD (No	te 3) (combined)	200 mA
Maximum current sourced by PORTC and PORTD	(Note 3) (combined)	200 mA
Note 1: Power dissipation is calculated as follow		

Note 2: Voltage spikes below Vss at the MCLR/VPP pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a "low" level to the MCLR/VPP pin rather than pulling this pin directly to Vss.

Note 3: PORTD and PORTE not available on the PIC16C63.

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 21-1: CROSS REFERENCE OF DEVICE SPECS FOR OSCILLATOR CONFIGURATIONS AND FREQUENCIES OF OPERATION (COMMERCIAL DEVICES)

osc	PIC16C63-04 PIC16C65A-04			PIC16LC63-04 PIC16LC65A-04	JW Devices
RC	VDD: 4.0V to 6.0V IDD: 5 mA max. at 5.5V IPD: 16 µA max. at 4V Freq: 4 MHz max.	VDD: 4.5V to 5.5V IDD: 2.7 mA typ. at 5.5V IPD: 1.5 μA typ. at 4V Freq: 4 MHz max.	VDD: 4.5V to 5.5V IDD: 2.7 mA typ. at 5.5V IPD: 1.5 μA typ. at 4V Freq: 4 MHz max.	VDD: 2.5V to 6.0V IDD: 3.8 mA max. at 3V IPD: 5 μA max. at 3V Freq: 4 MHz max.	VDD: 4.0V to 6.0V IDD: 5 mA max. at 5.5V IPD: 16 μA max. at 4V Freq: 4 MHz max.
XT	VDD: 4.0V to 6.0V IDD: 5 mA max. at 5.5V IPD: 16 µA max. at 4V Freq: 4 MHz max.	VDD: 4.5V to 5.5V IDD: 2.7 mA typ. at 5.5V IPD: 1.5 μA typ. at 4V Freq: 4 MHz max.	VDD: 4.5V to 5.5V IDD: 2.7 mA typ. at 5.5V IPD: 1.5 μA typ. at 4V Freq: 4 MHz max.	VDD: 2.5V to 6.0V IDD: 3.8 mA max. at 3V IPD: 5 μA max. at 3V Freq: 4 MHz max.	VDD: 4.0V to 6.0V IDD: 5 mA max. at 5.5V IPD: 16 µA max. at 4V Freq: 4 MHz max.
HS	VDD: 4.5V to 5.5V IDD: 13.5 mA typ. at 5.5V	OOY. COM.TW	VDD: 4.5V to 5.5V IDD: 20 mA max. at 5.5V	Not recommended for use in HS mode	VDD: 4.5V to 5.5V IDD: 20 mA max. at 5.5V
	IPD: 1.5 μA typ. at 4.5V Freq: 4 MHz max.	IPD 1.5 μA typ. at 4.5V Freq: 10 MHz max.	IPD: 1.5 μA typ. at 4.5V Freq: 20 MHz max.	OOY.COM.TW	IPD: 1.5 μA typ. at 4.5V Freq: 20 MHz max.
LP	VDD: 4.0V to 6.0V IDD: 52.5 μA typ. at 32 kHz, 4.0V IPD: 0.9 μA typ. at 4.0V Freq: 200 kHz max.	Not recommended for use in LP mode	Not recommended for use in LP mode	VDD: 2.5V to 6.0V IDD: 48 μA max. at 32 kHz, 3.0V IPD: 5 μA max. at 3.0V Freq: 200 kHz max.	VDD: 2.5V to 6.0V IDD: 48 μA max. at 32 kHz, 3.0V IPD: 5 μA max. at 3.0V Freq: 200 kHz max.

The shaded sections indicate oscillator selections which are tested for functionality, but not for MIN/MAX specifications. It is recommended that the user select the device type that ensures the specifications required.

DC CHARACTERISTICS

Applicable Devices 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

PIC16C63/65A-04 (Commercial, Industrial, Extended) DC Characteristics:

PIC16C63/65A-10 (Commercial, Industrial, Extended)

PIC16C63/65A-20 (Commercial, Industrial, Extended)

Standard Operating Conditions (unless otherwise stated)

Operating temperature -40°C

 \leq TA \leq +125°C for extended,

-40°C ≤ TA ≤ +85°C for industrial and

OM	WWW.I	ov.C	OME		0°0	2	≤ TA ≤ +70°C for commercial
Param No.	Characteristic	Sym	Min	Typ†	Max	Units	Conditions
D001 D001A	Supply Voltage	VDD	4.0 4.5	M.TV	6.0 5.5	V	XT, RC and LP osc configuration HS osc configuration
D002*	RAM Data Retention Voltage (Note 1)	VDR	N.C	1.5	M	V	WWW.100X.COM.TW
D003	VDD start voltage to ensure internal Power-on Reset signal	VPOR	007.C	Vss	TW TTN	V	See section on Power-on Reset for details
D004*	VDD rise rate to ensure internal Power-on Reset signal	SVDD	0.05	N.CC	N.T	V/ms	See section on Power-on Reset for details
D005	Brown-out Reset Voltage	BVDD	3.7	4.0	4.3	V	BODEN configuration bit is enabled
	CONT. TAN	W	3.7	4.0	4.4	V	Extended Range Only
D010	Supply Current (Note 2, 5)	IDD	MAN.	2.7	5	mA	XT, RC, osc config Fosc = 4 MHz, VDD = 5.5V (Note 4)
D013	N.100Y.COM.TW		WW	10	20	mA	HS osc config Fosc = 20 MHz, VDD = 5.5V
D015*	Brown-out Reset Current (Note 6)	Δlbor	WV	350	425	μА	BOR enabled, VDD = 5.0V
D020	Power-down Current	IPD	7//	10.5	42	μΑ	VDD = 4.0V, WDT enabled,-40°C to +85°C
D021	(Note 3, 5)	W	- 4	1.5	16	μΑ	$VDD = 4.0V$, WDT disabled, $-0^{\circ}C$ to $+70^{\circ}C$
D021A D021B	MM.In. COM.	CXN	-	1.5 2.5	19 19	μΑ	$VDD = 4.0V$, WDT disabled, $-40^{\circ}C$ to $+85^{\circ}C$ $VDD = 4.0V$, WDT disabled, $-40^{\circ}C$ to $+125^{\circ}C$
טטע ו ס	M. TM. TOOM:	7	-	2.5	19	μА	= 4.0v, vvD1 disabled,-40°C to +125°C
D023*	Brown-out Reset Current (Note 6)	Δlbor	-	350	425	μА	BOR enabled, VDD = 5.0V

- These parameters are characterized but not tested.
- Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.
- Note 1: This is the limit to which VDD can be lowered without losing RAM data.
 - 2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
 - The test conditions for all IDD measurements in active operation mode are:
 - OSC1 = external square wave, from rail to rail; all I/O pins tristated, pulled to VDD,
 - MCLR = VDD; WDT enabled/disabled as specified.
 - 3: The power down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and Vss.
 - For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kOhm.
 - Timer1 oscillator (when enabled) adds approximately 20 µA to the specification. This value is from characterization and is for design guidance only. This is not tested.
 - The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

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21.2 DC Characteristics: PIC16LC63/65A-04 (Commercial, Industrial)

DC CHA	RACTERISTICS	Standa Operation	-	-		°C ≤	unless otherwise stated) TA ≤ +85°C for industrial and TA ≤ +70°C for commercial
Param No.	Characteristic	Sym	Min	Тур†	Max	Units	Conditions
D001	Supply Voltage	VDD	2.5	-	6.0	٧	LP, XT, RC osc configuration (DC - 4 MHz)
D002*	RAM Data Retention Voltage (Note 1)	VDR	1.17	1.5	-4	V	TOOX.CON.TW
D003	VDD start voltage to ensure internal Power-on Reset signal	VPOR	M.T.MC	Vss	-	W.A.	See section on Power-on Reset for details
D004*	VDD rise rate to ensure internal Power-on Reset signal	SVDD	0.05	TY LTV	-	V/ms	See section on Power-on Reset for details
D005	Brown-out Reset Voltage	BVDD	3.7	4.0	4.3	٧	BODEN configuration bit is enabled
D010	Supply Current (Note 2, 5)	IDD	N.C.	2.0	3.8	mA	XT, RC osc configuration FOSC = 4 MHz, VDD = 3.0V (Note 4)
D010A	COM.TW W	MM'I	007	22.5	48	μA	LP osc configuration Fosc = 32 kHz, VDD = 3.0V, WDT disabled
D015*	Brown-out Reset Current (Note 6)	ΔIBOR	700	350	425	μΑ	BOR enabled, VDD = 5.0V
D020	Power-down Current	IPD	14.5	7.5	30	μΑ	VDD = 3.0V, WDT enabled, -40°C to +85°C
D021	(Note 3, 5)		11-11	0.9	5	μΑ	VDD = 3.0V, WDT disabled, 0°C to +70°C
D021A	OOY.COM.TW	WV	NW.1	0.9	5	μΑ	VDD = 3.0V, WDT disabled, -40°C to +85°C
D023*	Brown-out Reset Current (Note 6)	ΔIBOR	WW	350	425	μΑ	BOR enabled, VDD = 5.0V

- These parameters are characterized but not tested.
- † Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.
- Note 1: This is the limit to which VDD can be lowered without losing RAM data.
 - 2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
 - The test conditions for all IDD measurements in active operation mode are:
 - OSC1 = external square wave, from rail to rail; all I/O pins tristated, pulled to VDD,
 - MCLR = VDD; WDT enabled/disabled as specified.
 - 3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and Vss.
 - 4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kOhm.
 - 5: Timer1 oscillator (when enabled) adds approximately 20 µA to the specification. This value is from characterization and is for design guidance only. This is not tested.
 - 6: The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

PIC16C6X

DC CHARACTERISTICS

Applicable Devices 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

21.3 DC Characteristics: PIC16C63/65A-04 (Commercial, Industrial, Extended)

PIC16C63/65A-10 (Commercial, Industrial, Extended)

PIC16C63/65A-20 (Commercial, Industrial, Extended)

PIC16LC63/65A-04 (Commercial, Industrial)

Standard Operating Conditions (unless otherwise stated)

Operating temperature $-40^{\circ}\text{C} \le \text{TA} \le +125^{\circ}\text{C}$ for extended, $-40^{\circ}\text{C} \le \text{TA} \le +85^{\circ}\text{C}$ for industrial and

 0° C $\leq TA \leq +70^{\circ}$ C for commercial

Operating voltage VDD range as described in DC spec Section 21.1 and

Section 21.2

J CUN	The William Con-	Section			41/1/1	. 00	Y.C.
Param No.	Characteristic	Sym	Min	Typ †	Max	Units	Conditions
~ 1 C	Input Low Voltage	COB	TW		WW	44.,	WY.CO.
	I/O ports	VIL	W. I.			W.1	CONL
D030	with TTL buffer	N.C.	Vss	-	0.15VDD	V	For entire VDD range
D030A	COM.	V.C	Vss	-	0.8V	V	$4.5V \le VDD \le 5.5V$
D031	with Schmitt Trigger buffer	-7 (Vss	- - 181	0.2Vdd	V	· to COM
D032	MCLR, OSC1 (in RC mode)	1001.	Vss	11-	0.2VDD	V	N.100 Y.
D033	OSC1 (in XT, HS and LP)	Voor	Vss		0.3VDD	V	Note1
	Input High Voltage	170	1 CO $_{Mr}$.		N	wV	M. T. COM.
D040	I/O ports	VIH	601		<11/2	N/	16V 2V-2 5 60 N
D040	with TTL buffer	1 100	2.0 0.25VDD	C_{N}	VDD	V	$4.5V \le VDD \le 5.5V$
D040A	COMP.	11.1	+ 0.8V	N 3-	VDD	V	For entire VDD range
	100 1. COM: I.	W.1	10.00	$M_{\rm c}$	-XI		TMM. Inc. COM.
D041	with Schmitt Trigger buffer	N N	0.8VDD	-	VDD	V	For entire VDD range
D042	MCLR	M. M.	0.8VDD	(A)	VDD	V	WWW. 100X.CO
D042A	OSC1 (XT, HS and LP)	TWW	0.7VDD	CO	VDD	V	Note1
D043	OSC1 (in RC mode)	W .	0.9VDD	-	VDD	, V	WWW.100 TOM
D070	PORTB weak pull-up current	IPURB	50	250	400	μΑ	VDD = 5V, VPIN = VSS
-1	Input Leakage Current (Notes 2, 3)	WW	M.	V.(On	V	MM 100X.Co.
D060	I/O ports	lı∟	W. 10	-7	±1\	μΑ	Vss ≤ VPIN ≤ VDD, Pin at hi-
	WWW TOOK TO	1	W 10	01	Mon	L.A.	impedance
D061	MCLR, RA4/T0CKI	1	11 4	001	±5	μΑ	Vss ≤ Vpin ≤ Vdd
D063	OSC1		WW.	102	±5	μΑ	Vss ≤ VPIN ≤ VDD, XT, HS and LP osc configuration
	Output Low Voltage		N ·	101	77.	1	LF osc configuration
D080	I/O ports	VOL	M.M.	. 1 <u>. 1</u> . (0.6	V	IOL = 8.5 mA, VDD = 4.5V,
D000	WWW.To-V.COM	VOL	WW	N	0.00)NA	-40°C to +85°C
D080A	M.100 F. COW.1	as T	- 133	1	0.6	OV.	IOL = 7.0 mA, VDD = 4.5V,
	WW TOOY.	11	Al A	- 1	1007.	Mon	-40°C to +125°C
D083	OSC2/CLKOUT (RC osc config)	W	- 1	NJ.	0.6	V	IOL = 1.6 mA, VDD = 4.5V,
	WW.Inda COM.	- 1		W	N.In.	$^{L}CO_{J}$	-40°C to +85°C
D083A	M. 1007.	TW	- 1		0.6	V	IOL = 1.2 mA, VDD = 4.5V,
	MAN W. CO.	W	4	NV	100	Y.C.	-40°C to +125°C

These parameters are characterized but not tested.

- The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.
- 3: Negative current is defined as current sourced by the pin.

[†] Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C6X be driven with external clock in RC mode.

Standard Operating Conditions (unless otherwise stated)

Operating temperature

-40°C \leq TA \leq +125°C for extended,

-40°C ≤ TA ≤ +85°C for industrial and

0°C

≤ TA ≤ +70°C for commercial Operating voltage VDD range as described in DC spec Section 21.1 and

Section 21.2

Param No.	Characteristic	Sym	Min	Typ †	Max	Units	Conditions
Mil	Output High Voltage	3		4	W.In.	-7 CO	M
D090	I/O ports (Note 3)	Voн	VDD-0.7	N.Y	M.100	V	IOH = -3.0 mA, VDD = 4.5 V, -40 °C to $+85$ °C
D090A	MANN TOOK CO	WIL	VDD-0.7	1	WW.1	V	IOH = -2.5 mA, VDD = 4.5V, -40°C to +125°C
D092	OSC2/CLKOUT (RC osc config)	Σ_{Mr}	VDD-0.7	- 1	MEM.	1001	IOH = -1.3 mA, VDD = 4.5V, -40°C to +85°C
D092A	T.TW WWW.100Y.	co_{M}	VDD-0.7	-	W.W.	V.1V.0	IOH = -1.0 mA, VDD = 4.5V, -40°C to +125°C
D150*	Open-Drain High Voltage	Vod	CITY.	-	14	V	RA4 pin
00 Y.C	Capacitive Loading Specs on Output Pins	I.CO	M.TW		WW	NW.1	OOY.COM.TW
D100	OSC2 pin	Cosc ₂	M.T.W	-	15	pF	In XT, HS and LP modes when external clock is used to drive OSC1.
D101	All I/O pins and OSC2 (in RC mode)	Cio	LIZ	17	50	pF	N 100Y. OM.TW
D102	SCL, SDA in I ² C mode	Cb	COh	77	400	pF	TW.

These parameters are characterized but not tested.

DC CHARACTERISTICS

- † Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.
- Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C6X be driven with external clock in RC mode.
 - The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input volt-

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3: Negative current is defined as current sourced by the pin.

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Applicable Devices 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

21.4 <u>Timing Parameter Symbology</u>

The timing parameter symbols have been created following one of the following formats:

1. TppS2ppS 3. Tcc:st (I²C specifications only)
2. TppS 4. Ts (I²C specifications only)

T Time

Lowercase letters (pp) and their meanings:

osc	OSC1
	110
rd	RD
rw	RD or WR
sc	SCK
SS	SS
t0	TOCKI COMMON COMPON COM
t1	T1CKI
wr	WR
	rd rw sc ss t0 t1

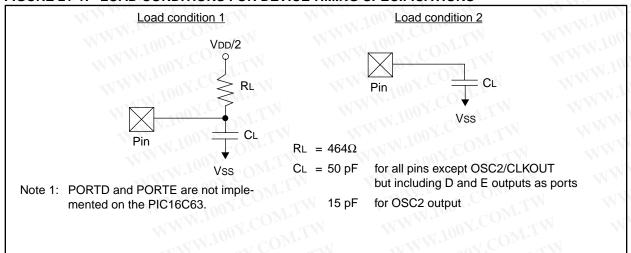
Uppercase letters and their meanings:

S 100	CONTINUE	OW.	I COM.
F 100	Fall	P	Period
H	High	R	Rise
J.W.10	Invalid (Hi-impedance)	(A)	Valid
L WI	Low	ZOM	Hi-impedance
I ² C only		M.COM	
AA	output access	High	High
BUF	Bus free	Low	Low

Tcc:st (I²C specifications only)

CC	31 100x. CM.TW	100 .	ON: I COL
HD	Hold	SU	Setup
ST		V. I	
DAT	DATA input hold	STO	STOP condition
STA	START condition	100	

FIGURE 21-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS



21.5 <u>Timing Diagrams and Specifications</u>

FIGURE 21-2: EXTERNAL CLOCK TIMING

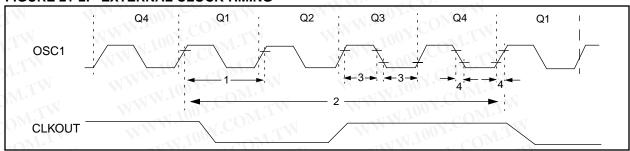


TABLE 21-2: EXTERNAL CLOCK TIMING REQUIREMENTS

Param No.	Sym	Characteristic	Min	Тур†	Max	Units	Conditions
a Co	Fosc	External CLKIN Frequency	DC	W-	4	MHz	XT and RC osc mode
7.		(Note 1)	DC	. √ . .≼T	4	MHz	HS osc mode (-04)
M.C.		MM 100X.	DC	LIN	10	MHz	HS osc mode (-10)
~√ C		WWW.	DC		20	MHz	HS osc mode (-20)
00 τ .		1, 100 -	DC	1. 1 <u> </u>	200	kHz	LP osc mode
NOV.		Oscillator Frequency	DC	V.IIA	4	MHz	RC osc mode
10-		(Note 1)	0.1	-	4	MHz	XT osc mode
1700		V.1.	4	$M_{\overline{r}_{r}}$	20	MHz	HS osc mode
100		MITH WWW TITO	5	ON!T	200	kHz	LP osc mode
1	Tosc	External CLKIN Period	250			ns	XT and RC osc mode
W.10		(Note 1)	250	$C\Theta_{MT}$	<u> </u>	ns	HS osc mode (-04)
-11		WITH WITH	100	-	TA	ns	HS osc mode (-10)
M.		COM WAY	50	I'CA	(P)	ns	HS osc mode (-20)
		COM.	5	47 CO	VI.	μs	LP osc mode
		Oscillator Period	250) y =	MITT	ns	RC osc mode
WW		(Note 1)	250	V I C	10,000	ns	XT osc mode
11		COM.	250	= (250	ns	HS osc mode (-04)
MA		OY. WITH	100	$10\sigma_{T}$	250	ns	HS osc mode (-10)
177		OV.COM W	50	Vin V	250	ns	HS osc mode (-20)
1		COM.	5	700	CONT.	μs	LP osc mode
2	Tcy	Instruction Cycle Time (Note 1)	200	TCY	DC	ns	Tcy = 4/Fosc
3*	TosL,	External Clock in (OSC1) High or	100	- 00	Y.C	ns	XT oscillator
	TosH	Low Time	2.5	Mra	~ √ 0	μs	LP oscillator
		31 100 Y. OM.TW	15	-1XN-19	M 7 CU	ns	HS oscillator
4*	TosR,	External Clock in (OSC1) Rise or	-1	M 47	25	ns	XT oscillator
	TosF	Fall Time		TW I N.	50	ns	LP oscillator
		1, 100 Y. W.T.	_		1015	ns	HS oscillator

^{*} These parameters are characterized but not tested.

Note 1: Instruction cycle period (TCY) equals four times the input oscillator time-base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1/CLKIN pin. When an external clock input is used, the "Max." cycle time limit is "DC" (no clock) for all devices.

[†] Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 21-3: CLKOUT AND I/O TIMING

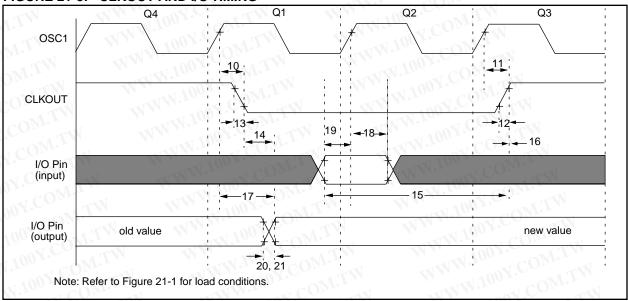


TABLE 21-3: CLKOUT AND I/O TIMING REQUIREMENTS

Parameter No.	Sym	Characteristic	OOX.COM.	Min	Typ†	Max	Units	Conditions
10*	TosH2ckL	OSC1↑ to CLKOUT↓	1007.00	[N-	75	200	ns	Note 1
11*	TosH2ckH	OSC1↑ to CLKOUT↑		TY	75	200	ns	Note 1
12*	TckR	CLKOUT rise time		-31	35	100	ns	Note 1
13*	TckF	CLKOUT fall time	M 1007.	W.T.	35	100	ns	Note 1
14*	TckL2ioV	CLKOUT ↓ to Port out valid	A. TOUN CO	W TW	_	0.5Tcy + 20	ns	Note 1
15*	TioV2ckH	Port in valid before CLKOUT ↑	NW. M. C	Tosc + 200	_	-	ns	Note 1
16*	TckH2iol	Port in hold after CLKOUT ↑	100 ·	0 0	- T		ns	Note 1
17*	TosH2ioV	OSC1↑ (Q1 cycle) to Port out va	llid	T.M.	50	150	ns	007.
18*	TosH2ioI	OSC1↑ (Q2 cycle) to Port input	PIC16 C 63/65A	100	1	-111	ns	100 Y.C
	WW.10	invalid (I/O in hold time)	PIC16 LC 63/65A	200	-TT	- 👊	ns	N.C
19*	TioV2osH	Port input valid to OSC1↑ (I/O in	setup time)	0	77	_	ns	1.100
20*	TioR	Port output rise time	PIC16 C 63/65A	7.4	10	40	ns	4 100 x.
	WWI	TO CONT.	PIC16 LC 63/65A	ON COP	777	80	ns	1007
21*	TioF	Port output fall time	PIC16 C 63/65A	27CO	10	40	ns	Min
	MM.	1100Y. OM.TW	PIC16 LC 63/65A	100 = 1	14.7	80	ns	1111.100
22††*	Tinp	INT pin high or low time	MM	TCY	= (TVI—	ns	110
23††*	Trbp	RB7:RB4 change INT high or lov	w time	Tcy	O.	TV V	ns	MAN

^{*} These parameters are characterized but not tested.

Note 1: Measurements are taken in RC Mode where CLKOUT output is 4 x Tosc.

[†] Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

^{††} These parameters are asynchronous events not related to any internal clock edge.

FIGURE 21-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING

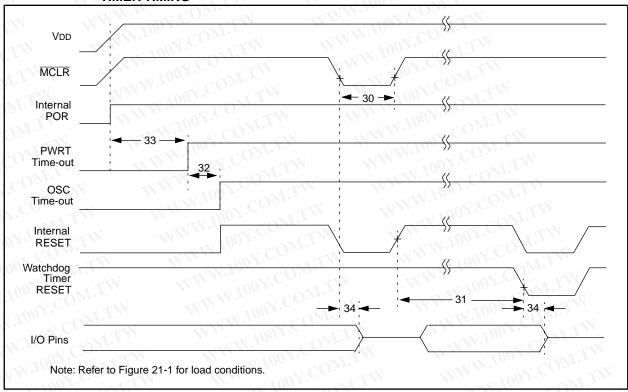


FIGURE 21-5: BROWN-OUT RESETTIMING

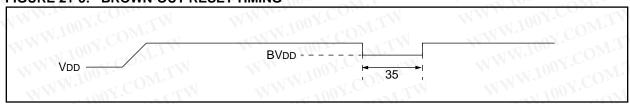


TABLE 21-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER, AND BROWN-OUT RESET REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
30	TmcL	MCLR Pulse Width (low)	2	11000	M.7	μs	VDD = 5V, -40°C to +125°C
31*	Twdt	Watchdog Timer Time-out Period (No Prescaler)	7	18	33	ms	$VDD = 5V, -40^{\circ}C \text{ to } +125^{\circ}C$
32	Tost	Oscillation Start-up Timer Period	<u> </u>	1024 Tosc		$\Gamma_{T,s}$	Tosc = OSC1 period
33*	Tpwrt	Power-up Timer Period	28	72	132	ms	VDD = 5V, -40°C to +125°C
34	Tioz	I/O Hi-impedance from MCLR Low or WDT reset	7/	MN-700	2.1	μs	M MM
35	TBOR	Brown-out Reset Pulse Width	100	VV = 10	OFF	μs	VDD ≤ BVDD (D005)

^{*} These parameters are characterized but not tested.

[†] Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 21-6: TIMERO AND TIMER1 EXTERNAL CLOCK TIMINGS

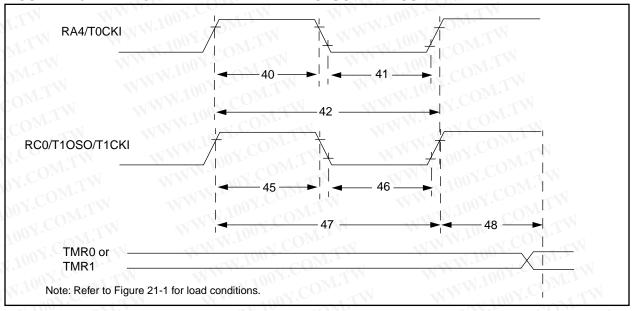


TABLE 21-5: TIMERO AND TIMER1 EXTERNAL CLOCK REQUIREMENTS

Param No.	Sym	Characteristic	MMA	1.100Y.CO	Min	Тур†	Max	Units	Conditions
40*	Tt0H	T0CKI High Pulse V	Vidth	No Prescaler	0.5Tcy + 20	7/	_	ns	Must also meet
	100	ONL		With Prescaler	10	-<	LAN A	ns	parameter 42
41*	TtOL	T0CKI Low Pulse W	/idth	No Prescaler	0.5Tcy + 20	—	-	ns	Must also meet
	Vio.	CONTRACTOR		With Prescaler	10	I —	UT.	ns	parameter 42
42*	Tt0P	T0CKI Period	-1	No Prescaler	Tcy + 40	<u> </u>	37	ns	COR
	M.M.100	Y.COM.TV		With Prescaler	Greater of: 20 or <u>Tcy + 40</u> N	_	N	ns	N = prescale value (2, 4,, 256)
45*	Tt1H	T1CKI High Time	Synchronous, F	Prescaler = 1	0.5Tcy + 20	_		ns	Must also meet
	- TXV.1	on cowi	Synchronous,	PIC16 C 6X	15	- K T	_	ns	parameter 47
	NN	100 Y. COM.	Prescaler = 2,4,8	PIC16LC6X	25	N_	_	ns	VW.100 X. C
	MIN .	1007.0	Asynchronous	PIC16C6X	30	1	_	ns	1001.
		CON	-XX	PIC16LC6X	50		_	ns	WW. OOV.
46*	Tt1L	T1CKI Low Time	Synchronous, F	Prescaler = 1	0.5Tcy + 20	, 1	_	ns	Must also meet
	Wir	M. CO	Synchronous,	PIC16 C 6X	15	T	_	ns	parameter 47
	WY	M.100 - CO	Prescaler = 2,4,8	PIC16LC6X	25	1.2	V -	ns	WWW.I
		W.100	Asynchronous	PIC16C6X	30	ZAF.	- - 1	ns	TWW.I
	W	W. 1001'r	TIN	PIC16LC6X	50	- TA	1.44	ns	10
47*	Tt1P	T1CKI input period	Synchronous	PIC16 C 6X	Greater of: 30 OR TCY + 40 N	COM	TV	ns	N = prescale value (1, 2, 4, 8)
		WWW.100	Y.COM.	PIC16LC6X	Greater of: 50 OR TCY + 40 N	CO	M.T	N	N = prescale value (1, 2, 4, 8)
		WWW	Asynchronous	PIC16 C 6X	60	15	77	ns	1111
		T.WW.I	TOM	PIC16LC6X	100	J-C	$\Omega_{\overline{\Omega}_{r}}$	ns	With
	Ft1	Timer1 oscillator in (oscillator enabled l			DC		200	kHz	
48	TCKEZtmr1	Delay from external	clock edge to tir	mer increment	2Tosc	00.	7Tosc		

These parameters are characterized but not tested.

[†] Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 21-7: CAPTURE/COMPARE/PWM TIMINGS (CCP1 AND CCP2)

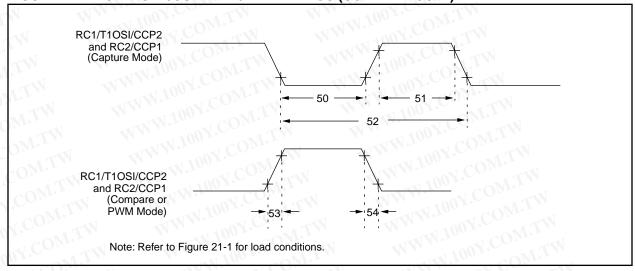


TABLE 21-6: CAPTURE/COMPARE/PWM REQUIREMENTS (CCP1 AND CCP2)

Parameter No.	Sym	Characteristic	WW.1007	COMIL	Min	Тур†	Max	Units	Conditions			
50*	TccL	CCP1 and CCP2	No Prescaler	V.COM	0.5Tcy + 20	May.	<u></u> 0	ns	WTY			
	-ON	CON	COM	TOM	input low time	With Prescaler	PIC16 C 63/65A	10	()	1.50	ns	OM.
		ATW	W 10	PIC16 LC 63/65A	20	-	N-10	ns	OM			
51*	TccH	CCP1 and CCP2	No Prescaler	T.Mo	0.5Tcy + 20	MT.	-x X -1	ns	COMITY			
	V.CC	input high time	With Prescaler	PIC16 C 63/65A	10	ALV.		ns	WILLE			
	- T C	OM.	WWW.	PIC16 LC 63/65A	20	-N		ns	V.COM			
52*	TccP	CCP1 and CCP2 in	nput period	1.100X'CON	3Tcy + 40 N	_	W.	ns	N = prescale value (1,4, or 16)			
53*	TccR	CCP1 and CCP2 of	output rise time	PIC16 C 63/65A	T Y I	10	25	ns	007.Co			
	700	COM		PIC16 LC 63/65A)Mr. =	25	45	ns	CON.			
54*	TccF	CCP1 and CCP2 of	output fall time	PIC16 C 63/65A	OWT.	10	25	ns	Jan COM			
	10	OY.COMITY		PIC16 LC 63/65A	ON FILM	25	45	ns	17001.			

^{*} These parameters are characterized but not tested.

[†] Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 21-8: PARALLEL SLAVE PORT TIMING (PIC16C65A)

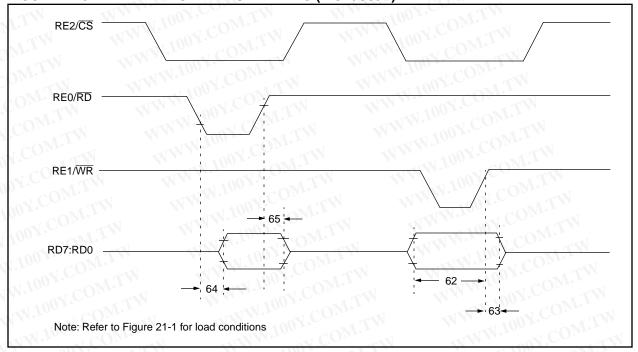


TABLE 21-7: PARALLEL SLAVE PORT REQUIREMENTS (PIC16C65A)

Parameter No.	Sym	Characteristic	107.COM.T	Min	Typ†	Max	Units	Conditions
62*	TdtV2wrH	Data in valid before WR↑ or CS↑ (set	up time)	20	_	N -	ns	MON.
WWW	W.100Y.	CONTA MAN		25	_	W.W	ns	Extended Range Only
63*	TwrH2dtl	WR↑ or CS↑ to data–in invalid (hold	PIC16 C 65A	20	1 —	=	ns	COL
	100	time)	PIC16 LC 65A	35	_		ns	100 5
64	TrdL2dtV	RD↓ and CS↓ to data–out valid	1007.0	THE	W_	80	ns	1007
	WW.	OOY.COM.TW W				90	ns	Extended Range Only
65*	TrdH2dtl	RD↑ or CS↑ to data–out invalid	1007	10	<u>-</u>	30	ns	W.100

^{*} These parameters are characterized but not tested.

[†] Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 21-9: SPI MODE TIMING

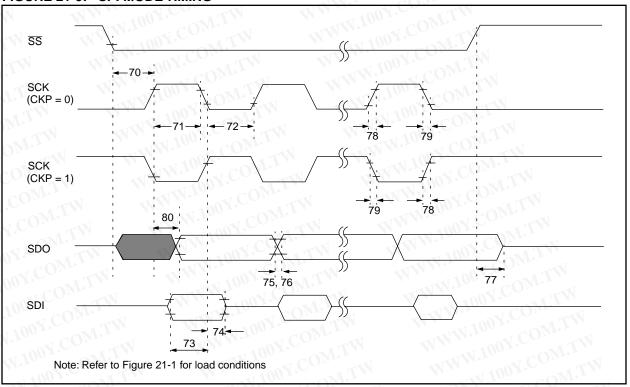


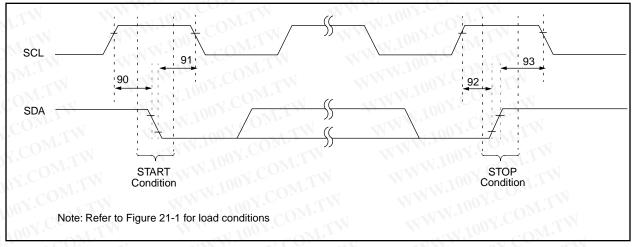
TABLE 21-8: SPI MODE REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Тур†	Max	Units	Conditions
70*	TssL2scH, TssL2scL	SS↓ to SCK↓ or SCK↑ input	Tcy	_	T I	ns	M.Com.
71*	TscH	SCK input high time (slave mode)	Tcy + 20	W		ns	07.0
72*	TscL	SCK input low time (slave mode)	Tcy + 20	-W-	-4	ns	W.Co.
73*	TdiV2scH, TdiV2scL	Setup time of SDI data input to SCK edge	50	TW	_	ns	100 Y.CO
74*	TscH2diL, TscL2diL	Hold time of SDI data input to SCK edge	50	T.EX	_	ns	N.100X.C
75*	TdoR	SDO data output rise time	1007.	10	25	ns	W.100 1.
76*	TdoF	SDO data output fall time	1002	10	25	ns	1007
77*	TssH2doZ	SS↑ to SDO output hi-impedance	10	<u> </u>	50	ns	1005
78*	TscR	SCK output rise time (master mode)	N.I	10	25	ns	WWW
79*	TscF	SCK output fall time (master mode)	W.700 F	10	25	ns	M.In.
80*	TscH2doV, TscL2doV	SDO data output valid after SCK edge	M. 100	V.COD	50	ns	MMM.10

^{*} These parameters are characterized but not tested.

[†] Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 21-10: I²C BUS START/STOP BITS TIMING



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TABLE 21-9: I²C BUS START/STOP BITS REQUIREMENTS

Parameter No.	Sym	Characteristic	M.100 r.Co	Min	Тур	Max	Units	Conditions	
90*	Tsu:sta	START condition	100 kHz mode	4700		_	no	Only relevant for repeated START condition	
	Y. C. C.	Setup time	400 kHz mode	600	44	_	ns		
91*	THD:STA	START condition	100 kHz mode	4000	147	_	200	After this period the first clock	
	COM	Hold time	400 kHz mode	600	_	_	ns	pulse is generated	
92*	Tsu:sto	STOP condition	100 kHz mode	4700	7.7	_		WWW.100Y.COM.	
	CO.	Setup time	400 kHz mode	600	7	W_	ns		
93	THD:STO	STOP condition	100 kHz mode	4000	NF.	- N		MAM. TOOX.CO.	
	- 100 Y.	Hold time	400 kHz mode	600	A.		ns		

These parameters are characterized but not tested.

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FIGURE 21-11: I²C BUS DATA TIMING

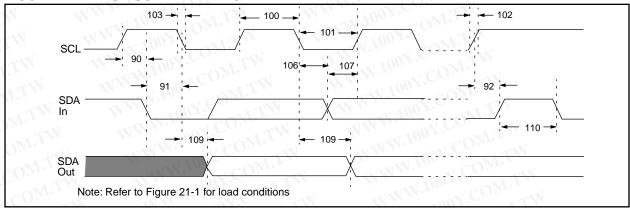


TABLE 21-10: I²C BUS DATA REQUIREMENTS

Parameter No.	Sym	Characteristic	OY.COM.TY	Min	Max	Units	Conditions	
100*	THIGH	Clock high time	100 kHz mode	4.0	WAY.	μs	Device must operate at a minimum of 1.5 MHz	
100X.C		N N N	400 kHz mode	0.6	1/1	μs	Device must operate at a minimum of 10 MHz	
1007.		1	SSP Module	1.5TcY		WW.	COMP	
101*	TLOW	Clock low time	100 kHz mode	4.7	-11	μs	Device must operate at a minimum of 1.5 MHz	
VW.1007		ILM MA	400 kHz mode	1.3	_	μs	Device must operate at a minimum of 10 MHz	
100		1.7.	SSP Module	1.5TcY	_	-43	N.IV. CONT.	
102*	2* TR	2* TR	SDA and SCL rise	100 kHz mode	TIM	1000	ns	11001.
MM'I	time		400 kHz mode	20 + 0.1Cb	300	ns	Cb is specified to be from 10-400 pF	
103*	TF	SDA and SCL fall time	100 kHz mode	V.COE	300	ns	W. CON.	
MAM		OM.I.V	400 kHz mode	20 + 0.1Cb	300	ns	Cb is specified to be from 10-400 pF	
90*	Tsu:sta	START condition	100 kHz mode	4.7	-31	μs	Only relevant for repeated	
MAN		setup time	400 kHz mode	0.6	17.7	μs	START condition	
91*	THD:STA		100 kHz mode	4.0	. 41	μs	After this period the first clock	
		time	400 kHz mode	0.6	17.2	μs	pulse is generated	
106*	THD:DAT	Data input hold time	100 kHz mode	0		ns	100 2	
		COM	400 kHz mode	0	0.9	μs	MAN W. OVY.CO	
107*	TSU:DAT	Data input setup time	100 kHz mode	250	$O_{\overline{A}^{*}}$,	ns	Note 2	
4	MMM	ON.CO. TW	400 kHz mode	100		ns	M.M. 100X.C	
92*	Tsu:sto	STOP condition setup	100 kHz mode	4.7	$\sim G_{Mr}$	μs	TIWW.	
	All Marie	time	400 kHz mode	0.6		μs	W . 100 E	
109*	TAA	Output valid from	100 kHz mode		3500	ns	Note 1	
	All .	clock	400 kHz mode	ANI HOUSE	_ _	ns	TINN. 10°	
110*	TBUF	Bus free time	100 kHz mode	4.7	1-	μs	Time the bus must be free	
	WW	MAN'ION'COM	400 kHz mode	1.3	O.Y.C.	μs	before a new transmission can start	
	Cb	Bus capacitive loading	- TXX	TATAL TATAL	400	pF		

^{*} These parameters are characterized but not tested.

- Note 1: As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (min. 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.
 - 2: A fast-mode (400 kHz) I²C-bus device can be used in a standard-mode (100 kHz) I²C-bus system, but the requirement Tsu:DAT ≥ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line TR max.+tsu;DAT = 1000 + 250 = 1250 ns (according to the standard-mode I²C bus specification) before the SCL line is released.

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FIGURE 21-12: USART SYNCHRONOUS TRANSMISSION (MASTER/SLAVE) TIMING

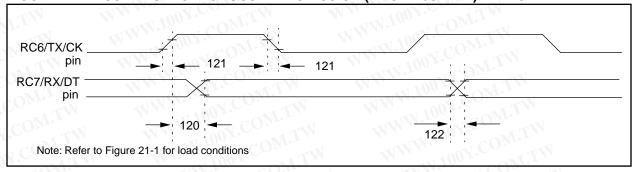


TABLE 21-11: USART SYNCHRONOUS TRANSMISSION REQUIREMENTS

Parameter No.	Sym	Characteristic	ic CONTA		Тур†	Max	Units	Conditions
120*	TckH2dtV	SYNC XMIT (MASTER & SLAVE)	PIC16 C 63/65A	=	1/1/1	80	ns	
	WILL	Clock high to data out valid	PIC16 LC 63/65A	74	L- 	100	ns	1.4
121*	Tckrf	Clock out rise time and fall time	PIC16 C 63/65A	-11	W-	45	ns	TW
	(Master Mode)	(Master Mode)	PIC16 LC 63/65A		NAN	50	Cns	TW
122*	Tdtrf	Data out rise time and fall time	PIC16 C 63/65A	_		45	ns	M
	Co	IM MM 100X	PIC16 LC 63/65A	_	WT.	50	ns	M.IM

- * These parameters are characterized but not tested.
- †: Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 21-13: USART SYNCHRONOUS RECEIVE (MASTER/SLAVE) TIMING

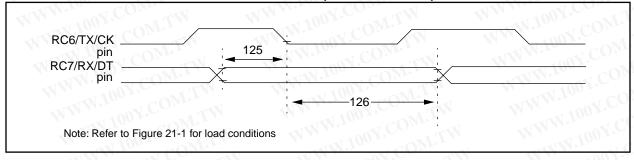


TABLE 21-12: USART SYNCHRONOUS RECEIVE REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Тур†	Max	Units	Conditions
125*	TdtV2ckL	SYNC RCV (MASTER & SLAVE) Data setup before CK ↓ (DT setup time)	15	057 O57	TW	ns	WW.10
126*	TckL2dtl	Data hold after CK ↓ (DT hold time)	15	<u> </u>	174	ns	MAA.

- * These parameters are characterized but not tested.
- †: Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

ELECTRICAL CHARACTERISTICS FOR PIC16CR63/R65 22.0

Absolute Maximum Ratings (†) Ambient temperature under bias....-.-55°C to +125°C Storage temperature-65°C to +150°C Voltage on any pin with respect to Vss (except VDD, MCLR, and RA4)-0.3V to (VDD + 0.3V) Voltage on VDD with respect to Vss-0.3V to +7.5V Input clamp current, lik (Vi < 0 or Vi > VDD) Output clamp current, lok (Vo < 0 or Vo > VDD)..... Maximum output current sunk by any I/O pin...... Maximum output current sourced by any I/O pin Maximum current sunk by PORTA, PORTB, and PORTE (Note 3) (combined)...... Maximum current sourced by PORTA, PORTB, and PORTE (Note 3) (combined) 5. Maximum current sunk by PORTC and PORTD (Note 3) (combined) Maximum current sourced by PORTC and PORTD (Note 3) (combined)... Note 1: Power dissipation is calculated as follows: Pdis = VDD χ-{IDD - Σ(IDN) + Σ (VDD-VOH) x IOH) + Σ(VOI x IOL)

Note 2: Voltage spikes below Vss at the MCLR/VPP pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a flow" level to the MCLR/VPP pin rather than pulling this pin directly to Vss.

Note 3: PORTD and PORTE not available on the P(C16CR63)

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

CROSS REFERENCE OF DEVICE SPECS FOR OSCILLATOR CONFIGURATIONS **TABLE 22-1:** AND FREQUENCIES OF OPERATION (COMMERCIAL DEVICES)

osc	PIC16CR63-04 PIC16CR65-04	PIC16CR63-10 PIC16CR65-10	PIC16CR63-20 PIC16CR65-20	PIC16LCR63-04 PIC16LCR65-04	JW Devices	
RC	VDD: 4.0V to 5.5V IDD: 5 mA max_at 5.5V IPD: 16 μA max_at 4V Freq: 4 MHz max)	VDD: 4.5V to 5.5V IDD: 2.7 m/k typ. at 5.5V IRD: 1.5 µA typ. at 4V Fren; 4 MHz max.	VDD: 4.5V to 5.5V IDD: 2.7 mA typ. at 5.5V IPD: 1.5 μA typ. at 4V Freq: 4 MHz max.	VDD: 3.0V to 5.5V IDD: 3.8 mA max. at 3V IPD: 5 μA max. at 3V Freq: 4 MHz max.	VDD: 4.0V to 5.5V IDD: 5 mA max. at 5.5V IPD: 16 μA max. at 4V Freq: 4 MHz max.	
XT	VDD: 4.0V to \$.5V IDD: 5 mA max. at 5.5V IPD: 16 µA max. at 4V Freq: 4 MHz max.	Vob: 4.5V to 5.5V IDD: 2.7 mA typ. at 5.5V IPD: 1.5 μA typ. at 4V Freq: 4 MHz max.	VDD: 4.5V to 5.5V IDD: 2.7 mA typ. at 5.5V IPD: 1.5 μA typ. at 4V Freq: 4 MHz max.	VDD: 3.0V to 5.5V IDD: 3.8 mA max. at 3V IPD: 5 μA max. at 3V Freq: 4 MHz max.	VDD: 4.0V to 5.5V IDD: 5 mA max. at 5.5V IPD: 16 μA max. at 4V Freq: 4 MHz max.	
HS	VDD: 4.5V to 5.5V IDD: 13.5 mA typ. at 5.5V	OOY. COM.TW	VDD: 4.5V to 5.5V IDD: 20 mA max. at 5.5V	Not recommended for use in HS mode	VDD: 4.5V to 5.5V IDD: 20 mA max. at 5.5V	
	IPD: 1.5 μA typ. at 4.5V Freq: 4 MHz max.	IPD 1.5 μA typ. at 4.5V Freq: 10 MHz max.	IPD: 1.5 μA typ. at 4.5V Freq: 20 MHz max.	On r. COW: I A	IPD: 1.5 μA typ. at 4.5V Freq: 20 MHz max.	
LP			Not recommended for use in LP mode	VDD: 3.0V to 5.5V IDD: 48 μA max. at 32 kHz, 3.0V IPD: 5 μA max. at 3.0V Freq: 200 kHz max.	VDD: 3.0V to 5.5V IDD: 48 μA max. at 32 kHz, 3.0V IPD: 5 μA max. at 3.0V Freq: 200 kHz max.	

The shaded sections indicate oscillator selections which are tested for functionality, but not for MIN/MAX specifications. It is recommended that the user select the device type that ensures the specifications required.

22.1 DC Characteristics: PIC16CR63/R65-04 (Commercial, Industrial)

PIC16CR63/R65-10 (Commercial, Industrial)

PIC16CR63/R65-20 (Commercial, Industrial)

DC CH		Standa Operatir		_		°C ≤	unless otherwise stated) ≤ TA ≤ +85°C for industrial and ≤ TA ≤ +70°C for commercial
Param No.	Characteristic	Sym	Min	Тур†	Max	Units	Conditions
D001 D001A	Supply Voltage	VDD	4.0 4.5	T.	5.5 5.5	V	XT, RC and LP osc configuration HS osc configuration
D002*	RAM Data Retention Voltage (Note 1)	VDR	Y.CO	1.5	N-	V	
D003	VDD start voltage to ensure internal Power-on Reset signal	VPOR	00X.C	Vss	T.M.	V	See section on Power-øn Reset for details
D004*	VDD rise rate to ensure internal Power-on Reset signal	SVDD	0.05		M.T	V/ms	See section on Power-on Reset for details
D005	Brown-out Reset Voltage	Bvdd	3.7	4.0	4.3	V	BODEN configuration bit is enabled
D010	Supply Current (Note 2, 5)	IDD	W.19	2.7	5	mA~	XI, RC, osc config Fosc = 4 MHz, VDD = 5.5V (Note 4)
D013	100Y.COM.TW	N	MA.	10	20	mA	HS osc config Fosc = 20 MHz, VDD = 5.5V
D015*	Brown-out Reset Current (Note 6)	Δ lbor	W-W	350	425	μA	BOR enabled, VDD = 5.0V
D020 D021 D021A	Power-down Current (Note 3, 5)	IPD	-	10.5 1.5 1.5	18 19	μΑ μΑ μΑ	VDD = 4.0V, WDT enabled,-40°C to +85°C VDD = 4.0V, WDT disabled,-0°C to +70°C VDD = 4.0V, WDT disabled,-40°C to +85°C
D023*	Brown-out Reset Current (Note 6)	ΔIBOR		350	425	μА	BOR enabled, VDD = 5.0V

- These parameters are characterized but not tested.
- † Data in "Typ" column is at 6V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.
- Note 1: This is the Jimit to which WDD can be lowered without losing RAM data.
 - 2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
 - The test conditions for all IDD measurements in active operation mode are:
 - OSC1/= external square wave, from rail to rail; all I/O pins tristated, pulled to VDD,
 - MCLR = VDD; WDT enabled/disabled as specified.
 - 3: The power down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and Vss.
 - 4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kOhm.
 - 5: Timer1 oscillator (when enabled) adds approximately 20 μA to the specification. This value is from characterization and is for design guidance only. This is not tested.
 - 6: The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

22.2 DC Characteristics: PIC16LCR63/R65-04 (Commercial, Industrial)

DC CHA	RACTERISTICS	Standa Operatir	•	-		°C ≤	Inless otherwise stated) TA ≤ +85°C for industrial and TA ≤ +70°C for commercial		
Param No.	Characteristic	Sym	Min	Тур†	Max	1241 AA	Conditions		
D001	Supply Voltage	VDD	3.0	-	5.5	V	LP, XT, RC osc configuration (DC - 4 MHz)		
D002*	RAM Data Retention Voltage (Note 1)	VDR	1.17	1.5	-4	V	100X.CONTTN		
D003	VDD start voltage to ensure internal Power-on Reset signal	VPOR	M.T.MC	Vss	-	W.A.	See section on Power-on Reset for details		
D004*	VDD rise rate to ensure internal Power-on Reset signal	SVDD	0.05	TY LTW	-	V/ms	See section on Pewer on Reset for details		
D005	Brown-out Reset Voltage	BVDD	3.7	4.0	4.3	V	BODEN configuration bit is enabled		
D010	Supply Current (Note 2, 5)	IDD	N.CC	2.0	3.8	mA	XT RC ose configuration Fosc = 4 MHz, VDD = 3.0V (Note 4)		
D010A	COM.TW W	NW.	001	22.5	48	μΑ	LP osc configuration Fosc = \$2 kHz, VDD = 3.0V, WDT disabled		
D015*	Brown-out Reset Current (Note 6)	Δlbor	$\frac{100}{100}$	350	425	μA	BOR enabled, VDD = 5.0V		
D020 D021 D021A	Power-down Current (Note 3, 5)	IPD	-	7.5 0.9 0.9	30 5 5	μΑ μΑ μΑ	VDD = 3.0V, WDT enabled, -40°C to +85°C VDD = 3.0V, WDT disabled, 0°C to +70°C VDD = 3.0V, WDT disabled, -40°C to +85°C		
D023*	Brown-out Reset Current (Note 6)	ΔIBOR	-	350	4 25	μА	BOR enabled, VDD = 5.0V		

- * These parameters are characterized but not tested.
- † Data in "Typ" column is at 50,25°C unless otherwise stated. These parameters are for design guidance only and are not tested.
- Note 1: This is the limit to which VDD can be lowered without losing RAM data.
 - 2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
 - The test conditions for all lpb measurements in active operation mode are:
 - OSC1 = external square wave, from rail to rail; all I/O pins tristated, pulled to VDD,
 - MCLR = VDD; WDT enabled/disabled as specified.
 - 3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and Vss.
 - 4 For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kOhm.
 - 5. Timer1 oscillator (when enabled) adds approximately 20 μA to the specification. This value is from characterization and is for design guidance only. This is not tested.
 - 6: The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

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22.3 DC Characteristics: PIC16CR63/R

PIC16CR63/R65-04 (Commercial, Industrial) PIC16CR63/R65-10 (Commercial, Industrial) PIC16CR63/R65-20 (Commercial, Industrial) PIC16LCR63/R65-04 (Commercial, Industrial)

DC CHARACTERISTICS		Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq \text{TA} \leq +85^{\circ}\text{C}$ for industrial and $0^{\circ}\text{C} \leq \text{TA} \leq +70^{\circ}\text{C}$ for commercial								
COM	IRACTERISTICS	Operating voltage VDD range as described in DC spec Section 22.1 an Section 22.2								
Param No.	Characteristic	Sym	Min	Typ †	Max	Units	Conditions			
M.C.	Input Low Voltage		TW		M.	x1 10	D. OM.			
	I/O ports	VIL	W		WW	N	CV.CV			
D030	with TTL buffer	- CO	Vss	-	0.15VDD	V	For entire VpD range			
D030A	WW.	N.C.	Vss	-	V8.0	V	4.5V ≤ VDØ ≤ 5.5V			
D031	with Schmitt Trigger buffer	J.C	Vss	(-	0.2VDD	V				
D032	MCLR, OSC1 (in RC mode)	00 -	Vss	· -	0.2VDD	X				
D033	OSC1 (in XT, HS and LP)	100 X.	Vss	W	0.3VDD	VY	Note1			
M.In	Input High Voltage		COM	W	^	M/V				
	I/O ports	VIH	COM	· -]			COM.			
D040	with TTL buffer	100	2.0	-	VDD	V,	4.5V ≤ VDD ≤ 5.5V			
D040A	A COM.	W - 2	0.25VDD	- {	(VDD	NA	For entire VDD range			
	OU I. COM.IV	W.10	+ 0.8V			/	MM.Ing COM.			
D041	with Schmitt Trigger buffer	WW.1	0,800	7	VDD	V	For entire VDD range			
D042	MCLR	- 1	0.870	\-\	VDD	V	W. T. TOWN COM.			
D042A	OSC1 (XT, HS and LP)		0.7Vpd	$\langle \cdot \rangle$	VDD	V	Note1			
D043	OSC1 (in RC mode)		0.9VDQ	1-1	VDD	V	M.M. To O.Y. COM.			
D070	PORTB weak pull-up current	(PURB	50	250	400	μA	VDD = 5V, VPIN = VSS			
W	Input Leakage Current (Notes 2, 3)	1			117	•	VIV 311001.			
D060	I/O ports	lı.	\ \-_\	Y - .(±1	μΑ	Vss ≤ VPIN ≤ VDD, Pin at himpedance			
D061	MCLR, RA4/T0CKI		W	V-0	±5	μΑ	Vss ≤ VPIN ≤ VDD			
D063	OSC1	\bigvee	MAN.T.	, ~ ⊲	±5	μA	Vss ≤ VPIN ≤ VDD, XT, HS and			
				700	MOD	1	LP osc configuration			
	Output Low Voltage		MA.	10	DA .C.	TY	M., 100x.			
D080	I/O ports	Vol	WWW	-	0.6	V	IOL = 8.5 mA, VDD = 4.5V,			
			- XXIV	N.1	JU - C (M·	-40°C to +85°C			
D083	OSC2/CLKOUT (RC osc config)		At M	v.	0.6	OM.	IOL = 1.6 mA, VDD = 4.5V, -40°C to +85°C			
	Output High Voltage		44.	T VI	700 .	MOS	. T. M. TO			
D090 <	1/O ports (Note 3)	Vон	VDD-0.7	''-''	N.100Y.	CO)	IOH = -3.0 mA, VDD = 4.5 V, -40 °C to $+85$ °C			
D092	OSC2/CLKOUT (RC osc config)	TW	VDD-0.7		W.100	V	IOH = -1.3 mA, VDD = 4.5V, -40°C to +85°C			
D150*	Open-Drain High Voltage	Vod	-	-	14	V	RA4 pin			

- * These parameters are characterized but not tested.
- † Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.
- Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C6X be driven with external clock in RC mode.
 - 2: The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.
 - 3: Negative current is defined as current sourced by the pin.

DC CHARACTERISTICS

Standard Operating Conditions (unless otherwise stated)

Operating temperature -40°C ≤ TA ≤ +85°C for industrial and

0°C ≤ TA ≤ +70°C for commercial

Operating voltage VDD range as described in DC spec Section 22.1 and Section 22.2

Param No.	Characteristic	Sym	Min	Typ †	Max	Units	Conditions
MT.W	Capacitive Loading Specs on Output Pins	TW	1		W.100	, CO	M.TW
D100	OSC2 pin	Cosc ₂	-	W.V	15		In XT, HS and LA modes when external clock is used to drive OSC1.
D101	All I/O pins and OSC2 (in RC mode)	Cio	N -	-11	50	pF	
D102	SCL, SDA in I ² C mode	Cb	- N	-	400	pF	

These parameters are characterized but not tested.

Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only

WWW.100Y Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C6X be driven with external clock in RC mode.

The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input volt-

Negative current is defined as current sourced by the pin.

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PIC16C6X

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22.4 <u>Timing Parameter Symbology</u>

The timing parameter symbols have been created following one of the following formats:

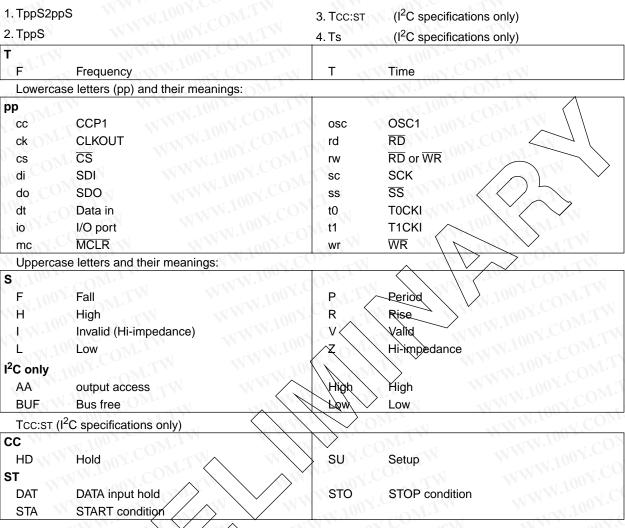
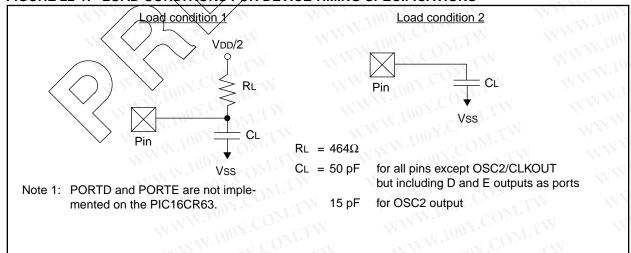


FIGURE 22-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS



22.5 **Timing Diagrams and Specifications**

FIGURE 22-2: EXTERNAL CLOCK TIMING

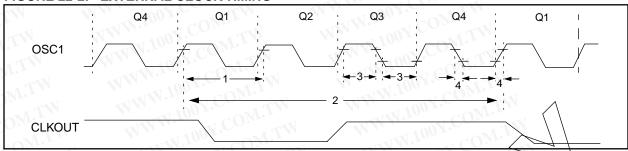


TABLE 22-2: EXTERNAL CLOCK TIMING REQUIREMENTS

Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
of CO	Fosc	External CLKIN Frequency	DC	- N	4	MHz	XT and RC osc mode
1.		(Note 1)	DC	- \\ -	4	MHz	HS osc mode (-04)
N.C.		M MM 100X.C	DC		10	MAZ	HS osc mode (-10)
- < T C		WWW.I	DC		20	MHZ	HS osc mode (-20)
00x.		11, 100 1.	DC	7.7	200	kHz	LP osc mode
MON.		Oscillator Frequency	DC		4	MHZ	RC osc mode
Too		(Note 1)	0.1	_<	4	MHz	XT osc mode
$^{1.700}$		W.T. 1. M. 100	4	/ \	20	MHz	HS osc mode
100		TIN WWW.	5_	/-/	200	kHz	LP osc mode
1	Tosc	External CLKIN Period	250			ns	XT and RC osc mode
JW.10		(Note 1)	250	+1	<u> </u>	ns	HS osc mode (-04)
1			100/	1/-/	7 7	ns	HS osc mode (-10)
WW.		COMPANY TO THE TOTAL OF THE TOT	50		(P)	ns	HS osc mode (-20)
W		COMPA	5	> -0	VI. =	μs	LP osc mode
MM.		Oscillator Period	250	<u> </u>	$M^{\frac{1}{2}}$	ns	RC osc mode
WW		(Note 1)	250	W.	10,000	ns	XT osc mode
W .		COM	250		250	ns	HS osc mode (-04)
1/1/1			100	$I_{0\overline{\Omega_{1}}}$.	250	ns	HS osc mode (-10)
			50	√m¥.	250	ns	HS osc mode (-20)
1			5	1.10	$C_{\Theta_{Mr}}$	μs	LP osc mode
2	TCY	Instruction Cycle Time (Note 1)	200	TCY	DC	ns	Tcy = 4/Fosc
3*	TosL,	External Clock in (OSC1) High or	100	700	1.00	ns	XT oscillator
	TosH	Low Time	2.5	11/1-	~ _ €0	μs	LP oscillator
	Mar.	$\langle \rangle$	15	-1XN-1	N 7-	ns	HS oscillator
4*	TosR,	External Clock in (OSC1) Rise or	-1	W -	25	ns	XT oscillator
	_TosF	Fall Time			50	ns	LP oscillator
	//	, × 100 x.	_	N	15	ns	HS oscillator

These parameters are characterized but not tested.

Note 1: Instruction cycle period (Tcy) equals four times the input oscillator time-base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1/CLKIN pin. When an external clock input is used, the "Max." cycle time limit is "DC" (no clock) for all devices.

Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not † tested,

FIGURE 22-3: CLKOUT AND I/O TIMING

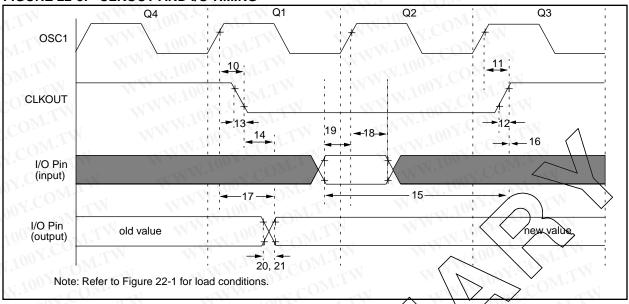


TABLE 22-3: CLKOUT AND I/O TIMING REQUIREMENTS

Param No.	Sym	Characteristic	100 ³ ·CO _N	Min	Typt	Max	Units	Conditions
10*	TosH2ckL	OSC1↑ to CLKOUT↓	1007.0	///	75	200	ns	Note 1
11*	TosH2ckH	OSC1↑ to CLKOUT↑			75	200	ns	Note 1
12*	TckR	CLKOUT rise time		\rightarrow	35	100	ns	Note 1
13*	TckF	CLKOUT fall time		\ _	35	100	ns	Note 1
14*	TckL2ioV	CLKOUT ↓ to Port out valid	11/11/	1 4 N	_	0.5Tcy + 20	ns	Note 1
15*	TioV2ckH	Port in valid before CLKOUT		Tosc + 200	_	#1111	ns	Note 1
16*	TckH2iol	Port in hold after CLKOUT ↑		0 0	. T	= 111	ns	Note 1
17*	TosH2ioV	OSC1↑ (Q1 cycle) tø Rort out va	lid \		50	150	ns	00 1.
18*	TosH2iol	OSC1↑ (Q2 cycle) to Port input	P1016CR63/R65	100	VI-	-41	ns	1001
		invalid (I/O in Kold time)	PIC16LCR63/R65	200		- 📉	ns	OV.C
19*	TioV2osH	Port input valid to OSC11 (I/Q in	setup time)	0		_ `	ns	1.700
20*	TioR	Port output rise time	PIC16CR63/R65	17	10	40	ns	M 100 X.
	WIN		PIC16 LCR 63/R65	W. CO.	777	80	ns	1007
21*	TioF	Port output fall time	PIC16CR63/R65	√ , CO	10	40	ns	111.70
			PIC16LCR63/R65	100 F.	M.	80	ns	M.100
22††*	Tinp	INT pin high or low time	MM	Tcy	<u> </u>	IN-	ns	10
23††*	Trbp	RB7:RB3 change INT high or lov	v time	TCY	CE.	TV V	ns	MAN

^{*} Nese parameters are characterized but not tested.

Note 1: Measurements are taken in RC Mode where CLKOUT output is 4 x Tosc.

[†] Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

^{††} These parameters are asynchronous events not related to any internal clock edge.

FIGURE 22-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING

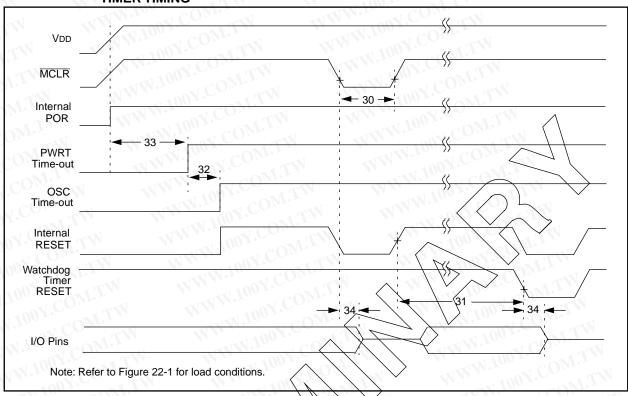


FIGURE 22-5: BROWN-OUT RESETTIMING

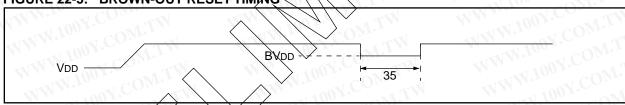


TABLE 22-4: RESET, WATCHOOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER, AND BROWN-OUT RESET REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
30	TrncL	MCLR Rulse Width (low)	2	11000		μs	VDD = 5V, -40°C to +125°C
31*	Twdt	Watchdog Timer Time-out Period (No Prescaler)	7	18	33	ms	VDD = 5V, -40°C to +125°C
32	Tost	Oscillation Start-up Timer Period		1024 Tosc		ľ.T.	Tosc = OSC1 period
33*	Tpwrt	Power-up Timer Period	28	72	132	ms	$VDD = 5V, -40^{\circ}C \text{ to } +125^{\circ}C$
34	Tioz	I/O Hi-impedance from MCLR Low or WDT reset		MA	2.1	μs	M MM
35	TBOR	Brown-out Reset Pulse Width	100	N 1 = 10	0 T.	μs	VDD ≤ BVDD (D005)

^{*} These parameters are characterized but not tested.

[†] Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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FIGURE 22-6: TIMERO AND TIMER1 EXTERNAL CLOCK TIMINGS

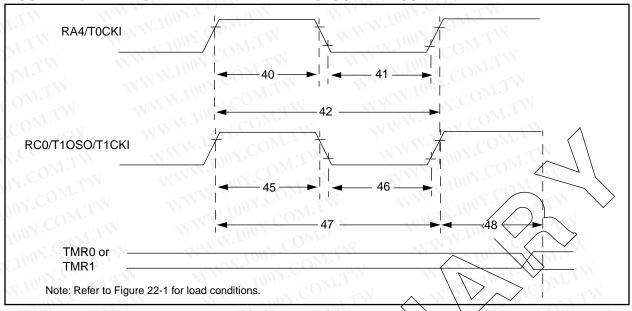


TABLE 22-5: TIMERO AND TIMER1 EXTERNAL CLOCK REQUIREMENTS

Param No.	Sym	Characteristic	MMA	1.100½.CO	Min	Typt	Max	Units	Conditions
40*	Tt0H	T0CKI High Pulse V	Vidth	No Prescaler	0.5TcY+20	7/	_	ns	Must also meet
	100	OM.		With Prescaler	10		147	ns	parameter 42
41*	TtOL	T0CKI Low Pulse W	/idth	No Prescaler	0.5(CY + 20	1-	-31	ns	Must also meet
	You.	CO		With Prescaler	10	I —	Mr.	ns	parameter 42
42*	Tt0P	T0CKI Period		No Prescater	7CY + 40	T —	-311	ns	CON.
	NW.100	OY.COM.TV		With Prescaler	Greater of: 20 or <u>Tcy + 40</u> N	_	N.	ns	N = prescale value (2, 4,, 256)
45*	Tt1H	T1CKI High Time	Synchronous, F	Prescaler = 1	0.5Tcy + 20	<u> </u>	- 1	ns	Must also meet
		00 r. OW. J	Synchronous,	PIC16C6X	15	-1	_	ns	parameter 47
	N N N	00 ^y .Co	Prescaler = 2,4,8	PIC 16LC6X	25	\\	_	ns	W.100Y.
	MM.	1008-4//	Asynchronous	PIC16 C 6X	30	1/7	_	ns	, 100 x.
	TAX V			PIC16LC6X	50	~ \\	_	ns	MM.
46*	Tt1L	T1CKI Low Time	Synchronous, F	Prescaler = 1	0.5Tcy + 20	737	_	ns	Must also meet
	Wix		Synchronous,	PIC16 C 6X	15	TV	· —	ns	parameter 47
			Prescaler = 2,4,8	PIC16 LC 6X	25	11.2	W	ns	MMM.100
		$\langle \vee \wedge \rangle$	Asynchronous	PIC16 C 6X	30	NF.	- 4 1	ns	TWW.10
		1	WILL	PIC16LC6X	50	77	1.11	ns	1111
47*	Trip	T1CK input period	Synchronous	PIC16 C 6X	Greater of: 30 OR TCY + 40 N	$co_{\overline{M}}$	TW	ns	N = prescale value (1, 2, 4, 8)
		MMM.100	Y.COM.	PIC16 LC 6X	Greater of: 50 OR TCY + 40 N	CO	M.T	N	N = prescale value (1, 2, 4, 8)
		MM	Asynchronous	PIC16 C 6X	60	X-	1	ns	Man
		II.WW.II	TI COM	PIC16LC6X	100	√ 7€	$\Omega \pi_{r}$	ns	War
	Ft1	Timer1 oscillator inp (oscillator enabled by		0	DC	0 F.	200	kHz	i w
48	TCKEZtmr1	Delay from external	clock edge to tir	ner increment	2Tosc	00	7Tosc	V7	

These parameters are characterized but not tested.

[†] Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 22-7: CAPTURE/COMPARE/PWM TIMINGS (CCP1 AND CCP2)

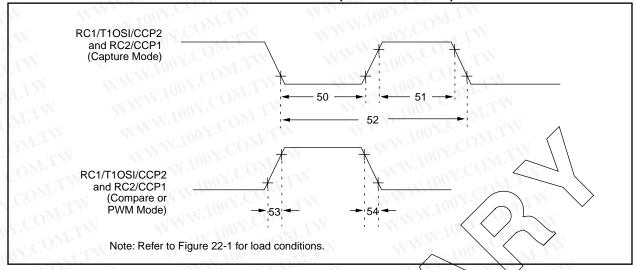


TABLE 22-6: CAPTURE/COMPARE/PWM REQUIREMENTS (CCP1 AND CGP2)

Param No.	Sym	Characteristic		Y.COM.TY	Min	Typt	Max	Units	Conditions
50*	TccL	CCP1 and CCP2	No Prescaler	W.COM	0.5Tc+ + 2Q	_	<u> </u>	ns	TW
	- c0	input low time	With Prescaler	PIC16CR63/R65	10	4	170	ns	OM
	1.0	W.TW	W TW.	PIC16LCR63/R65	30	-	$N_{\widehat{\mathcal{A}}_{\Omega}}$	ns	OM
51*	TccH	CCP1 and CCP2	No Prescaler		0.5Tcy + 20	$M_{\overline{A}}$.	~ √ 1	ns	COMITY
	N.	input high time	With Prescaler	PIC16 CR 63/R65	10	ATV.	<u> </u>	ns	WTM
	JU -	COM.		PIC16LCR63/R65	20	7/	M\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\	ns	V.CO.
52*	TccP	CCP1 and CCP2 in	nput period		3Tcy + 40 N	_	W	ns	N = prescale value (1,4, or 16)
53*	TccR	CCP1 and CCP2 of	output rise time	PIC16CR63/R65	7	10	25	ns	ONICO
	N.10	COM.	$\langle \ \rangle$	PIC16LCR63/R65	DATE:	25	45	ns	ON COM
54*	TccF	CCP1 and CCP2	output fall time	PIC16 CR 63/R65	OMT	10	25	ns	Ing COM
	1			PIC16 LCR 63/R65	WET W	25	45	ns	1.1001.

Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested. † tested.

PIC16C6X

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FIGURE 22-8: PARALLEL SLAVE PORT TIMING (PIC16CR65)

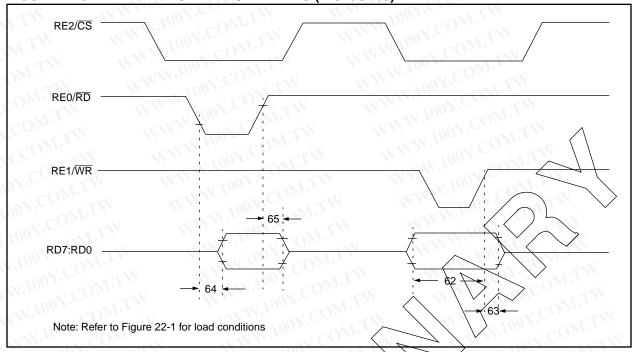


TABLE 22-7: PARALLEL SLAVE PORT REQUIREMENTS (PIC16CR65)

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
62*	TdtV2wrH	Data in valid before WR↑ or CS↑ (setup time)	20	_	<u> </u>	ns	· MOD
63*	TwrH2dtl	WR↑ or CS↑ to data-in invalid (hold R1C16CR65	20	_	4/Th	ns	N.O.
Wire		time) PIC16LCR65	35	_	4	ns	WY.Co.
64	TrdL2dtV	RD↓ and CS↓ to data–out valid		J —	80	ns	ON COL
65*	TrdH2dtl	RD↑ or CS↑ to data—out invalid	10		30	ns	Too - CC

* These parameters are characterized but not tested. >

† Data in "Typ" column is at 5%, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.



FIGURE 22-9: SPI MODE TIMING

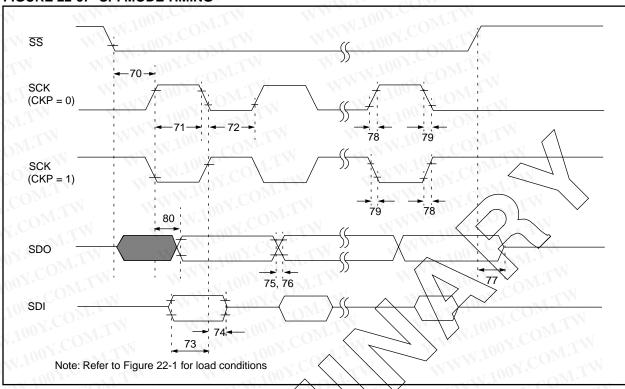


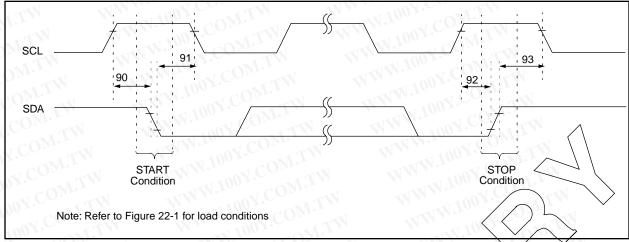
TABLE 22-8: SPI MODE REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Тур†	Max	Units	Conditions
70*	TssL2scH, TssL2scL	SS↓ to SCK↓ or SCK↑ input	Tcy	-	41	ns	M.COM
71*	TscH	SCK input high time (slave mode)	Tcy + 20	N _		ns	OY.CON
72*	TscL CON	SCK input low time (slave mode)	Tcy + 20	-W-	-4	ns	ON CO.
73*	TdiV2scH, TdiV2scL	Setup time of SDI data input to SCK edge	50	TW	_	ns	100X.CO
74*	TscH2diL, TscL2diL	Hold time of SDI data input to SCK edge	50	I.FI	_	ns	N.100Y.C
75*	TdoR)	SDO data output rise time	$700\overline{\lambda}$	10	25	ns	W.100 1
76*	TooF	SDO data output fall time	1007.0	10	25	ns	1007
77*	TşsH2doZ	SS↑ to SDO output hi-impedance	10	<u> </u>	50	ns	7 100
/78* <u> </u>	TscR	SCK output rise time (master mode)	N.In	10	25	ns	WWI
79*	TscF	SCK output fall time (master mode)	W.100	10	25	ns	TANN TO
80*	TscH2doV, TscL2doV	SDO data output valid after SCK edge	MM-100	V.COD	50	ns	WWW.1

^{*} These parameters are characterized but not tested.

[†] Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 22-10: I²C BUS START/STOP BITS TIMING



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TABLE 22-9: I²C BUS START/STOP BITS REQUIREMENTS

Parameter No.	Sym	Characteristic	M.100x.COM	Min	Тур	Max	Units	Conditions
90*	Tsu:sta	START condition	100 kHz mode	4700			700	Only relevant for repeated STAR
		Setup time	400 kHz mode	600	_	_/	ns	condition
91*	THD:STA	START condition	100 kHz mode	4000	(1	After this period the first clock
	COM	Hold time	400 kHz mode	600		X	ns	pulse is generated
92*	Tsu:sto	STOP condition	100 kHz mode	470Q	F	F	>	1 COM:
	ON CO	Setup time	400 kHz mode	600	-		ns	WW TOOY.CO
93	THD:STO	STOP condition	100 kHz mode	4000		\triangleright		MM. COB
	1007.0	Hold time	400 kHz mode	600	7		ns	W. TW. 100 r. COM
These par	ameters are	Hold time characterized but no		608		TW	N	MMM.100X.CO



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FIGURE 22-11: I²C BUS DATA TIMING

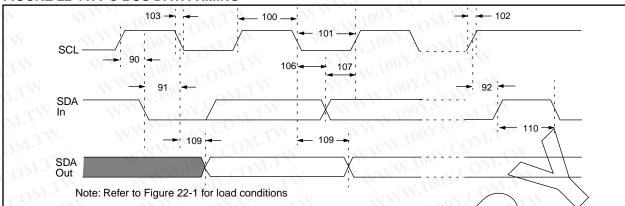


TABLE 22-10: I²C BUS DATA REQUIREMENTS

Parameter No.	Sym	Characteristic	OY.COM.TV	Min	Max	Units	Conditions
100*	THIGH	Clock high time	100 kHz mode	4.0	1	μs	Device must operate at a minimum of 1.5 MHz
100X.C		MAN	400 kHz mode	0.6	_ /	us	Device must operate at a min imum of 10 MHz
1007.			SSP Module	1.5Tex	/ /		CONL
101*	TLOW	Clock low time	100 kHz mode	4.7		μs	Device must operate at a minimum of 1.5 MHz
W.100		ILM MA	400 kHz mode	1.3	>-	μs	Device must operate at a minimum of 10 MHz
100		1.7.	SSP Module	1.5TcV	_		N.To. COM.
102*	TR	SDA and SCL rise	100 kHz mode	\ <u> </u>	1000	ns	1100x.
MM'I		time	400 kH2 mode	20 ≠ 0.1Cb	300	ns	Cb is specified to be from 10-400 pF
103*	TF	SDA and SCL fall time	100 kHz mode	COE	300	ns	M. ON.CO
MAN		OWIL	400 kHz mode	20 + 0.1Cb	300	ns	Cb is specified to be from 10-400 pF
90*	Tsu:sta	START condition	100 kHz mode	4.7	-31	μs	Only relevant for repeated
		setup time	400 kHz mode	0.6	27	μs	START condition
91*	THD:STA	START condition hold	100 kHz mode	4.0	- - -W	μs	After this period the first clock
		time /	400 kHz mode	0.6	15	μs	pulse is generated
106*	THD:DAT	Data input hold time	100 kHz mode	0	17	ns	W. 1001.
V .	WWW.		400 kHz mode	0	0.9	μs	WWW.
107*	TSU:DAT	Data input setup time	100 kHz mode	250	OH.	ns	Note 2
4			400 kHz mode	100	<u> </u>	ns	MM. 1001.6
92*	Tsu:ste	STOP condition setup	100 kHz mode	4.7	~ ()	μs	TIWW.
		time	400 kHz mode	0.6	= 1	μs	W . 100 r.
109*	TAA	Output valid from	100 kHz mode	144.5	3500	ns	Note 1
		člock	400 kHz mode	- TV	- 7 0	ns	
110*	TBUF	Bus free time	100 kHz mode	4.7	15	μs	Time the bus must be free
	VWV	W.100Y.COM	400 kHz mode	1.3	O.Y.C.	μs	before a new transmission car start
	Cb	Bus capacitive loading		A VIVE	400	pF	TO THE TAXABLE PARTY

These parameters are characterized but not tested.

Note 1: As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (min. 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

2: A fast-mode (400 kHz) I²C-bus device can be used in a standard-mode (100 kHz) I²C-bus system, but the requirement Tsu:DAT ≥ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line TR max.+tsu;DAT = 1000 + 250 = 1250 ns (according to the standard-mode I²C bus specification) before the SCL line is released.

FIGURE 22-12: USART SYNCHRONOUS TRANSMISSION (MASTER/SLAVE) TIMING

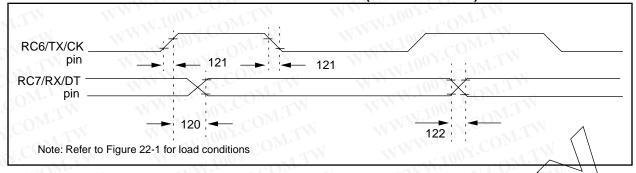


TABLE 22-11: USART SYNCHRONOUS TRANSMISSION REQUIREMENTS

Param No.	Sym	Characteristic	M.TW	Min	Typ†	Max	Units	Conditions
120*	TckH2dtV	SYNC XMIT (MASTER & SLAVE)	PIC16CR63/R65		4-11	80	ns	
	TI	Clock high to data out valid	PIC16LCR63/R65	70		100	ns	
121*	Tckrf	Clock out rise time and fall time	PIC16CR63/R65	-11	1	45	ns	TW
	COM	(Master Mode)	PIC16LCR63/R65		1-1	> 50 >	ns	TIN
122*	Tdtrf	Data out rise time and fall time	PIC16CR63/R65	1	+	45	ns	Mi
	Y.CON	TW WW 100	PIC16LCR63/R65	+	1-1	50	ns	MIN

These parameters are characterized but not tested.

FIGURE 22-13: USART SYNCHRONOUS RECEIVE (MASTER/SLAVE) TIMING

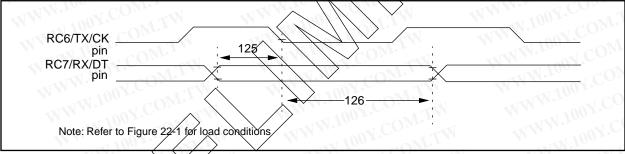


TABLE 22-12: USART SYNCHRONOUS RECEIVE REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Тур†	Max	Units	Conditions
125*		SYNC RCV (MASTER & SLAVE) Data setup before CK ↓ (DT setup time)	15	- <u>- w</u> O _M -	TVL	ns	WW.10
126*	TckL2dtl	Data hold after CK ↓ (DT hold time)	15	<u> </u>	14	ns	M

^{*} These parameters are characterized but not tested.

^{†:} Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

^{†:} Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

23.0 ELECTRICAL CHARACTERISTICS FOR PIC16C66/67

Absolute Maximum Ratings (†) Ambient temperature under bias.....-55°C to +125°C Voltage on any pin with respect to Vss (except VDD, MCLR, and RA4)-0.3V to (VDD + 0.3V) Voltage on VDD with respect to Vss-0.3V to +7.5V Input clamp current, IIK (VI < 0 or VI > VDD)±20 mA Maximum current sourced by PORTA, PORTB, and PORTE (Note 3) (combined)200 mA

- **Note 1:** Power dissipation is calculated as follows: Pdis = VDD x {IDD Σ IOH} + Σ {(VDD-VOH) x IOH} + Σ (Vol x IOL)
- Note 2: Voltage spikes below Vss at the \overline{MCLR}/VPP pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100 Ω should be used when applying a "low" level to the \overline{MCLR}/VPP pin rather than pulling this pin directly to Vss.
- Note 3: PORTD and PORTE not available on the PIC16C66.

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 23-1: CROSS REFERENCE OF DEVICE SPECS FOR OSCILLATOR CONFIGURATIONS AND FREQUENCIES OF OPERATION (COMMERCIAL DEVICES)

osc	PIC16C66-04 PIC16C67-04	PIC16C66-10 PIC16C67-10	PIC16C66-20 PIC16C67-20	PIC16LC66-04 PIC16LC67-04	JW Devices
RC	VDD: 4.0V to 6.0V IDD: 5 mA max. at 5.5V IPD: 16 µA max. at 4V Freq: 4 MHz max.	VDD: 4.5V to 5.5V IDD: 2.7 mA typ. at 5.5V IPD: 1.5 μA typ. at 4V Freq: 4 MHz max.	VDD: 4.5V to 5.5V IDD: 2.7 mA typ. at 5.5V IPD: 1.5 μA typ. at 4V Freq: 4 MHz max.	VDD: 2.5V to 6.0V IDD: 3.8 mA max. at 3V IPD: 5 μA max. at 3V Freq: 4 MHz max.	VDD: 4.0V to 6.0V IDD: 5 mA max. at 5.5V IPD: 16 μA max. at 4V Freq: 4 MHz max.
XT	VDD: 4.0V to 6.0V IDD: 5 mA max. at 5.5V IPD: 16 µA max. at 4V Freq: 4 MHz max.	VDD: 4.5V to 5.5V IDD: 2.7 mA typ. at 5.5V IPD: 1.5 μA typ. at 4V Freq: 4 MHz max.	VDD: 4.5V to 5.5V IDD: 2.7 mA typ. at 5.5V IPD: 1.5 μA typ. at 4V Freq: 4 MHz max.	VDD: 2.5V to 6.0V IDD: 3.8 mA max. at 3V IPD: 5 μA max. at 3V Freq: 4 MHz max.	VDD: 4.0V to 6.0V IDD: 5 mA max. at 5.5V IPD: 16 µA max. at 4V Freq: 4 MHz max.
HS	VDD: 4.5V to 5.5V IDD: 13.5 mA typ. at 5.5V	VDD: 4.5V to 5.5V IDD: 10 mA max. at 5.5V	VDD: 4.5V to 5.5V IDD: 20 mA max. at 5.5V	Not recommended for use in HS mode	VDD: 4.5V to 5.5V IDD: 20 mA max. at 5.5V
	IPD: 1.5 μA typ. at 4.5V	IPD 1.5 μA typ. at 4.5V	IPD: 1.5 μA typ. at 4.5V	use in 113 mode	IPD: 1.5 μA typ. at 4.5V
	Freq: 4 MHz max.	Freq: 10 MHz max.	Freq: 20 MHz max.	ON COMP	Freq: 20 MHz max.
LP	VDD: 4.0V to 6.0V IDD: 52.5 μA typ. at 32 kHz, 4.0V IPD: 0.9 μA typ. at 4.0V Freq: 200 kHz max.	Not recommended for use in LP mode	Not recommended for use in LP mode	VDD: 2.5V to 6.0V IDD: 48 μA max. at 32 kHz, 3.0V IPD: 5 μA max. at 3.0V Freq: 200 kHz max.	VDD: 2.5V to 6.0V IDD: 48 μA max. at 32 kHz, 3.0V IPD: 5 μA max. at 3.0V Freq: 200 kHz max.

The shaded sections indicate oscillator selections which are tested for functionality, but not for MIN/MAX specifications. It is recommended that the user select the device type that ensures the specifications required.

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Applicable Devices 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

23.1 DC Characteristics: PIC16C66/67-04 (Commercial, Industrial, Extended)

PIC16C66/67-10 (Commercial, Industrial, Extended)
PIC16C66/67-20 (Commercial, Industrial, Extended)

Standard Operating Conditions (unless otherwise stated)

DC CHARACTERISTICS

Operating temperature -40°C

-40°C \leq TA \leq +125°C for extended, -40°C \leq TA \leq +85°C for industrial and

 $40 \text{ C} \leq 1A \leq +85 \text{ C} \text{ for common}$

Param	Characteristic	Cum	Min	Trent	Max	Units	Conditions
No.	Characteristic	Sym	IVIIN	Typ†	wax	Units	Conditions
D001 D001A	Supply Voltage	VDD	4.0 4.5	1.TV	6.0 5.5	V	XT, RC and LP osc configuration HS osc configuration
D002*	RAM Data Retention Voltage (Note 1)	VDR	ov.CO	1.5	-W	V	WWW.100Y.COM.TW
D003	VDD start voltage to ensure internal Power-on Reset signal	VPOR	00 ⁷ .C	Vss	TW IT	V	See section on Power-on Reset for details
D004*	VDD rise rate to ensure internal Power-on Reset signal	SVDD	0.05	N.CC	M.T M.	V/ms	See section on Power-on Reset for details
D005	Brown-out Reset Voltage	BVDD	3.7	4.0	4.3	V	BODEN configuration bit is enabled
	CONTRACTOR	WV	3.7	4.0	4.4	V	Extended Range Only
D010	Supply Current (Note 2, 5)	IDD	MAN.	2.7	5	mA	XT, RC, osc config Fosc = 4 MHz, VDD = 5.5V (Note 4)
D013	N.100X.COM.TW		WW	10	20	mA	HS osc config Fosc = 20 MHz, VDD = 5.5V
D015*	Brown-out Reset Current (Note 6)	Δlbor	M.	350	425	μΑ	BOR enabled, VDD = 5.0V
D020	Power-down Current	IPD	- 17	10.5	42	μΑ	VDD = 4.0V, WDT enabled,-40°C to +85°C
D021	(Note 3, 5)	· · · · · · · · · · · · · · · · · · ·	- `	1.5	16	μΑ	VDD = 4.0V, WDT disabled,-0°C to +70°C
D021A	MM. 2100X.	L.M.	- 1	1.5	19	μΑ	VDD = 4.0V, WDT disabled,-40°C to +85°C
D021B	MMM. TOON COM	WT	-	2.5	19	μΑ	VDD = 4.0V, WDT disabled,-40°C to +125°C
D023*	Brown-out Reset Current (Note 6)	Δlbor	-	350	425	μΑ	BOR enabled, VDD = 5.0V

- * These parameters are characterized but not tested.
- † Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.
- Note 1: This is the limit to which VDD can be lowered without losing RAM data.
 - 2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.

The test conditions for all IDD measurements in active operation mode are:

OSC1 = external square wave, from rail to rail; all I/O pins tristated, pulled to VDD,

MCLR = VDD; WDT enabled/disabled as specified.

- 3: The power down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and Vss.
- 4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kOhm.
- 5: Timer1 oscillator (when enabled) adds approximately 20 µA to the specification. This value is from characterization and is for design guidance only. This is not tested.
- 6: The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

23.2 DC Characteristics: PIC16LC66/67-04 (Commercial, Industrial)

DC CHA	RACTERISTICS	Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq \text{TA} \leq +85^{\circ}\text{C}$ for industrial and $0^{\circ}\text{C} \leq \text{TA} \leq +70^{\circ}\text{C}$ for commercial										
Param No.	Characteristic	Sym	Min	Тур†	Max	Units	Conditions					
D001	Supply Voltage	VDD	2.5	-	6.0	٧	LP, XT, RC osc configuration (DC - 4 MHz)					
D002*	RAM Data Retention Voltage (Note 1)	VDR	W.TV	1.5	-4	V	TOOK CONTRA					
D003	VDD start voltage to ensure internal Power-on Reset signal	VPOR	M.T.MC	Vss	-	V	See section on Power-on Reset for details					
D004*	VDD rise rate to ensure internal Power-on Reset signal	SVDD	0.05	TY	-	V/ms	See section on Power-on Reset for details					
D005	Brown-out Reset Voltage	BVDD	3.7	4.0	4.3	V	BODEN configuration bit is enabled					
D010	Supply Current (Note 2, 5)	IDD	N.CC	2.0	3.8	mA	XT, RC osc configuration FOSC = 4 MHz, VDD = 3.0V (Note 4)					
D010A	COM.TW W	NN.I	100 <u>1</u>	22.5	48	μА	LP osc configuration Fosc = 32 kHz, VDD = 3.0V, WDT disabled					
D015*	Brown-out Reset Current (Note 6)	ΔIBOR	100	350	425	μА	BOR enabled, VDD = 5.0V					
D020	Power-down Current	IPD	14.5	7.5	30	μΑ	VDD = 3.0V, WDT enabled, -40°C to +85°C					
D021	(Note 3, 5)	1	11-11	0.9	5	μΑ	VDD = 3.0V, WDT disabled, 0°C to +70°C					
D021A	OOY.COM.TW	WV	NW.1	0.9	5	μА	VDD = 3.0V, WDT disabled, -40°C to +85°C					
D023*	Brown-out Reset Current (Note 6)	ΔIBOR	WW	350	425	μА	BOR enabled, VDD = 5.0V					

- These parameters are characterized but not tested.
- † Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.
- Note 1: This is the limit to which VDD can be lowered without losing RAM data.
 - 2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
 - The test conditions for all IDD measurements in active operation mode are:
 - OSC1 = external square wave, from rail to rail; all I/O pins tristated, pulled to VDD,
 - MCLR = VDD; WDT enabled/disabled as specified.
 - 3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and Vss.
 - 4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kOhm.
 - 5: Timer1 oscillator (when enabled) adds approximately 20 µA to the specification. This value is from characterization and is for design guidance only. This is not tested.
 - 6: The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

PIC16C6X

DC CHARACTERISTICS

Applicable Devices 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

23.3 DC Characteristics: PIC16C66/67-04 (Commercial, Industrial, Extended)

PIC16C66/67-10 (Commercial, Industrial, Extended)

PIC16C66/67-20 (Commercial, Industrial, Extended)

PIC16LC66/67-04 (Commercial, Industrial)

Standard Operating Conditions (unless otherwise stated)

Operating temperature $-40^{\circ}\text{C} \le \text{TA} \le +125^{\circ}\text{C}$ for extended, $-40^{\circ}\text{C} \le \text{TA} \le +85^{\circ}\text{C}$ for industrial and

 0° C $\leq TA \leq +70^{\circ}$ C for commercial

Operating voltage VDD range as described in DC spec Section 23.1 and

Section 23.2

Param No.	Characteristic	Sym	Min	Typ †	Max	Units	Conditions
00Y.C	Input Low Voltage I/O ports	VIL	WII		MI	W. 1	00X.COM.TW
D030	with TTL buffer	N.Co	Vss	-	0.15VDD	V	For entire VDD range
D030A	COM.	C C	Vss	N -	0.8V	V	4.5V ≤ VDD ≤ 5.5V
D031	with Schmitt Trigger buffer	00 7.	Vss	-	0.2VDD	V	1.100 COM.
D032	MCLR, OSC1 (in RC mode)	1007.	Vss	17	0.2VDD	V	N 100Y. OM.TW
D033	OSC1 (in XT, HS and LP)	OOV	Vss	~ ~	0.3VDD	V	Note1
VW.10	Input High Voltage I/O ports	Vih	$^{K}CO_{M}$	4	N		Mira
D040	with TTL buffer	W.Too	2.0		VDD	V	4.5V ≤ VDD ≤ 5.5V
D040A	100X.COM.TW WV	W.10	0.25VDD + 0.8V	<u>, 1</u>	VDD	V	For entire VDD range
D041	with Schmitt Trigger buffer	M M.	0.8VDD		VDD	V	For entire VDD range
D042	MCLR	11111	0.8VDD	70,	VDD	V	WW 1007.
D042A	OSC1 (XT, HS and LP)	TINV	0.7VDD	C-C	VDD	V	Note1
D043	OSC1 (in RC mode)	N ·	0.9VDD	-	VDD	V	WW.100 COM
D070	PORTB weak pull-up current	IPURB	50	250	400	μΑ	VDD = 5V, VPIN = VSS
D060	Input Leakage Current (Notes 2, 3) I/O ports	IIL W	N. 10	N.	.c.±1/1.7	μА	Vss ≤ VPIN ≤ VDD, Pin at hi- impedance
D061	MCLR, RA4/T0CKI		W.1	00	±5	μΑ	Vss ≤ Vpin ≤ Vdd
D063	OSC1			⁷ 00	±5	μA	Vss ≤ VPIN ≤ VDD, XT, HS and LP osc configuration
	Output Low Voltage			1.20	as CO	Na.	W WWW.
D080	I/O ports	VOL	W.	W-7	0.6	V	IOL = 8.5 mA, VDD = 4.5V, -40°C to +85°C
D080A	WWW.100X.COM.1	N	WV	W	0.6	V	IOL = 7.0 mA, VDD = 4.5V, -40°C to +125°C
D083	OSC2/CLKOUT (RC osc config)	W	- W		0.6		IOL = 1.6 mA, VDD = 4.5V, -40°C to +85°C
D083A	WWW.100X.COM	TW	- 1		0.6	V	IOL = 1.2 mA, VDD = 4.5V, -40°C to +125°C

These parameters are characterized but not tested.

- 2: The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.
- 3: Negative current is defined as current sourced by the pin.

[†] Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C6X be driven with external clock in RC mode.

Standard Operating Conditions (unless otherwise stated)

Operating temperature -40°C \leq TA \leq +125°C for extended, -40°C ≤ TA ≤ +85°C for industrial and

≤ TA ≤ +70°C for commercial 0°C

Operating voltage VDD range as described in DC spec Section 23.1 and Section 22.2

Param No.	Characteristic	Sym	Min	Typ †	Max	Units	Conditions
M.T.	Output High Voltage	-1		-73	Wiles	-7 CC	W.
D090	I/O ports (Note 3)	Vон	VDD-0.7		MM-10	V	IOH = -3.0 mA, VDD = 4.5 V, -40 °C to $+85$ °C
D090A	CM MAM. 1001.CC	M.T.	VDD-0.7	-	WW.1	V.	IOH = -2.5 mA, VDD = 4.5 V, -40 °C to $+125$ °C
D092	OSC2/CLKOUT (RC osc config)	$O_{M^{**}}$	VDD-0.7	-	WV-W	V	IOH = -1.3 mA, VDD = 4.5 V, -40 °C to $+85$ °C
D092A	WIM MAM. TOOK.	CO_{M}	VDD-0.7	-	M3N N	V. V00	IOH = -1.0 mA, VDD = 4.5 V, -40 °C to $+125$ °C
D150*	Open-Drain High Voltage	Vod	(17.7)	-	14	V	RA4 pin
00 ⁷ .C	Capacitive Loading Specs on Output Pins	Y.CO	M.TW		W	NW.	OOY.COM.TW
D100	OSC2 pin	Cosc ₂	OM:TY	N	15	pF	In XT, HS and LP modes when external clock is used to drive OSC1.
D101	All I/O pins and OSC2 (in RC mode)	Cio	M.	IN	50	pF	MIOON. COMITY
D102	SCL, SDA in I ² C mode	Cb	CODA	TV	400	pF	TOOY.CO. TTW

These parameters are characterized but not tested.

DC CHARACTERISTICS

- Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.
- Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C6X be driven with external clock in RC mode.
 - The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input volt-
 - 3: Negative current is defined as current sourced by the pin.

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PIC16C6X

Applicable Devices 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

23.4 <u>Timing Parameter Symbology</u>

The timing parameter symbols have been created following one of the following formats:

1. TppS2ppS 3. Tcc:st (I²C specifications only)
2. TppS 4. Ts (I²C specifications only)

T Frequency T Time

Lowercase letters (pp) and their meanings:

pp	M. 1001.		
CC	CCP1	osc	OSC1
ck	CLKOUT	rd	RD
cs	L'CS	rw	RD or WR
di	SDI	sc	SCK
do CO	SDO	SS	SS
dt	Data in	t0	TOCKI CONTRACTOR
io	I/O port	t1	T1CKI
mc	MCLR	wr	WR

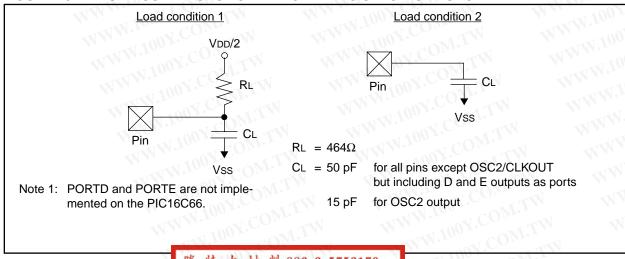
Uppercase letters and their meanings:

S		$O_{M^{*}}$	COM.
F 100	Fall	P	Period
WH .	High	R	Rise
J.W.10	Invalid (Hi-impedance)	CO Mr.	Valid
L 10	Low	Z OM.	Hi-impedance
I ² C only		M.COM	T.TW WY. 100 1. COM. T.
AA	output access	High	High
BUF	Bus free	Low	Low

Tcc:st (I²C specifications only)

CC	100x.	100 1.	OWITT	M. Jun COV
HD	Hold	SU	Setup	
ST		WWW.I		
DAT	DATA input hold	STO	STOP condition	
STA	START condition	77 100		

FIGURE 23-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS



23.5 <u>Timing Diagrams and Specifications</u>

FIGURE 23-2: EXTERNAL CLOCK TIMING

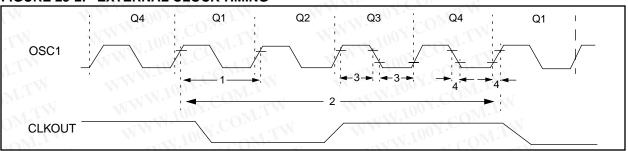


TABLE 23-2: EXTERNAL CLOCK TIMING REQUIREMENTS

Param No.	Sym	Characteristic	Min	Тур†	Max	Units	Conditions
a Co	Fosc	External CLKIN Frequency	DC	W-	4	MHz	XT and RC osc mode
7.		(Note 1)	DC	. √ . .≼T	4	MHz	HS osc mode (-04)
M.C.		MM 100X.	DC	LIN	10	MHz	HS osc mode (-10)
~√ C		WWW.	DC	-	20	MHz	HS osc mode (-20)
00 τ .		1, 100 -	DC	1. 1 <u> </u>	200	kHz	LP osc mode
NOV.		Oscillator Frequency	DC	V.IIV	4	MHz	RC osc mode
10-		(Note 1)	0.1		4	MHz	XT osc mode
1700		V.1.	4	$M_{\overline{r}_{r}}$	20	MHz	HS osc mode
100		MITH WWW TITO	5	ON!T	200	kHz	LP osc mode
1 Tosc	Tosc	External CLKIN Period	250			ns	XT and RC osc mode
	(Note 1)	250	$C\Theta_{MT}$	<u> </u>	ns	HS osc mode (-04)	
-11		WITH WITH	100	-	TA	ns	HS osc mode (-10)
M.		COM WAY	50	I'CA	(P)	ns	HS osc mode (-20)
		COM.	5	47 CO	VI.	μs	LP osc mode
		Oscillator Period	250) y =	MITT	ns	RC osc mode
WW		(Note 1)	250	V I C	10,000	ns	XT osc mode
11		COM.	250	= (250	ns	HS osc mode (-04)
MA		OY. WITH	100	$10\sigma_{T}$	250	ns	HS osc mode (-10)
177		OV.COM W	50	Vin V	250	ns	HS osc mode (-20)
1		COM	5	700	CONT.	μs	LP osc mode
2	Tcy	Instruction Cycle Time (Note 1)	200	TCY	DC	ns	Tcy = 4/Fosc
3*	TosL,	External Clock in (OSC1) High or	100	- 00	Y.C	ns	XT oscillator
	TosH	Low Time	2.5	Mra	~ √ 0	μs	LP oscillator
		31 100 Y. OM.TW	15	-1XN-19	M 7 CU	ns	HS oscillator
4*	TosR,	External Clock in (OSC1) Rise or	-1	M 47	25	ns	XT oscillator
	TosF	Fall Time		TW I N.	50	ns	LP oscillator
		1, 100 Y. W.T.	_		1015	ns	HS oscillator

^{*} These parameters are characterized but not tested.

Note 1: Instruction cycle period (TcY) equals four times the input oscillator time-base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1/CLKIN pin. When an external clock input is used, the "Max." cycle time limit is "DC" (no clock) for all devices.

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[†] Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 23-3: CLKOUT AND I/O TIMING

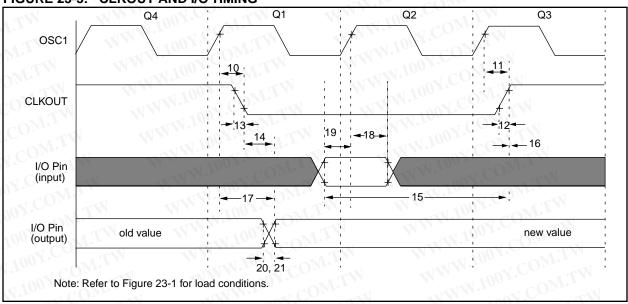


TABLE 23-3: CLKOUT AND I/O TIMING REQUIREMENTS

Parameter No.	Sym	Characteristic	OOX.COM	Min	Typ†	Max	Units	Conditions
10*	TosH2ckL	OSC1↑ to CLKOUT↓	1007.00	LVI-	75	200	ns	Note 1
11*	TosH2ckH	OSC1↑ to CLKOUT↑	···CO	TV	75	200	ns	Note 1
12*	TckR	CLKOUT rise time	N.100		35	100	ns	Note 1
13*	TckF	CLKOUT fall time	100	11.12	35	100	ns	Note 1
14*	TckL2ioV	CLKOUT ↓ to Port out valid	LKOUT ↓ to Port out valid			0.5Tcy + 20	ns	Note 1
15*	TioV2ckH	Port in valid before CLKOUT ↑	Tosc + 200	_	-	ns	Note 1	
16*	TckH2iol	Port in hold after CLKOUT ↑	0	-1	- 1	ns	Note 1	
17*	TosH2ioV	OSC1↑ (Q1 cycle) to Port out va	T.T.	50	150	ns	007.	
18*	TosH2ioI	OSC1↑ (Q2 cycle) to Port input	PIC16 C 66/67	100	1	-111	ns	100 Y.C.
	WW.10	invalid (I/O in hold time)	PIC16 LC 66/67	200		- 💉	ns	ov.C
19*	TioV2osH	Port input valid to OSC1↑ (I/O in	setup time)	0	77	_	ns	1.100
20*	TioR	Port output rise time	PIC16 C 66/67	17:4	10	40	ns	A 100 7.
	WWI	TOO CONT.	PIC16 LC 66/67	W.CO.	-717	80	ns	1007
21*	TioF	Port output fall time	PIC16 C 66/67	 CO	10	40	ns	Min
	MM	1100Y. OM.TW	PIC16 LC 66/67	100 F.	M.	80	ns	11V.100
22††*	Tinp	INT pin high or low time	Tcy	-	TVI	ns	10	
23††*	Trbp	RB7:RB4 change INT high or lov	w time	Tcy	(D)	TV V	ns	MAN

^{*} These parameters are characterized but not tested.

Note 1: Measurements are taken in RC Mode where CLKOUT output is 4 x Tosc.

[†] Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

^{††} These parameters are asynchronous events not related to any internal clock edge.

FIGURE 23-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING

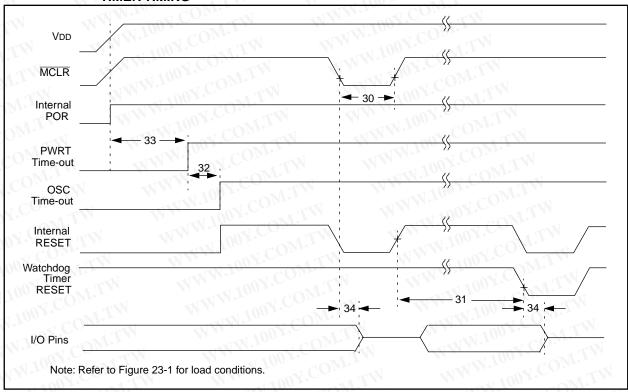


FIGURE 23-5: BROWN-OUT RESETTIMING

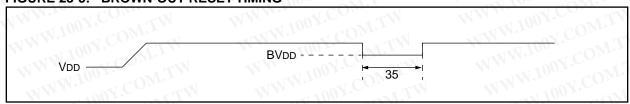


TABLE 23-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER, AND BROWN-OUT RESET REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions		
30	TmcL	MCLR Pulse Width (low)	2	11000	M.7	μs	VDD = 5V, -40°C to +125°C		
31*	Twdt	Watchdog Timer Time-out Period (No Prescaler)	7	18	33	ms	VDD = 5V, -40°C to +125°C		
32	Tost	Oscillation Start-up Timer Period	<u> </u>	1024 Tosc	(IOI)	$\Gamma_{T,s}$	Tosc = OSC1 period		
33*	Tpwrt	Power-up Timer Period	28	72	132	ms	VDD = 5V, -40°C to +125°C		
34	Tıoz	I/O Hi-impedance from MCLR Low or WDT reset	7/	MA. 100	2.1	μs	M MM		
35	TBOR	Brown-out Reset Pulse Width	100	N 1 10	OFF	μs	VDD ≤ BVDD (D005)		

^{*} These parameters are characterized but not tested.

[†] Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 23-6: TIMERO AND TIMER1 EXTERNAL CLOCK TIMINGS

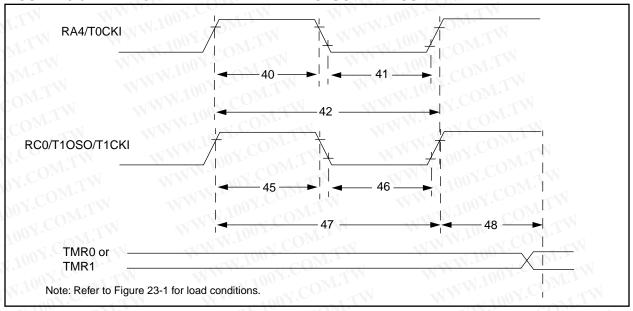


TABLE 23-5: TIMERO AND TIMER1 EXTERNAL CLOCK REQUIREMENTS

Param No.	Sym	Characteristic	MMA	1.100 J. CO.	Min	Тур†	Max	Units	Conditions		
40*	Tt0H	T0CKI High Pulse V	Vidth	No Prescaler	0.5Tcy + 20	7/		ns	Must also meet		
	70	COMP		With Prescaler	10	-1	1/1/1	ns	parameter 42		
41*	TtOL	T0CKI Low Pulse W	/idth	No Prescaler	0.5Tcy + 20	1 —	-30	ns	Must also meet		
		CO		With Prescaler	10	1 —	MA.	ns	parameter 42		
42*	Tt0P	T0CKI Period	7≥۔	No Prescaler	Tcy + 40	I —	-T1	ns	ON COP		
	WW.100	NY.COM.TW W		With Prescaler	Greater of: 20 or <u>Tcy + 40</u> N	_	1	ns	N = prescale value (2, 4,, 256)		
45*	45* Tt1H	T1CKI High Time	Synchronous, F	Prescaler = 1	0.5Tcy + 20	_	- 1	ns	Must also meet		
	-TXV.1	700 COW.	Synchronous,	PIC16 C 6X	15	-	_	ns	parameter 47		
		1001.COM	Prescaler = 2,4,8	PIC16 LC 6X	25	\\	_	ns	M. 100 J. C		
	MM.	100 Y.C	Asynchronous	PIC16 C 6X	30	1	_	ns	1001.		
		ON CON		PIC16LC6X	50		_	ns	MAN. OUN.		
46*	Tt1L	T1CKI Low Time	Synchronous, Prescaler = 1		0.5Tcy + 20		_	ns	Must also meet		
	WW	M. CO	Synchronous,	PIC16 C 6X	15	-	_	ns	parameter 47		
		MAM.100X.C.	Prescaler = 2,4,8	PIC16 LC 6X	25	- T	N	ns	WWW.100		
			Asynchronous	PIC16 C 6X	30	NE.	- N	ns			
	TV.			PIC16 LC 6X	50		1	ns			
47*	Tt1P	T1CKI input period	Synchronous	PIC16 C 6X	Greater of: 30 OR TCY + 40 N	COM	TW	ns	N = prescale value (1, 2, 4, 8)		
		WWW.100	Y.COM.	PIC16 LC 6X	Greater of: 50 OR TCY + 40 N	CO	M.T	W	N = prescale value (1, 2, 4, 8)		
		WWW	Asynchronous	PIC16 C 6X	60	1	17	ns	N. T.		
		WW.L	TOM	PIC16LC6X	100	-C	$\Omega_{\overline{M}_{\kappa}}$	ns	WW		
	Ft1	Timer1 oscillator inp (oscillator enabled by		0	DC	0 <u>2</u>	200	kHz			
48	TCKEZtmr1	Delay from external	clock edge to tir	mer increment	2Tosc	00.	7Tosc	VI-			

These parameters are characterized but not tested.

[†] Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 23-7: CAPTURE/COMPARE/PWM TIMINGS (CCP1 AND CCP2)

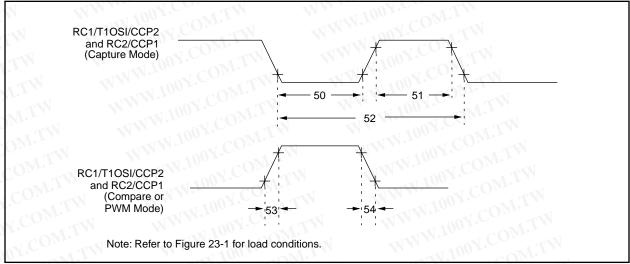


TABLE 23-6: CAPTURE/COMPARE/PWM REQUIREMENTS (CCP1 AND CCP2)

Parameter No.	Sym	Characteristic	MM.1007	Min	Тур†	Max	Units	Conditions	
50*	TccL	CCP1 and CCP2	No Prescaler	V.CON	0.5Tcy + 20	NZA.	<u> </u>	ns	WT
	~OM	input low time	With Prescaler	PIC16 C 66/67	10	+	1.70	ns	OM
		I.T.	W 10	PIC16 LC 66/67	20	-	N-10	ns	OM
51*	TccH	CCP1 and CCP2	No Prescaler		0.5Tcy + 20	MT.	× √ .1	ns	COMITY
	V.CC	input high time	With Prescaler	PIC16 C 66/67	10	ALV.		ns	WILL
	₹7 C	COMP		PIC16 LC 66/67	20	<u> </u>		ns	Y.COM TV
52*	TccP	CCP1 and CCP2 in	nput period	TIOON.CON	3Tcy + 40 N	_	W.	ns	N = prescale value (1,4, or 16)
53*	TccR	CCP1 and CCP2 of	output rise time	PIC16 C 66/67	- - 	10	25	ns	001.Co.
	$J_{0\alpha}$	PIC16 LC 66/6		PIC16 LC 66/67	DIVI.	25	45	ns	ON COM
54*	TccF	La Con and		PIC16 C 66/67	OM7	10	25	ns	Jan T COM
	11			PIC16 LC 66/67	-01/ - 11/1	25	45	ns	1.100 2.

^{*} These parameters are characterized but not tested.

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[†] Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 23-8: PARALLEL SLAVE PORT TIMING (PIC16C67)

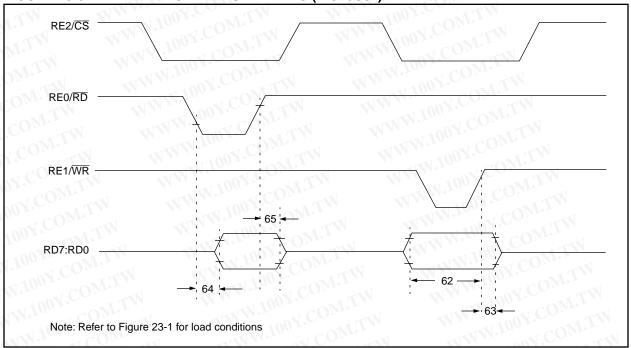


TABLE 23-7: PARALLEL SLAVE PORT REQUIREMENTS (PIC16C67)

Parameter No.	Sym	Characteristic	OM.T	Min	Typ†	Max	Units	Conditions
62*	TdtV2wrH	Data in valid before WR↑ or CS↑ (set	up time)	20	_	- XI	ns	COM
WWW	W.100Y.	COM.TW WWW		25	_	MIN.	ns	Extended Range Only
63*	TwrH2dtl	WR↑ or CS↑ to data–in invalid (hold	PIC16 C 67	20		_	ns	COL
	100	time)	PIC16 LC 67	35	_		ns	100 5
64	TrdL2dtV	RD↓ and CS↓ to data–out valid	1007.0	T.T	W	80	ns	1007
	WW.	OOY.COM.TW W		COM		90	ns	Extended Range Only
65*	TrdH2dtl	RD↑ or CS↑ to data–out invalid	111.1001	10	177	30	ns	W.100

^{*} These parameters are characterized but not tested.

[†] Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 23-9: SPI MASTER MODE TIMING (CKE = 0)

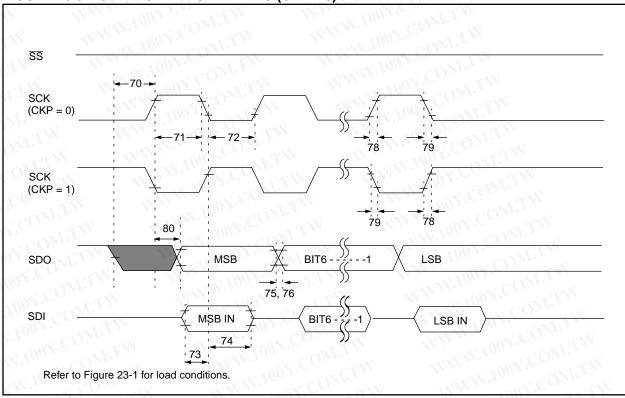
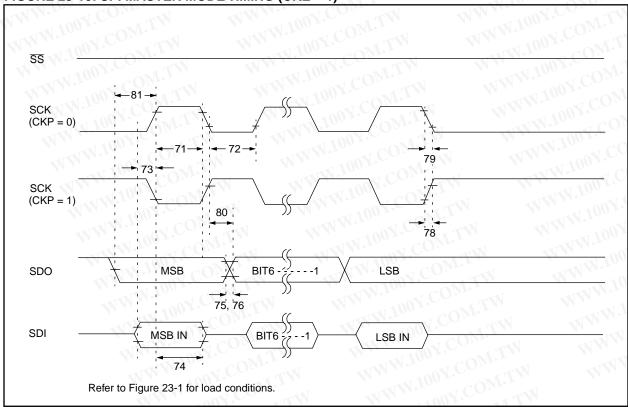


FIGURE 23-10: SPI MASTER MODE TIMING (CKE = 1)



PIC16C6X

Applicable Devices 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

FIGURE 23-11: SPI SLAVE MODE TIMING (CKE = 0)

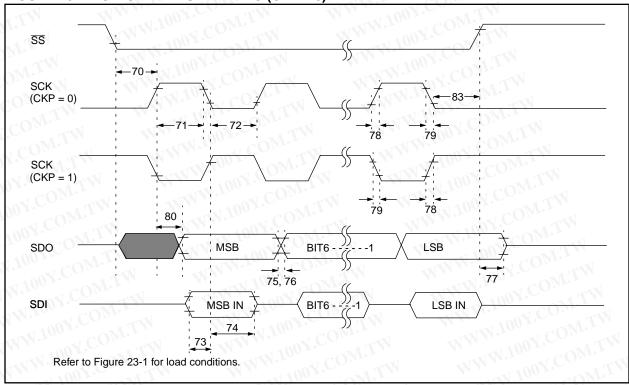
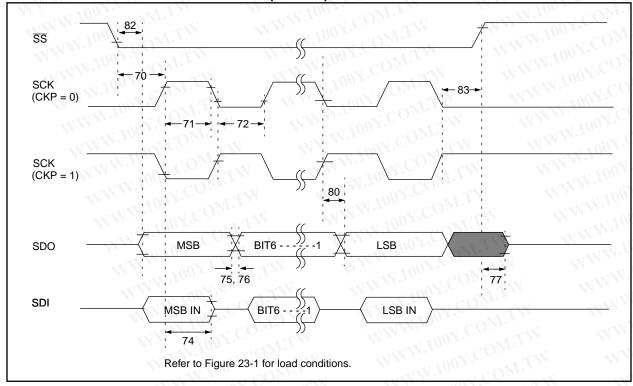


FIGURE 23-12: SPI SLAVE MODE TIMING (CKE = 1)



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TABLE 23-8: SPI MODE REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
70*	TssL2scH, TssL2scL	SS↓ to SCK↓ or SCK↑ input	Tcy	I.COM	V.TW	ns	
71*	TscH	SCK input high time (slave mode)	Tcy + 20	N.CO	-	ns	
72*	TscL	SCK input low time (slave mode)	Tcy + 20	- 7 CC	Mr.	ns	
73*	TdiV2scH, TdiV2scL	Setup time of SDI data input to SCK edge	100	00 7 .	OM.T	ns	
74*	TscH2diL, TscL2diL	Hold time of SDI data input to SCK edge	100	100 X	CO-Jy	ns	
75*	TdoR	SDO data output rise time	- 	10	25	ns	
76*	TdoF	SDO data output fall time	<u> </u>	10	25	ns	
77*	TssH2doZ	SS↑ to SDO output hi-impedance	10	700	50	ns	
78*	TscR	SCK output rise time (master mode)		10	25	ns	
79*	TscF	SCK output fall time (master mode)	_ ~	10	25	ns	-7
80*	TscH2doV, TscL2doV	SDO data output valid after SCK edge	- 1		50	ns	N
81*	TdoV2scH, TdoV2scL	SDO data output setup to SCK edge	Tcy	WW	70m z.	ns	TW
82*	TssL2doV	SDO data output valid after SS↓ edge	- N	WW	50	ns	WTN
83*	TscH2ssH, TscL2ssH	SS ↑ after SCK edge	1.5Tcy + 40	WA	W	ns	WIIM

^{*} These parameters are characterized but not tested.

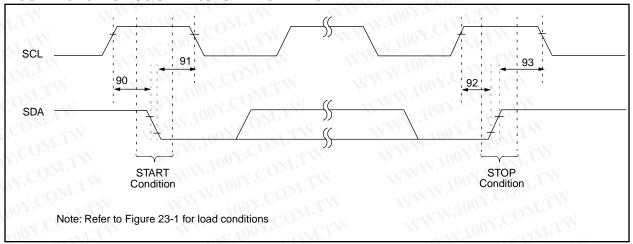
勝 特 力 材 料 886-3-5753170 胜特力电子(上海) 86-21-54151736 胜特力电子(深圳) 86-755-83298787 Http://www.100y.com.tw

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[†] Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 23-13: I²C BUS START/STOP BITS TIMING



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I²C BUS START/STOP BITS REQUIREMENTS **TABLE 23-9:**

Parameter No.	Sym	Characteristic	M.100 F. CO.	Min	Тур	Max	Units	Conditions
90*	Tsu:sta	START condition	100 kHz mode	4700		_	no	Only relevant for repeated START
	1.0	Setup time	400 kHz mode	600	44	_	ns	condition
91*	THD:STA	START condition	100 kHz mode	4000	147	_	200	After this period the first clock
	COM	Hold time	400 kHz mode	600	_	_	ns	pulse is generated
92*	Tsu:sto	STOP condition	100 kHz mode	4700	7	_		100 COM. 1
	CO.	Setup time	400 kHz mode	600	T	<i>N</i> —	ns	WWW 100Y.Com.T.
93	THD:STO	STOP condition	100 kHz mode	4000	NE.	- T		MM. COB
	1007.	Hold time	400 kHz mode	600	A.	7 7	ns	100 r. COM.

These parameters are characterized but not tested.

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FIGURE 23-14: I²C BUS DATA TIMING

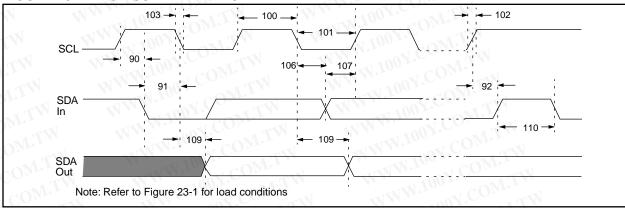


TABLE 23-10: I²C BUS DATA REQUIREMENTS

Parameter No.	Sym	Characteristic	ON.COM.TV	Min	Max	Units	Conditions
100*	THIGH	Clock high time	100 kHz mode	4.0	W.T.	μs	Device must operate at a min- imum of 1.5 MHz
100 X.C		N WWW	400 kHz mode	0.6		μs	Device must operate at a minimum of 10 MHz
1007.			SSP Module	1.5TcY			COMP
101*	TLOW	Clock low time	100 kHz mode	4.7	-1	μs	Device must operate at a minimum of 1.5 MHz
W.100		ILM MA	400 kHz mode	1.3	_	μs	Device must operate at a minimum of 10 MHz
100		1.7.	SSP Module	1.5TcY	_	- (1)	M.In. COM.
102*	TR	SDA and SCL rise	100 kHz mode	-TW	1000	ns	11001.
WW.Y		time	400 kHz mode	20 + 0.1Cb	300	ns	Cb is specified to be from 10-400 pF
103*	TF	SDA and SCL fall time	100 kHz mode	COE	300	ns	W. CON. CO.
WWW		OW.I.	400 kHz mode	20 + 0.1Cb	300	ns	Cb is specified to be from 10-400 pF
90*	Tsu:sta	START condition	100 kHz mode	4.7	- TA	μs	Only relevant for repeated
A A		setup time	400 kHz mode	0.6	177	μs	START condition
91*	THD:STA	START condition hold	100 kHz mode	4.0	- - -1	μs	After this period the first clock
		time	400 kHz mode	0.6	11.5	μs	pulse is generated
106*	THD:DAT	Data input hold time	100 kHz mode	0		ns	1002.
`	MM.To	COM	400 kHz mode	0	0.9	μs	MAN M. OOK.Co
107*	TSU:DAT	Data input setup time	100 kHz mode	250	$O_{\overline{A}^{-1}}$	ns	Note 2
4	MWW	any.Co.	400 kHz mode	100		ns	11/1/2/2017
92*	Tsu:sto	STOP condition setup	100 kHz mode	4.7	$\Box \Theta_{Mr}$	μs	WWW.L
	MM.	time	400 kHz mode	0.6		μs	W . 100 E
109*	TAA	Output valid from	100 kHz mode	W	3500	ns	Note 1
	N	clock	400 kHz mode		₂ C O	ns	11111.10
110*	TBUF	Bus free time	100 kHz mode	4.7	1-	μs	Time the bus must be free
		M.Too Y.COM	400 kHz mode	1.3	O.Y.C.	μs	before a new transmission car start
	Cb	Bus capacitive loading		TAT VILLE	400	pF	WWW.

^{*} These parameters are characterized but not tested.

- Note 1: As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (min. 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.
 - 2: A fast-mode (400 kHz) I²C-bus device can be used in a standard-mode (100 kHz) I²C-bus system, but the requirement Tsu:DAT ≥ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line TR max.+tsu;DAT = 1000 + 250 = 1250 ns (according to the standard-mode I²C bus specification) before the SCL line is released.

FIGURE 23-15: USART SYNCHRONOUS TRANSMISSION (MASTER/SLAVE) TIMING

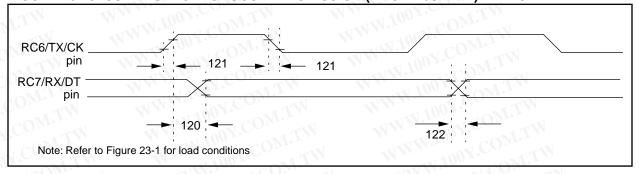


TABLE 23-11: USART SYNCHRONOUS TRANSMISSION REQUIREMENTS

Parameter No.	Sym	Characteristic	LTW	Min	Тур†	Max	Units	Conditions
120*	TckH2dtV	SYNC XMIT (MASTER & SLAVE)	PIC16 C 66/67	_	14.10	80	ns	_ 1
	WTI	Clock high to data out valid	PIC16 LC 66/67	7/1	= 1	100	ns	In
121*	Tckrf	Clock out rise time and fall time	PIC16 C 66/67	-01	MA.	45	ns	WT
	COM'L'	(Master Mode)	PIC16 LC 66/67		W.W.	50	ns	TIN
122*	Tdtrf	Data out rise time and fall time	PIC16 C 66/67	_	-314	45	ns	Will
	CON	TW WWW. 100X	PIC16 LC 66/67	_	WIN	50	ns	TILL

^{*} These parameters are characterized but not tested.

FIGURE 23-16: USART SYNCHRONOUS RECEIVE (MASTER/SLAVE) TIMING

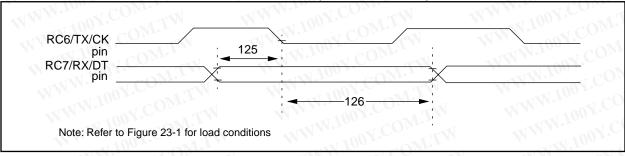


TABLE 23-12: USART SYNCHRONOUS RECEIVE REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
125*	TdtV2ckL	SYNC RCV (MASTER & SLAVE) Data setup before CK ↓ (DT setup time)	15	$CO_{j_{j_{p}}}$	TYL	ns	MM-70
126*	TckL2dtl	Data hold after CK ↓ (DT hold time)	15	(CA,	TH	ns	MAN

^{*} These parameters are characterized but not tested.

^{†:} Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

^{†:} Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

24.0 DC AND AC CHARACTERISTICS GRAPHS AND TABLES FOR: PIC16C62, PIC16C62A, PIC16C62, PIC16C63, PIC16C64, PIC16C64A, PIC16C66A, PIC16C65A, PIC16C66, PIC16C67

The graphs and tables provided in this section are for design guidance and are not tested or guaranteed.

In some graphs or tables the data presented are outside specified operating range (i.e., outside specified VDD range). This is for information only and devices are guaranteed to operate properly only within the specified range.

Note: The data presented in this section is a statistical summary of data collected on units from different lots over a period of time and matrix samples. 'Typical' represents the mean of the distribution at, 25° C, while 'max' or 'min' represents (mean +3 σ) and (mean -3 σ) respectively where σ is standard deviation.

FIGURE 24-1: TYPICAL IPD vs. VDD (WDT DISABLED, RC MODE)

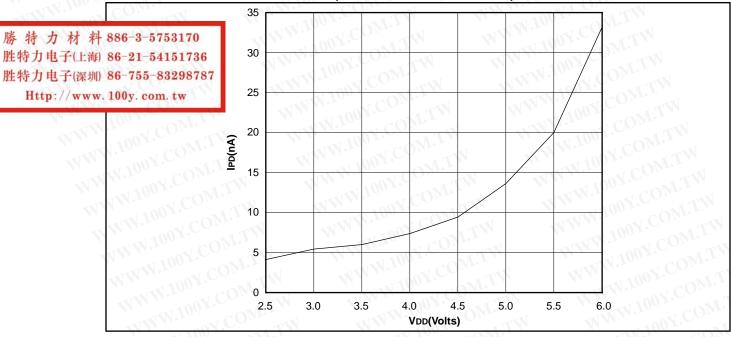


FIGURE 24-2: MAXIMUM IPD vs. VDD (WDT DISABLED, RC MODE)

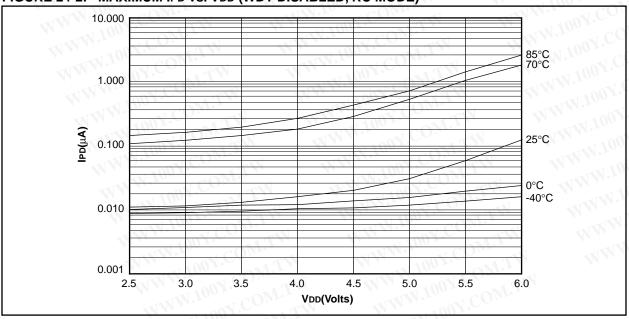


FIGURE 24-3: TYPICAL IPD vs. VDD @ 25°C (WDT ENABLED, RC MODE)

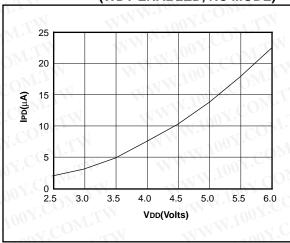


FIGURE 24-4: MAXIMUM IPD vs. VDD (WDT ENABLED, RC MODE)

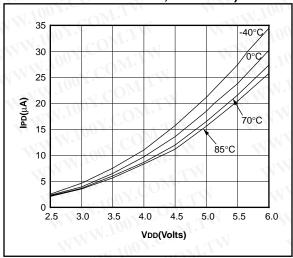


FIGURE 24-5: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD

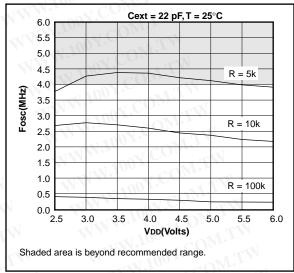


FIGURE 24-6: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD

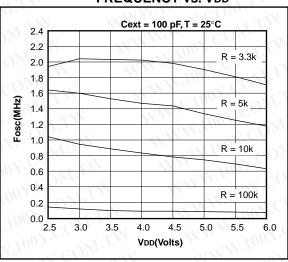


FIGURE 24-7: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD

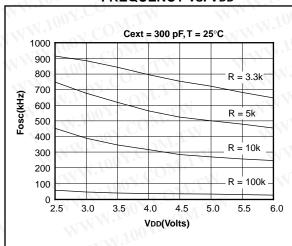


FIGURE 24-8: TYPICAL IPD vs. VDD BROWN-OUT DETECT ENABLED (RC MODE)

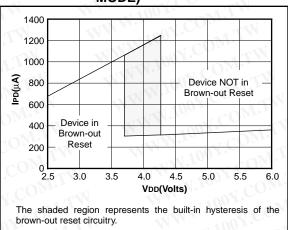


FIGURE 24-9: MAXIMUM IPD vs. VDD
BROWN-OUT DETECT
ENABLED
(85°C TO -40°C, RC MODE)

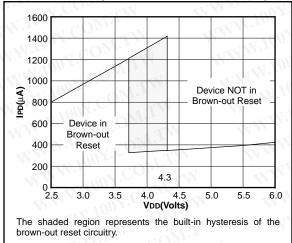


FIGURE 24-10: TYPICAL IPD vs. TIMER1 ENABLED (32 kHz, RC0/RC1 = 33 pF/33 pF, RC MODE)

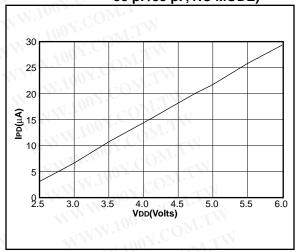


FIGURE 24-11: MAXIMUM IPD vs. TIMER1 ENABLED (32 kHz, RC0/RC1 = 33 pF/33 pF, 85°C TO -40°C, RC MODE)

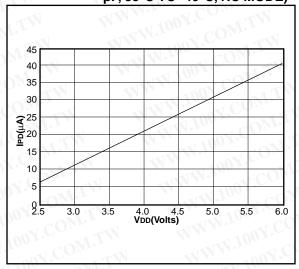


FIGURE 24-12: TYPICAL IDD vs. FREQUENCY (RC MODE @ 22 pF, 25°C)

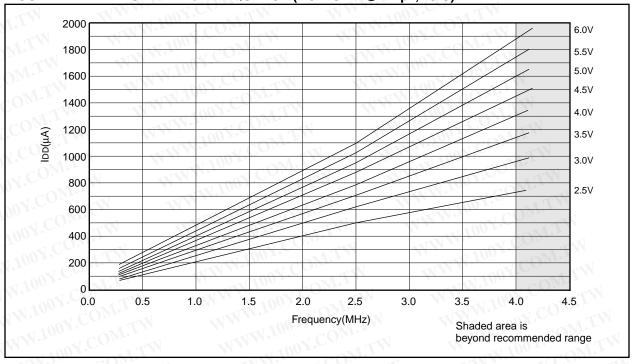


FIGURE 24-13: MAXIMUM IDD vs. FREQUENCY (RC MODE @ 22 pF, -40°C TO 85°C)

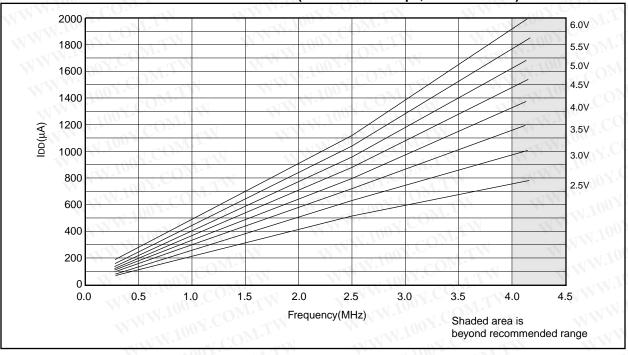


FIGURE 24-14: TYPICAL IDD vs. FREQUENCY (RC MODE @ 100 pF, 25°C)

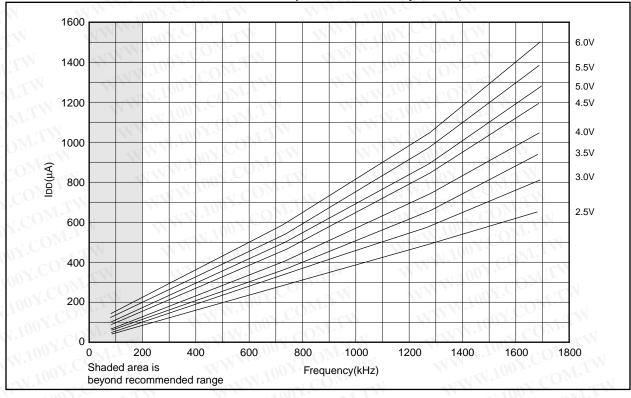
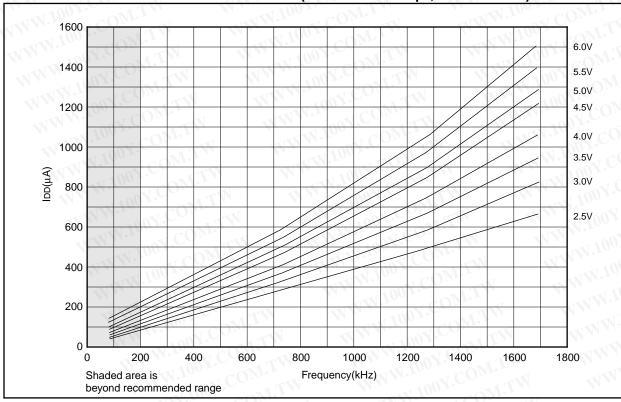


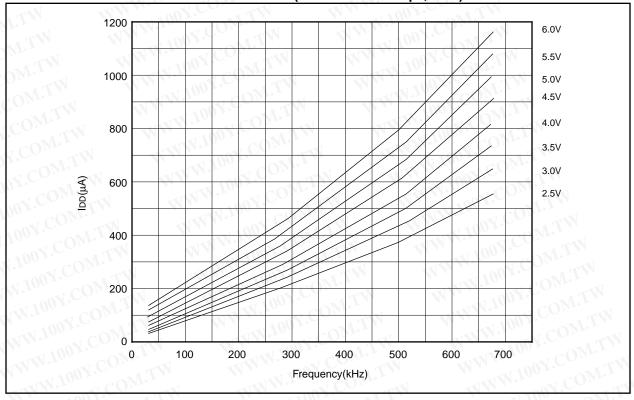
FIGURE 24-15: MAXIMUM IDD vs. FREQUENCY (RC MODE @ 100 pF, -40°C TO 85°C)



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FIGURE 24-16: TYPICAL IDD vs. FREQUENCY (RC MODE @ 300 pF, 25°C)



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FIGURE 24-17: MAXIMUM IDD vs. FREQUENCY (RC MODE @ 300 pF, -40°C TO 85°C)

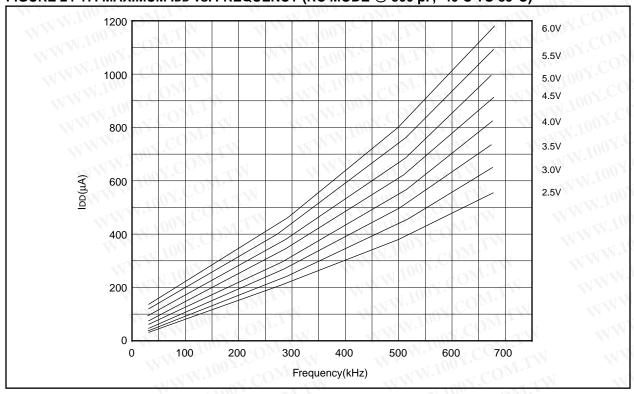


FIGURE 24-18: TYPICAL IDD vs.

CAPACITANCE @ 500 kHz

(RC MODE)

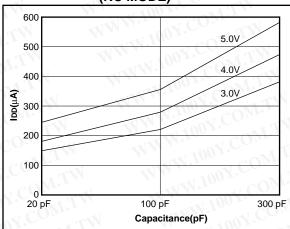


TABLE 24-1: RC OSCILLATOR FREQUENCIES

Cext	Rext	Average				
Cext	Rext	Fosc @ 5V, 25°C				
22 pF	5k	4.12 MHz	± 1.4%			
W.100 r.	10k	2.35 MHz	± 1.4%			
1007	100k	268 kHz	± 1.1%			
100 pF	3.3k	1.80 MHz	± 1.0%			
MN.L	5k	1.27 MHz	± 1.0%			
WW.10	10k	688 kHz	± 1.2%			
W	100k	77.2 kHz	± 1.0%			
300 pF	3.3k	707 kHz	± 1.4%			
MMM	5k	501 kHz	± 1.2%			
WWW	10k	269 kHz	± 1.6%			
-133	100k	28.3 kHz	± 1.1%			

The percentage variation indicated here is part to part variation due to normal process distribution. The variation indicated is ± 3 standard deviation from average value for VDD = 5V.

FIGURE 24-19: TRANSCONDUCTANCE(gm)
OF HS OSCILLATOR vs. VDD

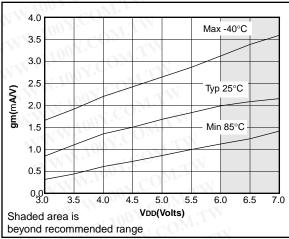


FIGURE 24-20: TRANSCONDUCTANCE(gm)
OF LP OSCILLATOR vs. VDD

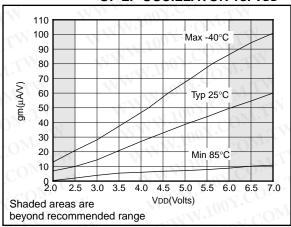


FIGURE 24-21: TRANSCONDUCTANCE(gm)
OF XT OSCILLATOR vs. VDD

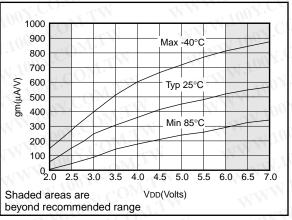


FIGURE 24-22: TYPICAL XTAL STARTUP
TIME vs. VDD (LP MODE, 25°C)

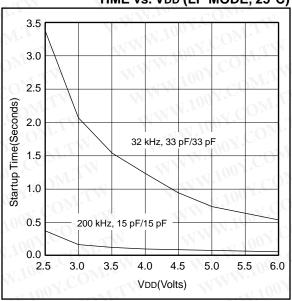
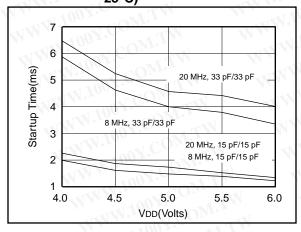


FIGURE 24-23: TYPICAL XTAL STARTUP TIME vs. VDD (HS MODE, 25°C)



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FIGURE 24-24: TYPICAL XTAL STARTUP
TIME vs. VDD (XT MODE, 25°C)

 $_{
m WW.100Y.COM.T}$

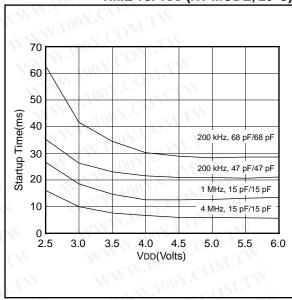


TABLE 24-2: CAPACITOR SELECTION FOR CRYSTAL OSCILLATORS

Crystal Freq	Cap. Range C1	Cap. Range C2	
32 kHz	33 pF	33 pF	
200 kHz	15 pF	15 pF	
200 kHz	47-68 pF	47-68 pF	
1 MHz	15 pF	15 pF	
4 MHz	15 pF	15 pF	
4 MHz	15 pF	15 pF	
8 MHz	15-33 pF	15-33 pF	
20 MHz	15-33 pF	15-33 pF	
WILL	MA	1007.	
OM.TV	I W	111.1001 C	
Epson C-00)1R32.768K-A	± 20 PPM	
STD XTL 2	00.000KHz	± 20 PPM	
ECS ECS-1	10-13-1	± 50 PPM	
ECS ECS-4	10-20-1	± 50 PPM	
EPSON CA	-301 8.000M-C	± 30 PPM	
EDSONICA	A-301 20.000M-C	± 30 PPM	
	Freq 32 kHz 200 kHz 200 kHz 1 MHz 4 MHz 4 MHz 20 MHz 20 MHz Epson C-00 STD XTL 20 ECS ECS-1	Freq C1 32 kHz 33 pF 200 kHz 15 pF 200 kHz 47-68 pF 1 MHz 15 pF 4 MHz 15 pF 4 MHz 15 pF 8 MHz 15-33 pF	Freq C1 C2 32 kHz 33 pF 33 pF 200 kHz 15 pF 15 pF 200 kHz 47-68 pF 47-68 pF 1 MHz 15 pF 15 pF 4 MHz 15 pF 15 pF 8 MHz 15-33 pF 15-33 pF 20 MHz 15-33 pF 15-33 pF Epson C-001R32.768K-A ± 20 PPM STD XTL 200.000KHz ± 20 PPM ECS ECS-10-13-1 ± 50 PPM ECS ECS-40-20-1 ± 50 PPM

Applicable Devices 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

FIGURE 24-25: TYPICAL IDD vs. FREQUENCY (LP MODE, 25°C)

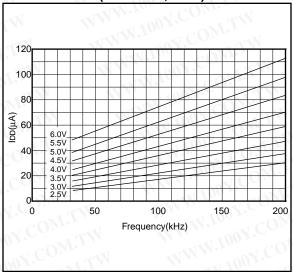


FIGURE 24-26: MAXIMUM IDD vs. FREQUENCY (LP MODE, 85°C TO -40°C)

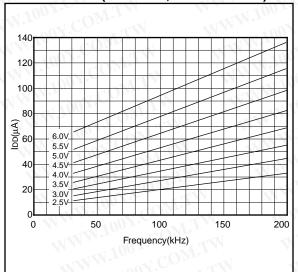


FIGURE 24-27: TYPICAL IDD vs. FREQUENCY (XT MODE, 25°C)

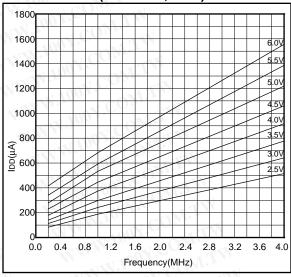
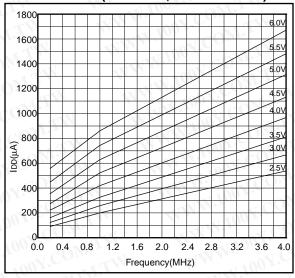


FIGURE 24-28: MAXIMUM IDD vs.
FREQUENCY
(XT MODE, -40°C TO 85°C)



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Applicable Devices 61 62 62A R62 63 R63 64 64A R64 65 65A R65 66 67

FIGURE 24-29: TYPICAL IDD vs. FREQUENCY (HS MODE, 25°C)

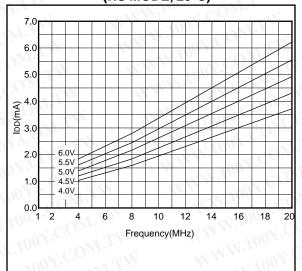
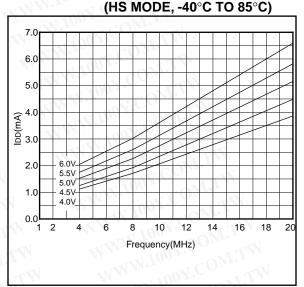


FIGURE 24-30: MAXIMUM IDD vs. FREQUENCY

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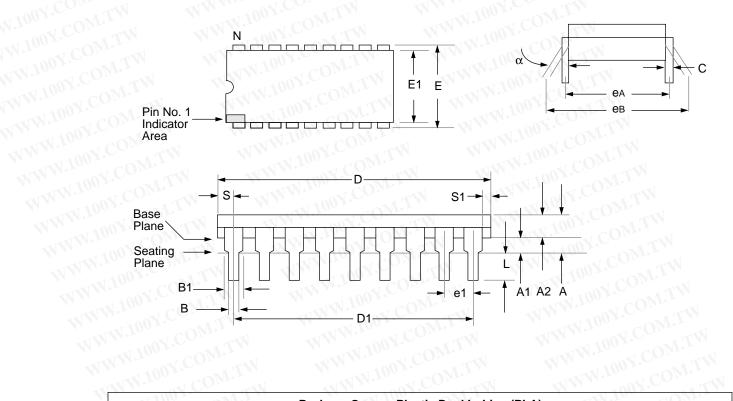
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25.0 PACKAGING INFORMATION

25.1 18-Lead Plastic Dual In-line (300 mil) (P)



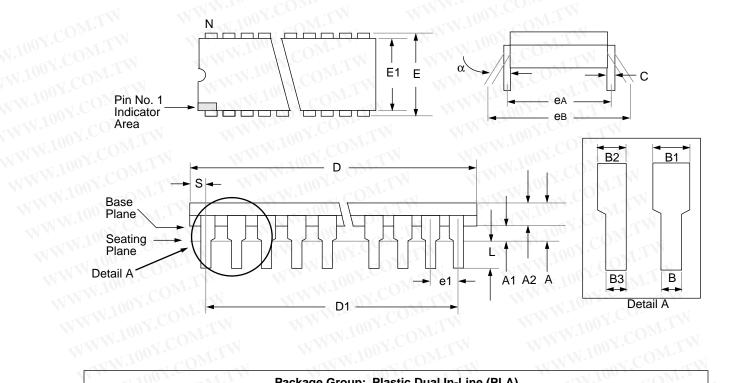
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	COM	Millimeters	M. Jos CO	I. E	Inches	OX.COM.
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°	W.100	0°	10°	CON
Α	107.0- NJ	4.064	1007.0	OM.TW	0.160	100 1.
A1	0.381	- W	WWW.	0.015	1	1100Y.
A2	3.048	3.810	TIMN.IO	0.120	0.150	V. CC
В	0.355	0.559	W.100	0.014	0.022	M.In
B1	1.524	1.524	Reference	0.060	0.060	Reference
C	0.203	0.381	Typical	0.008	0.015	Typical
D	22.479	23.495	TWW.IA	0.885	0.925	MM.
D1	20.320	20.320	Reference	0.800	0.800	Reference
E N	7.620	8.255	MW	0.300	0.325	N 1 100
E1	6.096	7.112	WWW.	0.240	0.280	MM
e1	2.489	2.591	Typical	0.098	0.102	Typical
eA	7.620	7.620	Reference	0.300	0.300	Reference
eВ	7.874	9.906		0.310	0.390	MAN
L	3.048	3.556	W W	0.120	0.140	MMM
N	18	18		18	18	
S	0.889	1007.	1111	0.035	TOM-TW	111
S1	0.127	ON COM	TW	0.005	CO TW	MA

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25.2 28-Lead Plastic Dual In-line (300 mil) (SP)



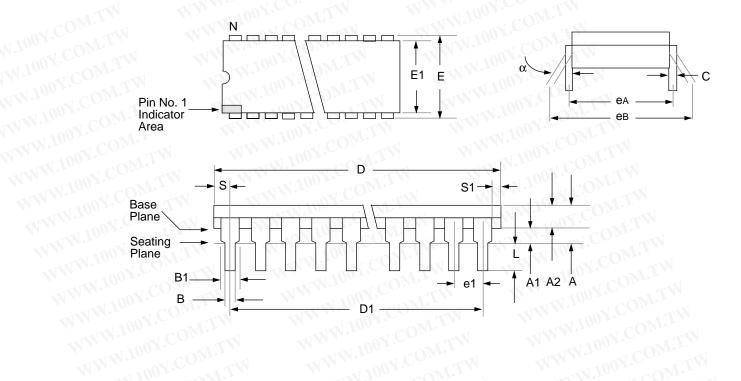
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		Package Gro	up: Plastic Dual I	n-Line (PLA)		
VIN 100	COMITW	Millimeters	M.100 F. CO.	W.L.	Inches	ON COM
ymbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°	131,100	0°	10°	1100
Α	3.632	4.572	1007	0.143	0.180	11007.
A1	0.381	- W	WWW.	0.015	-0111	A. C.
A2	3.175	3.556	INN. Ino	0.125	0.140	M. In Car
В	0.406	0.559	100	0.016	0.022	W.100
B1	1.016	1.651	Typical	0.040	0.065	Typical
B2	0.762	1.016	4 places	0.030	0.040	4 places
B3	0.203	0.508	4 places	0.008	0.020	4 places
C W	0.203	0.331	Typical	0.008	0.013	Typical
D	34.163	35.179	MMM	1.385	1.395	WWW
D1	33.020	33.020	Reference	1.300	1.300	Reference
E	7.874	8.382		0.310	0.330	TWW.
E1	7.112	7.493	4/1/	0.280	0.295	W.
e1	2.540	2.540	Typical	0.100	0.100	Typical
eA	7.874	7.874	Reference	0.310	0.310	Reference
eВ	8.128	9.652		0.320	0.380	V1
L	3.175	3.683	TW	0.125	0.145	111
N	28	28		28	28	V W
S	0.584	1.220	17.7	0.023	0.048	-17

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25.3 40-Lead Plastic Dual In-line (600 mil) (P)



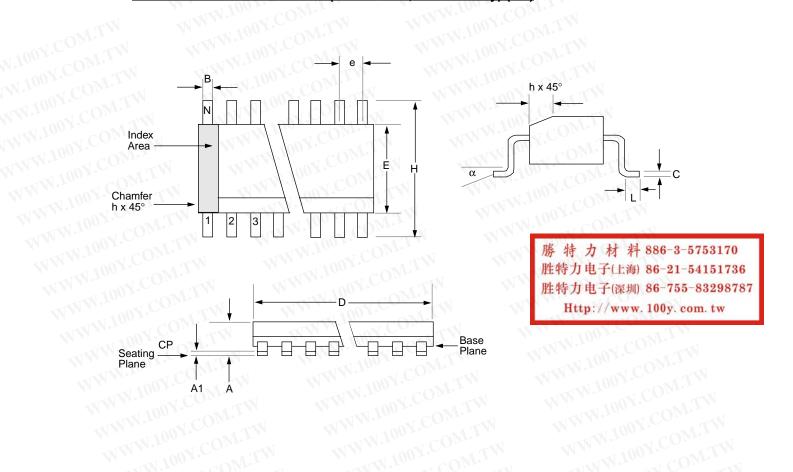
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		Package Gro	oup: Plastic Dual I	n-Line (PLA)		
W 100Y.	COM.TW	Millimeters	N.100Y.COM	IN	Inches	COMIT
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°	1007.	0°	10°	COM:
Α	V.CO.	5.080	M. JOON CO	N E T 1	0.200	100X.C
A1	0.381		INN. IN CO	0.015	12 WW	· COA.COA
A2	3.175	4.064	100 L	0.125	0.160	1.100 = 1 CO
В	0.355	0.559	MM. 100X.	0.014	0.022	11.1007.
B1	1.270	1.778	Typical	0.050	0.070	Typical
С	0.203	0.381	Typical	0.008	0.015	Typical
D	51.181	52.197	W 100	2.015	2.055	W.100
D1	48.260	48.260	Reference	1.900	1.900	Reference
E	15.240	15.875	MMN	0.600	0.625	1 1/11
E1	13.462	13.970	J.W.	0.530	0.550	TWW.IO
e1	2.489	2.591	Typical	0.098	0.102	Typical
eA	15.240	15.240	Reference	0.600	0.600	Reference
eВ	15.240	17.272	WWW	0.600	0.680	MMM
L	2.921	3.683		0.115	0.145	TAN W.
N	40	40		40	40	111
S	1.270	VA'COM	W WY	0.050	TW	MM
S1	0.508	COM.		0.020	OM.	With

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25.4 18-Lead Plastic Surface Mount (SOIC - Wide, 300 mil Body) (SO)



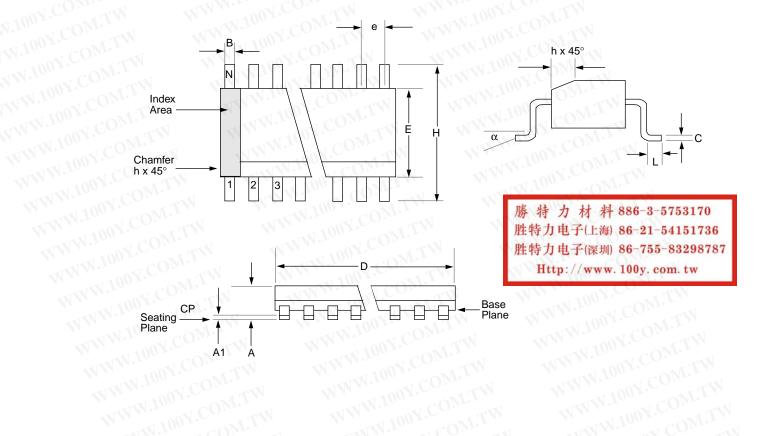
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		Package	Group: Plastic S	OIC (SO)		
WWW	·In. COM	Millimeters	WWW.	I.COM.	Inches	100 X.C
nbol	Min	Max	Notes	CMin	Max 📢	Notes
α	0°	8°	TWW.IV	0°	8°	WWW
A	2.362	2.642	-TV.1	0.093	0.104	TANN TOO
1 W	0.101	0.300		0.004	0.012	100
3	0.355	0.483	MININ	0.014	0.019	MM
	0.241	0.318	TWW.	0.009	0.013	MM
	11.353	11.735	1	0.447	0.462	W.
	7.416	7.595		0.292	0.299	1111
	1.270	1.270	Reference	0.050	0.050	Reference
	10.007	10.643		0.394	0.419	
	0.381	0.762		0.015	0.030	No.
	0.406	1.143	TW	0.016	0.045	11/11
	18	18	T. XXI	18	CO 18	I W
	7/1	0.102	M.L.	1. 100	0.004	-17

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25.5 28-Lead Plastic Surface Mount (SOIC - Wide, 300 mil Body) (SO)



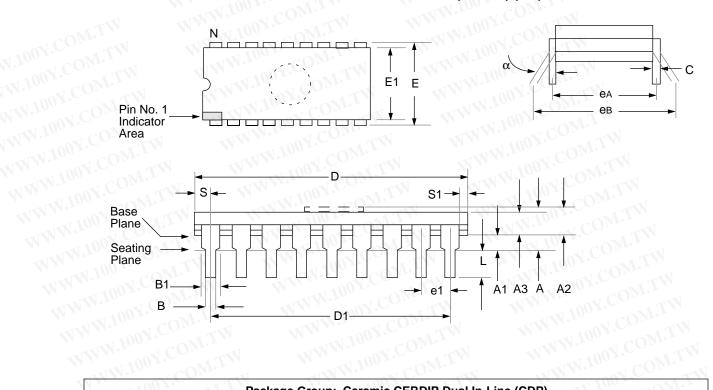
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WW.100	T COM.	Package	Group: Plastic S	SOIC (SO)	WWW.	. O.Y.COM
WW.10	COMIT	Millimeters	MM. Too.	OM.	Inches	Inc. COM
Symbol	Min	Max	Notes	Min	Max	Notes
α	0° 0°	8°	-17V.100	0°	8°	V.100
Α	2.362	2.642	WW 1005	0.093	0.104	N 100 Y
A1	0.101	0.300	MAM	0.004	0.012	100X.C
В	0.355	0.483	TIMM'IO	0.014	0.019	WW.
С	0.241	0.318	W.11	0.009	0.013	MW.Inc
D W	17.703	18.085	WW	0.697	0.712	1007
E	7.416	7.595	MMM.	0.292	0.299	NW 100
е	1.270	1.270	Typical	0.050	0.050	Typical
Н	10.007	10.643		0.394	0.419	10.10
h	0.381	0.762	MM	0.015	0.030	WW - 11
L	0.406	1.143	W.	0.016	0.045	M.M.
N	28	28	-1	28	28	
СР	11/1	0.102	M M	HOLL	0.004	11

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25.6 18-Lead Ceramic CERDIP Dual In-line with Window (300 mil) (JW)

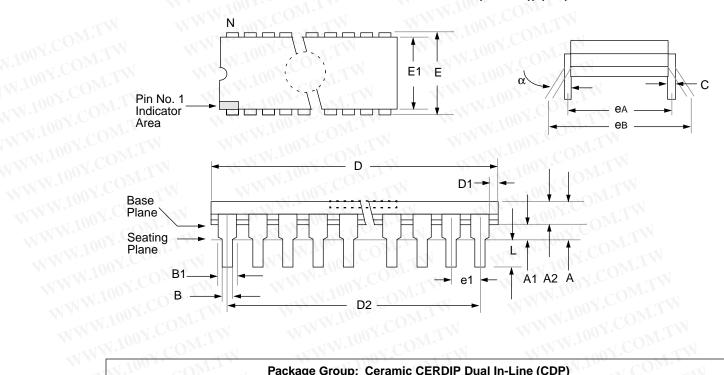


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N	CONT. FA	ckage Group.	Seramic CERDIP	Dual In-Line (CDP)				
	COM	Millimeters	VW.100 TCO	Mr.	Inches	COM.		
ymbol	Min	Max	Notes	Min	Max	Notes		
α	0°	10°	111,1001.	0°	10°	100		
Α	W.Co	5.080	1007	T.T.	0.200	11001.		
A1	0.381	1.778	WWW.	0.015	0.070	A. OUX.C.		
A2	3.810	4.699	I TOWN	0.150	0.185	M. In Car		
A3	3.810	4.445	W 100	0.150	0.175	1001		
В	0.355	0.585	WW	0.014	0.023	11003		
B1	1.270	1.651	Typical	0.050	0.065	Typical		
С	0.203	0.381	Typical	0.008	0.015	Typical		
D W	22.352	23.622		0.880	0.930	W 100		
D1 🕤	20.320	20.320	Reference	0.800	0.800	Reference		
E	7.620	8.382		0.300	0.330	WWW.		
E1	5.588	7.874	NY T	0.220	0.310	W.		
e1	2.540	2.540	Reference	0.100	0.100	Reference		
eA	7.366	8.128	Typical	0.290	0.320	Typical		
eВ	7.620	10.160		0.300	0.400			
L	3.175	3.810		0.125	0.150			
N	18	18	TW	18	18	Al A		
S	0.508	1.397		0.020	0.055	i w		
S1	0.381	1.270	T. I.	0.015	0.050	-11 -		

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25.7 28-Lead Ceramic CERDIP Dual In-line with Window (300 mil)) (JW)



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	JW:T	Millimeters	Ing COM.		Inches	COM
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°	1.100 TOM	0°	10°	COM.
A .007	3.30	5.84	N 100 Y	.130	0.230	G. CONTA
A1	0.38	-111	1001.00	0.015	M.M.	OY.COMIT
A2	2.92	4.95	M. Par CO	0.115	0.195	ON COP
B 10	0.35	0.58	W.100 x	0.014	0.023	in COM.
B1	1.14	1.78	Typical	0.045	0.070	Typical
C	0.20	0.38	Typical	0.008	0.015	Typical
D. W.	34.54	37.72	TINN TOO	1.360	1.485	M. To CO.
D2	32.97	33.07	Reference	1.298	1.302	Reference
EWW	7.62	8.25	11/11	0.300	0.325	1007.
E1	6.10	7.87	WWW.	0.240	0.310	MAL TONY CO
е	2.54	2.54	Typical	0.100	0.100	Typical
eA	7.62	7.62	Reference	0.300	0.300	Reference
eB 🕥	MAN -OX.C	11.43	MM	1001 Co	0.450	1007
L	2.92	5.08		0.115	0.200	WWW. CON
N	28	28		28	28	TWW.Io.
D1	0.13	TI		0.005	MITH	W 100

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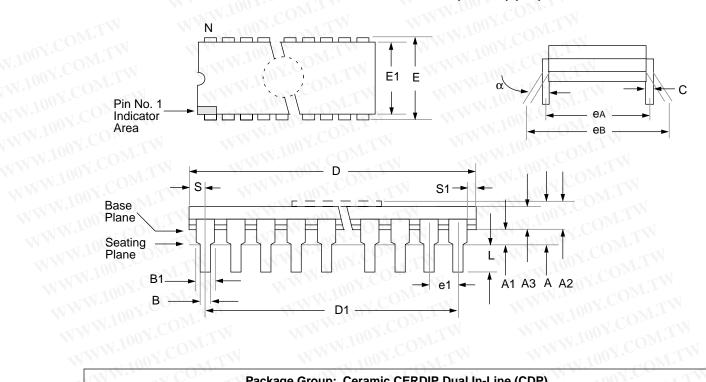
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25.8 40-Lead Ceramic CERDIP Dual In-line with Window (600 mil) (JW)



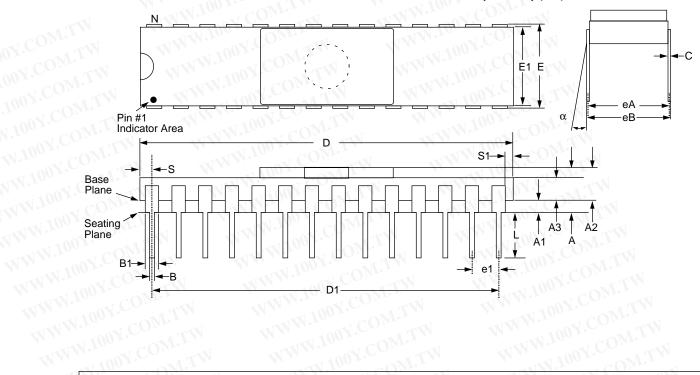
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111.		Millimeters	1100 Y.CO		Inches	
Symbol	.C Min	Max	Notes	Min	Max	Notes
α	CO°	10°	NN. OV.C	0°	10°	TOUX CO.
A	4.318	5.715	MAN Jan	0.170	0.225	N. CO
A1	0.381	1.778	100 1.	0.015	0.070	V1.100
A2	3.810	4.699	11007	0.150	0.185	N 1007.
A3	3.810	4.445	MAM	0.150	0.175	1007.0
В	0.355	0.585	TANN Too	0.014	0.023	WW.I
B1	1.270	1.651	Typical	0.050	0.065	Typical
C	0.203	0.381	Typical	0.008	0.015	Typical
D	51.435	52.705	WWW.	2.025	2.075	MAN
D1	48.260	48.260	Reference	1.900	1.900	Reference
E	15.240	15.875	W.	0.600	0.625	W.10
E1 .	12.954	15.240	MM	0.510	0.600	MM
e1	2.540	2.540	Reference	0.100	0.100	Reference
eA	14.986	16.002	Typical	0.590	0.630	Typical
eВ	15.240	18.034		0.600	0.710	N
L	3.175	3.810	W W	0.125	0.150	WW
N	40	40	· ' '	40	40	VIV
S	1.016	2.286	3.11	0.040	0.090	
S1	0.381	1.778	WT	0.015	0.070	4/1

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25.9 28-Lead Ceramic Side Brazed Dual In-Line with Window (300 mil) (JW)



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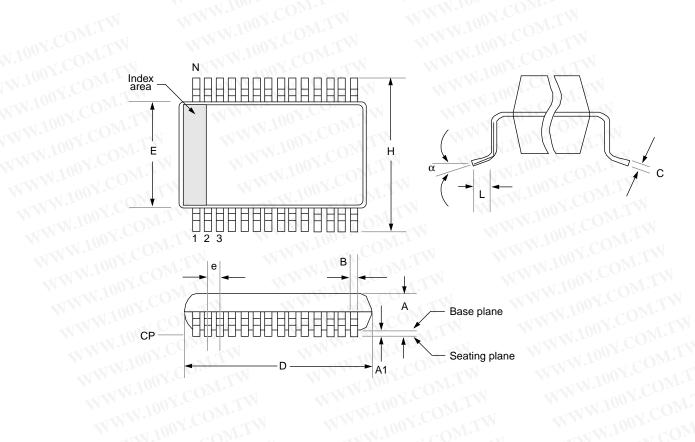
100 X.C.	Pack	age Group: Ce	ramic Side Braze	d Dual In-Line	(CER)	COM.II
. 100Y.C	WILK	Millimeters	100 Y. CON.		Inches	T.MOD
symbol	Min	Max	Notes	Min	Max	Notes
α	0° N	10°	. O.Y.Co.	0°	10°	V.C.
A 100	3.937	5.030	W. Too	0.155	0.198	COM
A1 100	1.016	1.524	W.100 F.	0.040	0.060	COM
A2	2.921	3.506	1007.0	0.115	0.138	100 J.
A3	1.930	2.388	WW.	0.076	0.094	TOUX:CO.
В	0.406	0.508	TANN. TOO	0.016	0.020	CO
B1	1.219	1.321	Typical	0.048	0.052	N.100 . CO
C	0.228	0.305	Typical	0.009	0.012	1007.
D	35.204	35.916	WWW.	1.386	1.414	M. C.
D1	32.893	33.147	Reference	1.295	1.305	WW.Inc
E	7.620	8.128	7/1/10	0.300	0.320	-1XV.100 1.
E1	7.366	7.620	MM	0.290	0.300	1007
e1	2.413	2.667	Typical	0.095	0.105	WWW.
eA	7.366	7.874	Reference	0.290	0.310	, TANN Joo
еВ	7.594	8.179	MM.	0.299	0.322	W 10
L	3.302	4.064	MAN	0.130	0.160	MAN
N	28	28	N T	28	28	TANN.
S	1.143	1.397		0.045	0.055	Wire
S1	0.533	0.737	M MM	0.021	0.029	1/1/1

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25.10 28-Lead Plastic Surface Mount (SSOP - 209 mil Body 5.30 mm) (SS)



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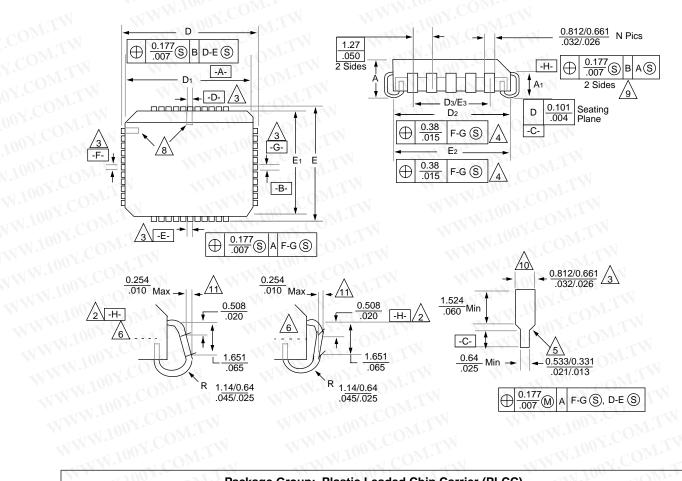
		Packa	ge Group: Plastic	SSOP		
W TANK	1001. COM	Millimeters	W. Too	COM	Inches	AM. Ino
mbol	Min Min	Max	Notes	Min	Max	Notes
α	0°	8°	W.10	0°	8°	M.100
A 1	1.730	1.990	11/1	0.068	0.078	N 100
A1 💉	0.050	0.210	MM	0.002	0.008	100
3	0.250	0.380		0.010	0.015	WWW.
C	0.130	0.220	V	0.005	0.009	LINW.II
D	10.070	10.330	1/1/1	0.396	0.407	1
E	5.200	5.380	WW	0.205	0.212	MM
е	0.650	0.650	Reference	0.026	0.026	Reference
Н	7.650	7.900	10	0.301	0.311	
L	0.550	0.950	TV V	0.022	0.037	1111
N	28	28		28	28	WW
CP CP	1	0.102	1.7	TOO.	0.004	iT -=17

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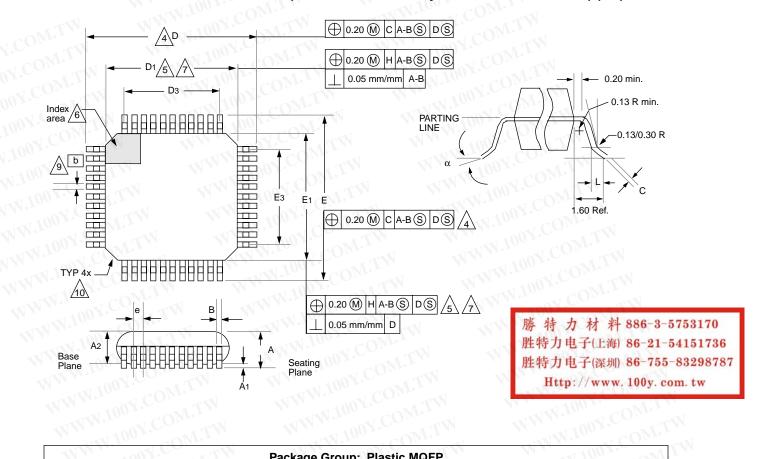
25.11 44-Lead Plastic Leaded Chip Carrier (Square) (PLCC)



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	Pa	ckage Group:	Plastic Leaded Ch	nip Carrier (PLC	cc)	
W.10	DY. COM.T.	Millimeters	N. 100 1.	OWLI	Inches	Too Y.COM
Symbol	Min	Max	Notes	Min	Max	Notes
Α	4.191	4.572	W. 100x	0.165	0.180	W.100 - CC
A1	2.413	2.921	11003	0.095	0.115	W 1007.
D	17.399	17.653	WWW.	0.685	0.695	VI TOON.C
D1	16.510	16.663	INW.Io.	0.650	0.656	WW. POW
D2	15.494	16.002	W 10	0.610	0.630	WW.100
D3	12.700	12.700	Reference	0.500	0.500	Reference
E	17.399	17.653	WWW.	0.685	0.695	MANA
E1	16.510	16.663	WW	0.650	0.656	-AIMM.To.
E2	15.494	16.002	N. V.	0.610	0.630	W.10
E3	12.700	12.700	Reference	0.500	0.500	Reference
N	44	44	W W	44	44	MAN
CP	- 10'	0.102		W.110	0.004	WW
LT	0.203	0.381	W W	0.008	0.015	W.

25.12 44-Lead Plastic Surface Mount (MQFP 10x10 mm Body 1.6/0.15 mm Lead Form) (PQ)

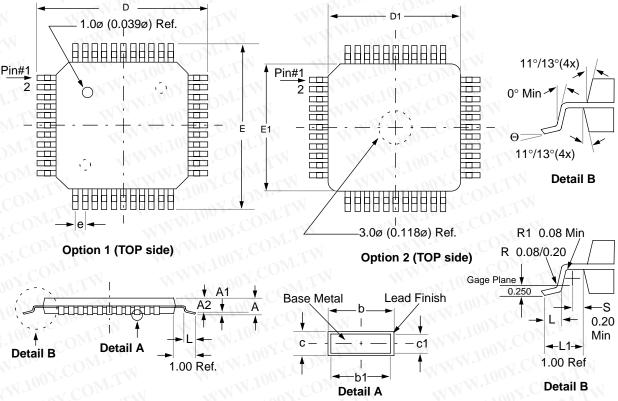


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MM		Millimeters	1007.		Inches	
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	7°	WW 100	0°	7°	100 Y.
A	2.000	2.350	WWW	0.078	0.093	1007
A1	0.050	0.250	M.In	0.002	0.010	WW.
A2	1.950	2.100	W	0.768	0.083	100 I
b W	0.300	0.450	Typical	0.011	0.018	Typical
С	0.150	0.180	MW.	0.006	0.007	MM
D	12.950	13.450		0.510	0.530	T.WW.L
D1	9.900	10.100	W.	0.390	0.398	TIN.
D3	8.000	8.000	Reference	0.315	0.315	Reference
Е	12.950	13.450	N WY	0.510	0.530	WWW
E1	9.900	10.100		0.390	0.398	
E3	8.000	8.000	Reference	0.315	0.315	Reference
е	0.800	0.800	TW V	0.031	0.032	MA
L	0.730	1.030		0.028	0.041	J W
N	44	110044	1.1.	44	44	
СР	0.102	100-11-00	WT	0.004	7. 1. T	1

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25.13 44-Lead Plastic Surface Mount (TQFP 10x10 mm Body 1.0/0.10 mm Lead Form) (TQ)



1007	WT.Mor	Packag	e Group: Plas	tic TQFP	W 100	COM	
100	I.CO. TV	Millimeters	W.100Y.	Inches			
Symbol	Min	Max	Notes	Min	Max	Notes	
Α	1.00	1.20	1007.	0.039	0.047	1007.	
A1	0.05	0.15	WW. DOW	0.002	0.006	OUN.Co	
A2	0.95	1.05		0.037	0.041	Tro-	
D	11.75	12.25	W " 100	0.463	0.482	W.100 r.	
D1	9.90	10.10	MM	0.390	0.398	1007	
E	11.75	12.25	WW.I	0.463	0.482	W.	
E1	9.90	10.10	V. 1	0.390	0.398	M.Ino.	
L	0.45	0.75	MAL	0.018	0.030	100	
е	0.80	BSC	MM	0.03	1 BSC	NW TO	
b	0.30	0.45		0.012	0.018	TANNA . I	
b1	0.30	0.40	N ·	0.012	0.016	TATIVI.	
С	0.09	0.20	MIN	0.004	0.008	WW	
c1	0.09	0.16		0.004	0.006	MM	
N	44	44	41	44	44	WW	
Θ	0°	7°	n n	0°	7°	1	

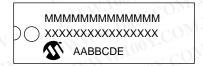
- Note 1: Dimensions D1 and E1 do not include mold protrusion. Allowable mold protrusion is 0.25m/m (0.010") per side. D1 and E1 dimensions including mold mismatch.
 - 2: Dimension "b" does not include Dambar protrusion, allowable Dambar protrusion shall be 0.08m/m (0.003")max.
 - 3: This outline conforms to JEDEC MS-026.

25.14 Package Marking Information

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18-Lead PDIP



Example



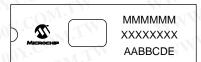
18-Lead SOIC



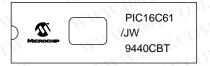
Example



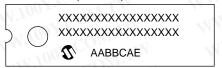
18-Lead CERDIP Windowed



Example



28-Lead PDIP (.300 MIL)



Example



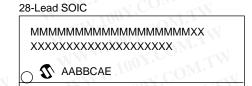
Legend:	MMM	Microchip part number information	
	XXX	Customer specific information*	
	AA	Year code (last 2 digits of calender year)	
	BB	Week code (week of January 1 is week '01')	
	M. 6	Facility code of the plant at which wafer is manufactured. C = Chandler, Arizona, U.S.A. S = Tempe, Arizona, U.S.A.	
	D ₁	Mask revision number for microcontroller	
	D_2	Mask revision number for EEPROM	
	WEN.100	Assembly code of the plant or country of origin in which part was assembled.	
Note:	line, it will b	t the full Microchip part number cannot be marked on one be carried over to the next line thus limiting the number of paracters for customer specific information.	N

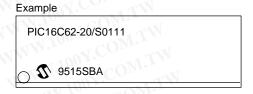
^{*} Standard OTP marking consists of Microchip part number, year code, week code, facility code, mask revision number, and assembly code. For OTP marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

Package Marking Information (Cont'd)

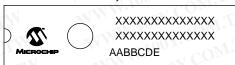
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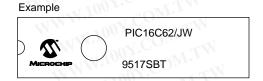
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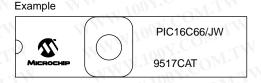




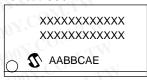


28-Lead Side Brazed Skinny Windowed











40-Lead PDIP



Example



Legend:	MMM	Microchip part number information	
	XXX	Customer specific information*	
	AA	Year code (last 2 digits of calender year)	
	BB	Week code (week of January 1 is week '01')	
	10(C).CO	Facility code of the plant at which wafer is manufactured. C = Chandler, Arizona, U.S.A. S = Tempe, Arizona, U.S.A.	
	D_1	Mask revision number for microcontroller	
	M·E	Assembly code of the plant or country of origin in which part was assembled.	
lote:	line, it will b	t the full Microchip part number cannot be marked on one be carried over to the next line thus limiting the number of characters for customer specific information.	N

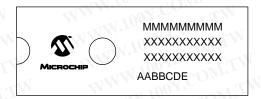
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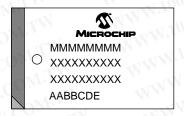
Http://www. 100y. com. tw

Package Marking Information (Cont'd)

40-Lead CERDIP Windowed



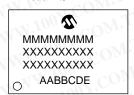
44-Lead PLCC



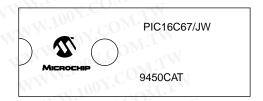
44-Lead MQFP



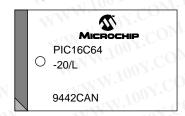
44-Lead TQFP



Example



Example



Example



Example



Legend:	MMM	Microchip part number information	M.In. COM.
	XXX	Customer specific information*	M. 100 1. COM'I
	AA	Year code (last 2 digits of calender year)	WWW.100Y.CO.T.TV
	BB	Week code (week of January 1 is week '01')	MAN'IN COM
	TW. COOX.C	Facility code of the plant at which wafer is manufactured. C = Chandler, Arizona, U.S.A. S = Tempe, Arizona, U.S.A.	NAMN:100X:COW:
	D_1	Mask revision number for microcontroller	WW. 1007.
	VWEN.100	Assembly code of the plant or country of origin in which part was assembled.	MMM. 100 X. CO.
Note:	line, it will be	the full Microchip part number cannot be marked on one e carried over to the next line thus limiting the number of aracters for customer specific information.	M.M. 100X.C.

^{*} Standard OTP marking consists of Microchip part number, year code, week code, facility code, mask revision number, and assembly code. For OTP marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

APPENDIX A: MODIFICATIONS

The following are the list of modifications over the PIC16C5X microcontroller family:

- Instruction word length is increased to 14-bits.
 This allows larger page sizes both in program memory (2K now as opposed to 512 before) and register file (128 bytes now versus 32 bytes before).
- A PC high latch register (PCLATH) is added to handle program memory paging. PA2, PA1, PA0 bits are removed from STATUS register.
- Data memory paging is redefined slightly. STA-TUS register is modified.
- Four new instructions have been added: RETURN, RETFIE, ADDLW, and SUBLW.
 Two instructions TRIS and OPTION are being phased out although they are kept for compatibility with PIC16C5X.
- OPTION and TRIS registers are made addressable.
- Interrupt capability is added. Interrupt vector is at 0004h.
- 7. Stack size is increased to 8 deep.
- 8. Reset vector is changed to 0000h.
- Reset of all registers is revisited. Five different reset (and wake-up) types are recognized. Registers are reset differently.
- Wake-up from SLEEP through interrupt is added.
- 11. Two separate timers, Oscillator Start-up Timer (OST) and Power-up Timer (PWRT), are included for more reliable power-up. These timers are invoked selectively to avoid unnecessary delays on power-up and wake-up.
- PORTB has weak pull-ups and interrupt on change feature.
- 13. Timer0 pin is also a port pin (RA4/T0CKI) now.
- 14. FSR is made a full 8-bit register.
- "In-circuit programming" is made possible. The user can program PIC16CXX devices using only five pins: VDD, Vss, VPP, RB6 (clock) and RB7 (data in/out).
- 16. Power Control register (PCON) is added with a Power-on Reset status bit (POR).(Not on the PIC16C61).
- Brown-out Reset has been added to the following devices: PIC16C62A/R62/63/R63/64A/R64/65A/R65/66/

APPENDIX B: COMPATIBILITY

To convert code written for PIC16C5X to PIC16CXX, the user should take the following steps:

- Remove any program memory page select operations (PA2, PA1, PA0 bits) for CALL, GOTO.
- Revisit any computed jump operations (write to PC or add to PC, etc.) to make sure page bits are set properly under the new scheme.
- Eliminate any data memory page switching. Redefine data variables to reallocate them.
- Verify all writes to STATUS, OPTION, and FSR registers since these have changed.
- 5. Change reset vector to 0000h.

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67.

APPENDIX C: WHAT'S NEW

Added PIC16CR63 and PIC16CR65 devices.

Added PIC16C66 and PIC16C67 devices. The PIC16C66/67 devices have 368 bytes of data memory distributed in 4 banks and 8K of program memory in 4 pages. These two devices have an enhanced SPI that supports both clock phase and polarity. The USART has been enhanced.

When upgrading to the PIC16C66/67 please note that the upper 16 bytes of data memory in banks 1,2, and 3 are mapped into bank 0. This may require relocation of data memory usage in the user application code.

Q-cycles for instruction execution were added to Section 14.0 Instruction Set Summary.

APPENDIX D: WHAT'S CHANGED

Minor changes, spelling and grammatical changes.

Divided SPI section into SPI for the PIC16C66/67 (Section 11.3) and SPI for all other devices (Section 11.2).

Added the following note for the USART. This applies to all devices except the PIC16C66 and PIC16C67.

For the PIC16C63/R63/65A/R65 the asynchronous high speed mode (BRGH = 1) may experience a high rate of receive errors. It is recommended that BRGH = 0. If you desire a higher baud rate than BRGH = 0 can support, refer to the device errata for additional information or use the PIC16C66/67.

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APPENDIX E: PIC16/17 MICROCONTROLLERS

E.1 PIC12CXXX Family of Devices

		PIC12C508	PIC12C509	PIC12C671	PIC12C672
Clock	Maximum Frequency of Operation (MHz)	4	4 V.100 Y.C	4	4
Memory	EPROM Program Memory	512 x 12	1024 x 12	1024 x 14	2048 x 14
	Data Memory (bytes)	25	41	128	128
Peripherals	Timer Module(s)	TMR0	TMR0	TMR0	TMR0
Peripherais	A/D Converter (8-bit) Channels		4111	4	4
	Wake-up from SLEEP on pin change	Yes	Yes	Yes	Yes
	I/O Pins	C 5	5	5	5
	Input Pins	10	1	1 CON	1
Features	Internal Pull-ups	Yes	Yes	Yes	Yes
	Voltage Range (Volts)	2.5-5.5	2.5-5.5	2.5-5.5	2.5-5.5
	In-Circuit Serial Programming	Yes	Yes	Yes	Yes
	Number of Instructions	33	33	35	35
	Packages	8-pin DIP, SOIC	8-pin DIP, SOIC	8-pin DIP, SOIC	8-pin DIP, SOIC

All PIC12C5XX devices have Power-on Reset, selectable Watchdog Timer, selectable code protect and high I/O current capability. All PIC12C5XX devices use serial programming with data pin GP1 and clock pin GP0.

E.2 PIC14C000 Family of Devices

		PIC14C000				
Clock	Maximum Frequency of Operation (MHz)	20 (0)				
	EPROM Program Memory (x14 words)	4K COM-				
Memory	Data Memory (bytes)	192				
ilemeny	Timer Module(s)	TMR0 ADTMR				
Peripherals	Serial Port(s) (SPI/I ² C, USART)	I ² C with SMBus Support				
Slope A/I	Slope A/D Converter Channels	8 External; 6 Internal				
	Interrupt Sources	11 V 100 - CN. IV				
	I/O Pins	22				
	Voltage Range (Volts)	2.7-6.0				
eripherals eatures	In-Circuit Serial Programming	Yes				
	Additional On-chip Features	Internal 4MHz Oscillator, Bandgap Reference, Temperature Sensor, Calibration Factors, Low Voltage Detector, SLEEP, HIBERNATE, Comparators with Programmable References (2)				
	Packages	28-pin DIP (.300 mil), SOIC, SSOP				

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E.3 PIC16C15X Family of Devices

		PIC16C154	PIC16CR154	PIC16C156	PIC16CR156	PIC16C158	PIC16CR158
Clock	Maximum Frequency of Operation (MHz)	20	20	20	20 COM.)	20	20
	EPROM Program Memory (x12 words)	512	N	1K	OX.COM.	2K	_
Memory	ROM Program Memory (x12 words)	Z.COM	512	MAN	1K	T.TW	2K
	RAM Data Memory (bytes)	25	25	25	25	73	73
Peripherals	Timer Module(s)	TMR0	TMR0	TMR0	TMR0	TMR0	TMR0
	I/O Pins	12	12	12	12	12	12
	Voltage Range (Volts)	3.0-5.5	2.5-5.5	3.0-5.5	2.5-5.5	3.0-5.5	2.5-5.5
Features	Number of Instructions	33	33	33	33	33	33
	Packages	18-pin DIP, SOIC; 20-pin SSOP					

All PIC16/17 Family devices have Power-on Reset, selectable Watchdog Timer, selectable code protect and high I/O current capability.

E.4 PIC16C5X Family of Devices

		PIC16C52	PIC16C54	PIC16C54A	PIC16CR54A	PIC16C55	PIC16C56
Clock	Maximum Frequency of Operation (MHz)	4	20 CO	20	20	20	20
	EPROM Program Memory (x12 words)	384	512	512	- WW	512	1K
Memory	ROM Program Memory (x12 words)	- 444	VN.100Y.C	WIMO	512	ZIVI.1007	COM.T
	RAM Data Memory (bytes)	25	25	25	25	24	25
Peripherals	Timer Module(s)	TMR0	TMR0	TMR0	TMR0	TMR0	TMR0
	I/O Pins	12	12	12	12	20	12
	Voltage Range (Volts)	2.5-6.25	2.5-6.25	2.0-6.25	2.0-6.25	2.5-6.25	2.5-6.25
Features	Number of Instructions	33	33	33	33	33	33
	Packages	18-pin DIP, SOIC	18-pin DIP, SOIC; 20-pin SSOP	18-pin DIP, SOIC; 20-pin SSOP	18-pin DIP, SOIC; 20-pin SSOP	28-pin DIP, SOIC, SSOP	18-pin DIP, SOIC; 20-pin SSOP

		PIC16C57	PIC16CR57B	PIC16C58A	PIC16CR58A	
Clock	Maximum Frequency of Operation (MHz)	20	20	20	20	
	EPROM Program Memory (x12 words)	2K	WW.100	2K	-WWW.10	
lemory	ROM Program Memory (x12 words)	TW	2K	ON.TW	2K	
	RAM Data Memory (bytes)	72	72	73	73	
eripherals	Timer Module(s)	TMR0	TMR0	TMR0	TMR0	
	I/O Pins	20	20	12	12	
	Voltage Range (Volts)	2.5-6.25	2.5-6.25	2.0-6.25	2.5-6.25	
eatures	Number of Instructions	33	33	33	33	
	Packages	28-pin DIP, SOIC, SSOP	28-pin DIP, SOIC, SSOP	18-pin DIP, SOIC; 20-pin SSOP	18-pin DIP, SOIC; 20-pin SSOP	

All PIC16/17 Family devices have Power-on Reset, selectable Watchdog Timer (except PIC16C52), selectable code protect and high I/O current capability.

E.5 PIC16C55X Family of Devices

		PIC16C554	PIC16C556 ⁽¹⁾	PIC16C558
Clock	Maximum Frequency of Operation (MHz)	20	20	20
Memory	EPROM Program Memory (x14 words)	512	1K	2K
welliory	Data Memory (bytes)	80	80	128
	Timer Module(s)	TMR0	TMR0	TMR0
Peripherals	Comparators(s)	- 1111	10 EX. OM. TW	_
	Internal Reference Voltage	1 - 11/11/11	TY.Com	<u> </u>
	Interrupt Sources	3	3	3
	I/O Pins	13	13	13
	Voltage Range (Volts)	2.5-6.0	2.5-6.0	2.5-6.0
eatures	Brown-out Reset	W WY	AAT. COM	4
	Packages	18-pin DIP, SOIC; 20-pin SSOP	18-pin DIP, SOIC; 20-pin SSOP	18-pin DIP, SOIC; 20-pin SSOP

All PIC16/17 Family devices have Power-on Reset, selectable Watchdog Timer, selectable code protect and high I/O current capability. All PIC16C5XX Family devices use serial programming with clock pin RB6 and data pin RB7. Note 1: Please contact your local Microchip sales office for availability of these devices.

E.6 PIC16C62X and PIC16C64X Family of Devices

		PIC16C620	PIC16C621	PIC16C622	PIC16C642	PIC16C662
Clock	Maximum Frequency of Operation (MHz)	20 CO	20	20	20 CC	20
Memory	EPROM Program Memory (x14 words)	512	1K	2K	4K	4K
	Data Memory (bytes)	80	80	128	176	176
	Timer Module(s)	TMR0	TMR0	TMR0	TMR0	TMR0
eripherals	Comparators(s)	2	2	2	2	2 0
	Internal Reference Voltage	Yes	Yes	Yes	Yes Yes	Yes
	Interrupt Sources	4	4	4	4	5
	I/O Pins	13	13	13	22	33
	Voltage Range (Volts)	2.5-6.0	2.5-6.0	2.5-6.0	3.0-6.0	3.0-6.0
	Brown-out Reset	Yes	Yes	Yes	Yes	Yes
Features	Packages	18-pin DIP, SOIC; 20-pin SSOP	18-pin DIP, SOIC; 20-pin SSOP	18-pin DIP, SOIC; 20-pin SSOP	28-pin PDIP, SOIC, Windowed CDIP	40-pin PDIP, Windowed CDIP; 44-pin PLCC, MQFP

All PIC16/17 Family devices have Power-on Reset, selectable Watchdog Timer, selectable code protect and high I/O current capability. All PIC16C62X and PIC16C64X Family devices use serial programming with clock pin RB6 and data pin RB7.

PIC16C7XX Family of Devces **E.7**

		PIC16C710	PIC16C71	PIC16C711	PIC16C715	PIC16C72	PIC16CR72 ⁽¹
Clock	Maximum Frequency of Operation (MHz)	20	20	20	20	20	20
	EPROM Program Memory (x14 words)	512	1K	1K	2K	2K	_
Memory	ROM Program Memory (14K words)	COMIT	+	WW.	ON.COM	TTW	2K
	Data Memory (bytes)	36	36	68	128	128	128
	Timer Module(s)	TMR0	TMR0	TMR0	TMR0	TMR0, TMR1, TMR2	TMR0, TMR1, TMR2
Peripherals	Capture/Compare/ PWM Module(s)	OOY.CON	T.T.M	- 444	A 100 Y	10 M.TV	1
	Serial Port(s) (SPI/I ² C, USART)	1007.CO	MIW	- 11	ZW.1007	SPI/I ² C	SPI/I ² C
	Parallel Slave Port	=100 X .	=W.TW	- 1	= 100	F. COM.	
	A/D Converter (8-bit) Channels	4	4	4	4	5	5
	Interrupt Sources	4	4	4	4	8	8
	I/O Pins	13	13	13	13	22	22
	Voltage Range (Volts)	3.0-6.0	3.0-6.0	3.0-6.0	3.0-5.5	2.5-6.0	3.0-5.5
Features	In-Circuit Serial Programming	Yes	Yes	Yes	Yes	Yes	Yes
	Brown-out Reset	Yes		Yes	Yes	Yes	Yes
	Packages	18-pin DIP, SOIC; 20-pin SSOP	18-pin DIP, SOIC	18-pin DIP, SOIC; 20-pin SSOP	18-pin DIP, SOIC; 20-pin SSOP	28-pin SDIP, SOIC, SSOP	28-pin SDIP, SOIC, SSOP

		PIC16C73A	PIC16C74A	PIC16C76	PIC16C77
ock	Maximum Frequency of Operation (MHz)	20	20	20	20
nory	EPROM Program Memory (x14 words)	4K	4K	8K	8K
	Data Memory (bytes)	192	192	368	368
	Timer Module(s)	TMR0, TMR1, TMR2	TMR0, TMR1, TMR2	TMR0, TMR1, TMR2	TMR0, TMR1, TMR2
herals	Capture/Compare/PWM Mod- ule(s)	2	2 2 100 Y.CC	2	2
	Serial Port(s) (SPI/I ² C, US-ART)	SPI/I ² C, USART	SPI/I ² C, USART	SPI/I ² C, USART	SPI/I ² C, USART
	Parallel Slave Port	£177	Yes		Yes
	A/D Converter (8-bit) Channels	5	8	5	8
	Interrupt Sources	11	12	11	12
	I/O Pins	22	33	22	33
	Voltage Range (Volts)	2.5-6.0	2.5-6.0	2.5-6.0	2.5-6.0
	In-Circuit Serial Programming	Yes	Yes	Yes	Yes
	Brown-out Reset	Yes	Yes	Yes	Yes
	Packages	28-pin SDIP, SOIC	40-pin DIP; 44-pin PLCC, MQFP, TQFP	28-pin SDIP, SOIC	40-pin DIP; 44-pin PLCC, MQFP, TQFP

E.8 PIC16C8X Family of Devices

		PIC16F83	PIC16CR83	PIC16F84	PIC16CR84
Clock	Maximum Frequency of Operation (MHz)	10	10 CO	10	10
	Flash Program Memory	512	111 TO	1K	_
	EEPROM Program Memory	<u> </u>	= 1007.	<u></u>	_
Memory	ROM Program Memory	TY TY	512		1K
	Data Memory (bytes)	36	36	68	68
	Data EEPROM (bytes)	64	64	64	64
Peripher- als	Timer Module(s)	TMR0	TMR0	TMR0	TMR0
	Interrupt Sources	4	4	4 000	4
	I/O Pins	13	13	13	13
Features	Voltage Range (Volts)	2.0-6.0	2.0-6.0	2.0-6.0	2.0-6.0
	Packages	18-pin DIP, SOIC	18-pin DIP, SOIC	18-pin DIP, SOIC	18-pin DIP, SOIC

All PIC16/17 Family devices have Power-on Reset, selectable Watchdog Timer, selectable code protect and high I/O current capability. All PIC16C8X Family devices use serial programming with clock pin RB6 and data pin RB7.

E.9 PIC16C9XX Family Of Devices

		PIC16C923	PIC16C924
Clock	Maximum Frequency of Operation (MHz)	OMP. 8	8 COM
Managara	EPROM Program Memory	4K	4K
Memory	Data Memory (bytes)	176	176
	Timer Module(s)	TMR0, TMR1, TMR2	TMR0, TMR1, TMR2
	Capture/Compare/PWM Module(s)	V COI	VIN. SOV. COM
Peripherals	Serial Port(s) (SPI/I ² C, USART)	SPI/I ² C	SPI/I ² C
	Parallel Slave Port	CONTRACTOR	AM. COm
	A/D Converter (8-bit) Channels	100 - OW. r.	5
	LCD Module	4 Com, 32 Seg	4 Com, 32 Seg
	Interrupt Sources	N.10/8	9
	I/O Pins	25	25
	Input Pins	27	27
	Voltage Range (Volts)	3.0-6.0	3.0-6.0
eatures	In-Circuit Serial Programming	Yes	Yes
	Brown-out Reset	TWO TOO TO THE	- WW 1007
	Packages	64-pin SDIP ⁽¹⁾ , TQFP; 68-pin PLCC, Die	64-pin SDIP ⁽¹⁾ , TQFP; 68-pin PLCC, Die

All PIC16/17 Family devices have Power-on Reset, selectable Watchdog Timer, selectable code protect and high I/O current capability. All PIC16C9XX Family devices use serial programming with clock pin RB6 and data pin RB7.

E.10 **PIC17CXXX Family of Devices**

		PIC17C42A	PIC17CR42	PIC17C43	PIC17CR43	PIC17C44
Clock	Maximum Frequency of Operation (MHz)	33	33	33 CO	33	33
0	EPROM Program Memory (words)	2K	- "	4K	M.TW	8K
Memory	ROM Program Memory (words)	COMITY	2K	W.100Y.C	4K	_
	RAM Data Memory (bytes)	232	232	454	454	454
Peripherals	Timer Module(s)	TMR0, TMR1, TMR2, TMR3	TMR0, TMR1, TMR2, TMR3	TMR0, TMR1, TMR2, TMR3	TMR0, TMR1, TMR2, TMR3	TMR0, TMR1, TMR2, TMR3
	Captures/PWM Module(s)	2	2	2	2	2
	Serial Port(s) (USART)	Yes	Yes	Yes	Yes	Yes
	Hardware Multiply	Yes	Yes	Yes	Yes	Yes
	External Interrupts	Yes	Yes	Yes	Yes	Yes
	Interrupt Sources	11	11	11	1100	11
	I/O Pins	33	33	33	33	33
Features	Voltage Range (Volts)	2.5-6.0	2.5-6.0	2.5-6.0	2.5-6.0	2.5-6.0
	Number of Instructions	58	58	58	58	58
	Packages	40-pin DIP; 44-pin PLCC, MQFP, TQFP				
				•		

		PIC17C752	PIC17C756
Clock	Maximum Frequency of Operation (MHz)	33	33 CON
	EPROM Program Memory (words)	8K	16K
Memory	ROM Program Memory (words)	- 777	M.1007.C
	RAM Data Memory (bytes)	454	902
Peripherals	Timer Module(s)	TMR0, TMR1, TMR2, TMR3	TMR0, TMR1, TMR2, TMR3
	Captures/PWM Module(s)	4/3	4/3
	Serial Port(s) (USART)	2	2
	Hardware Multiply	Yes	Yes
	External Interrupts	Yes	Yes
	Interrupt Sources	18	18
	I/O Pins	50	50
Features	Voltage Range (Volts)	3.0-6.0	3.0-6.0
	Number of Instructions	58	58
	Packages	64-pin DIP; 68-pin LCC, 68-pin TQFP	64-pin DIP; 68-pin LCC, 68-pin TQFP

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All PIC16/17 Family devices have Power-on Reset, selectable Watchdog Timer, selectable code protect and high WWW.100Y.COM.T I/O current capability.

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PIN COMPATIBILITY

Devices that have the same package type and VDD, Vss and MCLR pin locations are said to be pin compatible. This allows these different devices to operate in the same socket. Compatible devices may only requires minor software modification to allow proper operation in the application socket (ex., PIC16C56 and PIC16C61 devices). Not all devices in the same package size are pin compatible; for example, the PIC16C62 is compatible with the PIC16C63, but not the PIC16C55.

Pin compatibility does not mean that the devices offer the same features. As an example, the PIC16C54 is pin compatible with the PIC16C71, but does not have an A/D converter, weak pull-ups on PORTB, or interrupts.

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WWW.100Y.C **TABLE E-1:** PIN COMPATIBLE DEVICES

Pin Compatible Devices	Package	
PIC12C508, PIC12C509, PIC12C671, PIC12C672	8-pin	
PIC16C154, PIC16CR154, PIC16C156, PIC16CR156, PIC16C158, PIC16CR158, PIC16C52, PIC16C54, PIC16C54A, PIC16C56, PIC16C58A, PIC16CR58A, PIC16C61, PIC16C554, PIC16C556, PIC16C558 PIC16C620, PIC16C621, PIC16C622 PIC16C641, PIC16C642, PIC16C661, PIC16C662 PIC16C710, PIC16C71, PIC16C711, PIC16C715 PIC16F83, PIC16CR83, PIC16F84A, PIC16CR84	18-pin, 20-pin	
PIC16C55, PIC16C57, PIC16CR57B	28-pin	
PIC16CR62, PIC16C62A, PIC16C63, PIC16CR63, PIC16C66, PIC16C72, PIC16C73A, PIC16C76	28-pin	
PIC16CR64, PIC16C64A, PIC16C65A, PIC16CR65, PIC16C67, PIC16C74A, PIC16C77	40-pin	
PIC17CR42, PIC17C42A, PIC17C43, PIC17CR43, PIC17C44	40-pin	
PIC16C923, PIC16C924	64/68-pin	
PIC17C756, PIC17C752	64/68-pin	

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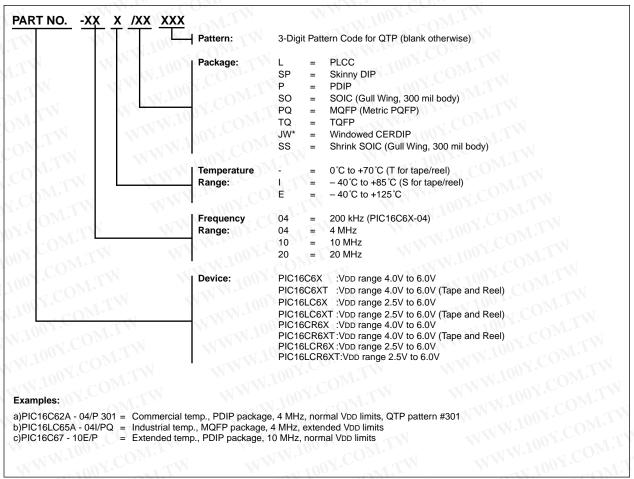
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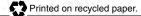
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