

ULTRA LOW CAPACITANCE TVS ARRAY
APPLICATIONS

- ✓ Ethernet - 10/100 Base T
- ✓ Cellular Phones
- ✓ FireWire
- ✓ Audio/Video Inputs
- ✓ Portable Electronics

IEC COMPATIBILITY (EN61000-4)

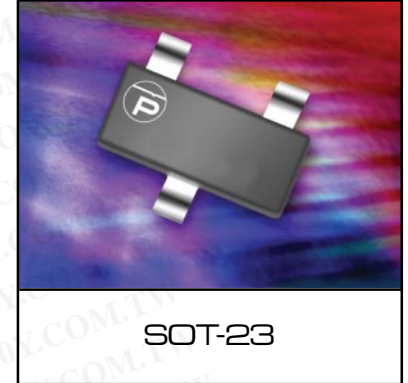
- ✓ 61000-4-2 (ESD): Air - 15kV, Contact - 8kV
- ✓ 61000-4-4 (EFT): 40A - 5/50ns
- ✓ 61000-4-5 (Surge): 12A, 8/20 μ s - Level 1(Line-Ground) & Level 2(Line-Line)

FEATURES

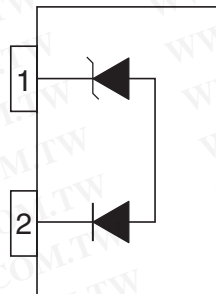
- ✓ ESD Protection > 40 kilovolts
- ✓ 500 Watts Peak Pulse Power per Line ($t_p = 8/20\mu$ s)
- ✓ Low Clamping Voltage
- ✓ Available in Multiple Voltage Types Ranging from 3V to 36V
- ✓ **ULTRA LOW CAPACITANCE: 5pF**
- ✓ RoHS Compliant in Lead-Free Versions

MECHANICAL CHARACTERISTICS

- ✓ Molded JEDEC SOT-23
- ✓ Weight 8 milligrams (Approximate)
- ✓ Available in Tin-Lead or Lead-Free Pure-Tin Plating(Annealed)
- ✓ Solder Reflow Temperature:
 - Tin-Lead - Sn/Pb, 85/15: 240-245°C
 - Pure-Tin - Sn, 100: 260-270°C
- ✓ Flammability rating UL 94V-0
- ✓ 8mm Tape and Reel Per EIA Standard 481
- ✓ Device Marking: Marking Code



勝特力材料 886-3-5753170
 勝特力电子(上海) 86-21-54151736
 勝特力电子(深圳) 86-755-83298787
[Http://www.100y.com.tw](http://www.100y.com.tw)

PIN CONFIGURATION


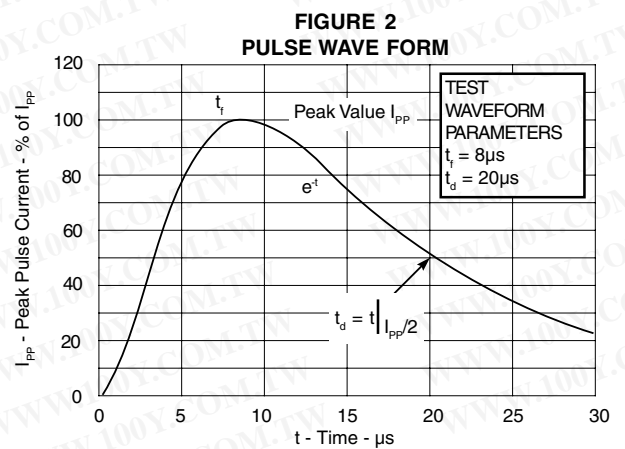
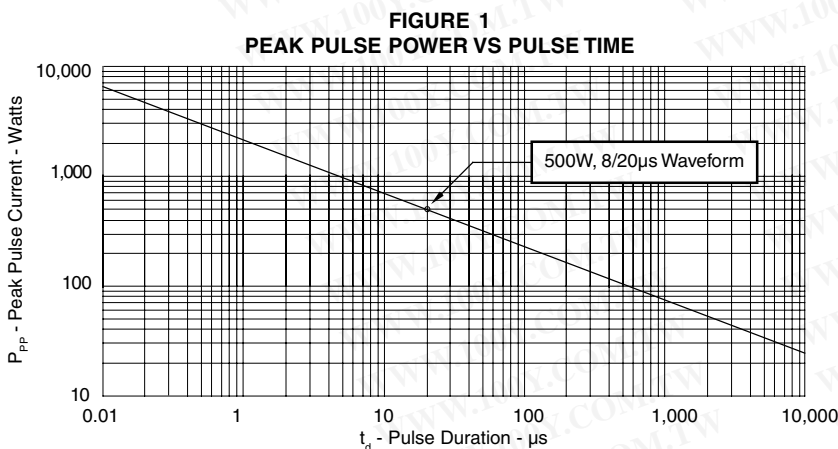
DEVICE CHARACTERISTICS

MAXIMUM RATINGS @ 25°C Unless Otherwise Specified			
PARAMETER	SYMBOL	VALUE	UNITS
Peak Pulse Power - $t_p = 8/20\mu s$ (See Figure 1)	P_{PP}	500	W
Operating Temperature	T_J	-55°C to 150°C	°C
Storage Temperature	T_{STG}	-55°C to 150°C	°C

ELECTRICAL CHARACTERISTICS PER LINE @ 25°C Unless Otherwise Specified							
PART NUMBER (Note 1)	DEVICE MARKING	RATED STAND-OFF VOLTAGE V_{WM} VOLTS	MINIMUM BREAKDOWN VOLTAGE (See Note 2) @ 1mA $V_{(BR)}$ VOLTS	MAXIMUM CLAMPING VOLTAGE (See Fig. 2) @ $I_p = 1A$ V_C VOLTS	MAXIMUM CLAMPING VOLTAGE (See Fig. 2) @ 8/20µs $V_C @ I_{PP}$	MAXIMUM LEAKAGE CURRENT @ V_{WM} I_D µA	TYPICAL CAPACITANCE @ 0V, 1 MHz C pF
PSOT05LC	05L	5.0	6.0	9.8	13.5V @ 42.0A	20	5
PSOT08LC	08L	8.0	8.5	13.4	16.9V @ 34.0A	10	5
PSOT12LC	12L	12.0	13.3	19.0	25.9V @ 21.0A	1	5
PSOT15LC	15L	15.0	16.7	24.0	30.0V @ 17.0A	1	5
PSOT24LC	24L	24.0	26.7	43.0	49.0V @ 12.0A	1	5
PSOT36LC	36L	36.0	40.0	51.0	76.8V @ 9.0A	1	5

Note 1: Positive potential is applied from pin 1 to 2; pin 2 is ground.

Note 2: Do not test or surge from pin 2 to 1. PIV typically greater than 100V for the rectifier diode.



GRAPHS

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FIGURE 3
POWER DERATING CURVE

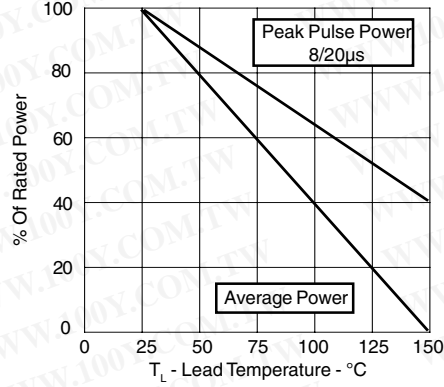
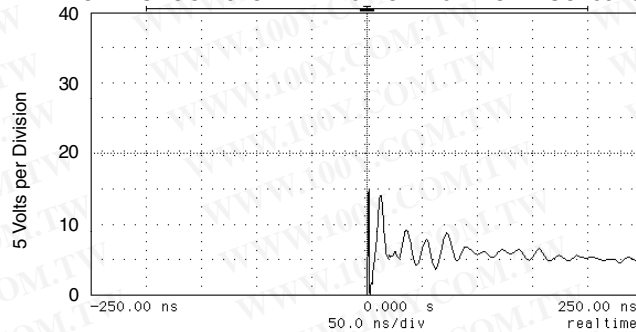
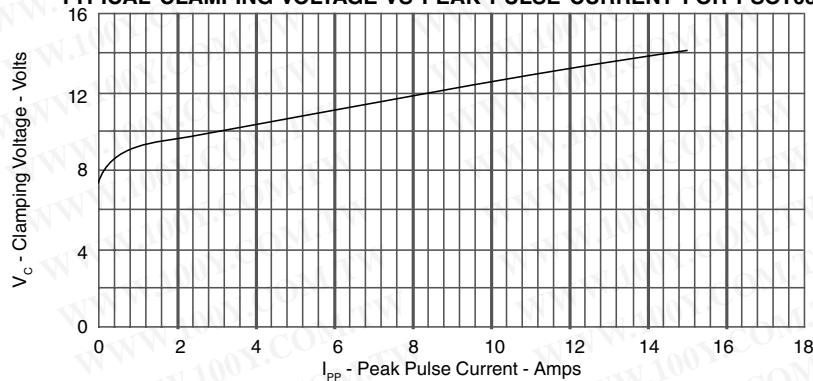


FIGURE 4
OVERSHOOT & CLAMPING VOLTAGE FOR PSOT03LC



ESD Test Pulse: 7 kilovolt, 1/30ns (waveform)

FIGURE 5
TYPICAL CLAMPING VOLTAGE VS PEAK PULSE CURRENT FOR PSOT05LC



APPLICATION NOTE

The PSOTxxLC Series are low capacitance TVS arrays designed to protect I/O or data lines from the damaging effects of ESD or EFT. This product series provides unidirectional & bidirectional protection, with a surge capability of 500 Watts P_{PP} per line for an 8/20 μ s waveform and ESD protection > 40 kilovolts.

BIDIRECTIONAL COMMON-MODE CONFIGURATION (Figure 1)

Two PSOTxxLC devices, when used in parallel, provide protection in a common-mode configuration as depicted in Figure 1.

Circuit connectivity is as follows:

- ✓ I/O Line is connected to Device 1, Pin 1.
- ✓ I/O Line is connect to Device 2, Pin 2.
- ✓ Device 1, Pin 2 is connected to ground.
- ✓ Device 2, Pin 1 is connected to ground.
- ✓ Device 1 & 2, Pin 3 is not connected.

BIDIRECTIONAL DIFFERENTIAL-MODE CONFIGURATION (Figure 1)

In addition, two PSOTxxLC devices, when used in parallel, provide protection in a differential-mode configuration for Ethernet applications as depicted in Figure 2.

Circuit connectivity is as follows:

- ✓ I/O Line 1 is connected to Device 1, Pin 1.
- ✓ I/O Line 1 is connect to Device 2, Pin 2.
- ✓ I/O Line 2 is connected to Device 1, Pin 1.
- ✓ I/O Line 2 is connect to Device 2, Pin 2.
- ✓ Device 1 & 2, Pin 3 is not connected.

CIRCUIT BOARD LAYOUT RECOMMENDATIONS

Circuit board layout is critical for Electromagnetic Compatibility (EMC) protection. The following guidelines are recommended:

- ✓ The protection device should be placed near the input terminals or connectors, the device will divert the transient current immediately before it can be coupled into the nearby traces.
- ✓ The path length between the TVS device and the protected line should be minimized.
- ✓ All conductive loops including power and ground loops should be minimized.
- ✓ The transient current return path to ground should be kept as short as possible to reduce parasitic inductance.
- ✓ Ground planes should be used whenever possible. For multilayer PCBs, use ground vias.

Figure 1 - Common-Mode I/O Port Protection

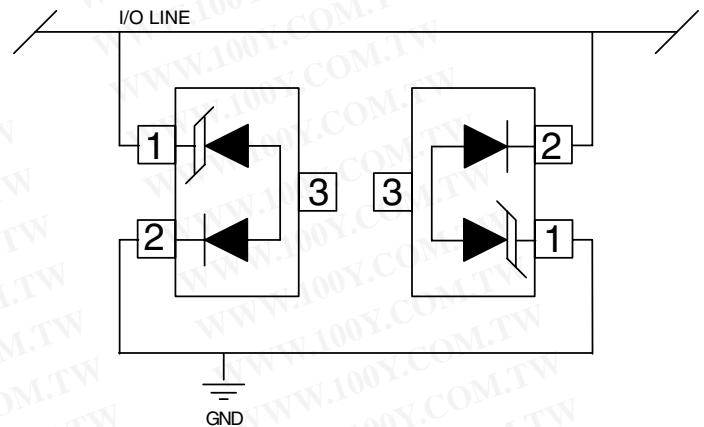
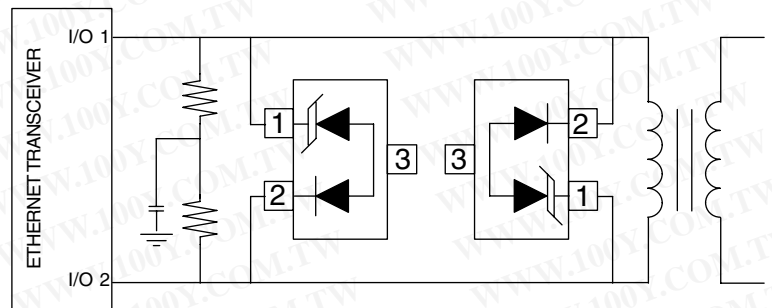
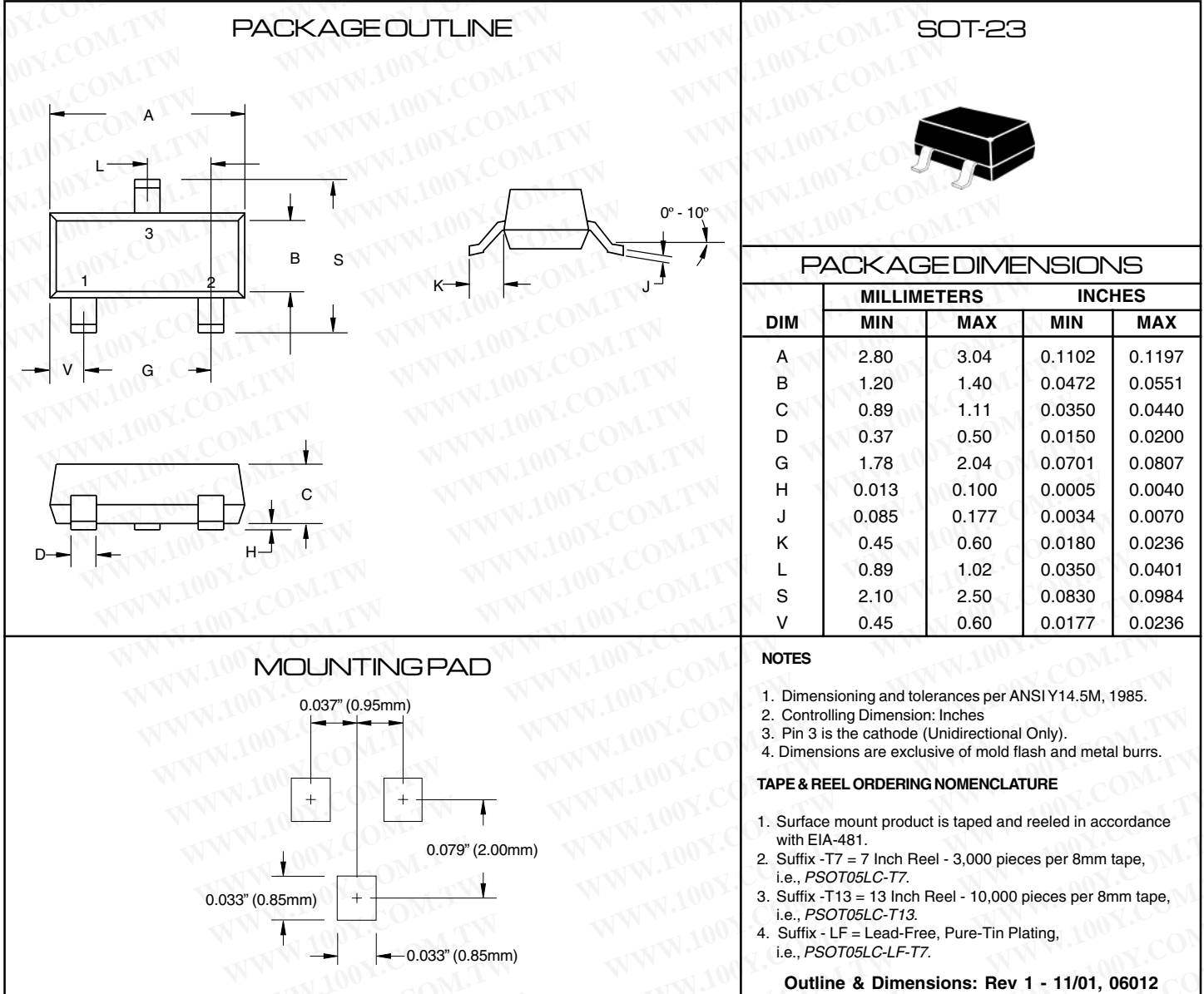


Figure 2 - Differential-Mode Ethernet Protection



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PACKAGE OUTLINE & DIMENSIONS



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