PULSE WIDTH MODULATION AMPLIFIERS

SA08

FEATURES

- IGBT OUTPUTS
- WIDE SUPPLY RANGE—16-500V
- 20A TO 100°C CASE
- 3 PROTECTION CIRCUITS
- SYNCHRONIZED OR EXTERNAL OSCILLATOR
- FLEXIBLE FREQUENCY CONTROL

APPLICATIONS

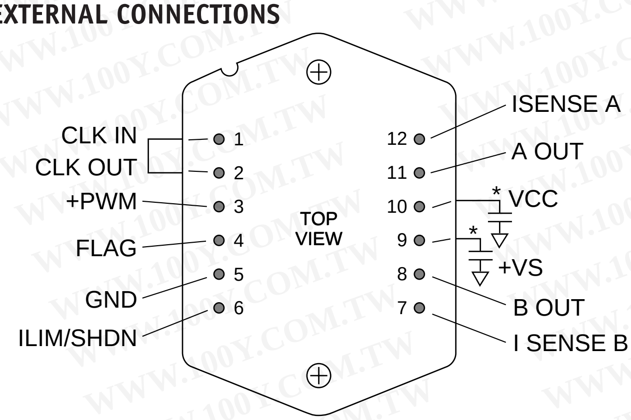
- MOTORS
- REACTIVE LOADS
- MAGNETIC BEARINGS
- LARGE PIEZO ELEMENTS
- OFF-LINE DRIVERS
- C-D WELD CONTROLLER

DESCRIPTION

The SA08 is a pulse width modulation amplifier that can supply 10KW to the load. An internal oscillator requires no external components. The clock input stage divides the oscillator frequency by two, which provides the switching frequency of 22.5 kHz. The oscillator may also be used to synchronize multiple amplifiers. Current sensing is provided for each half of the bridge giving amplitude and direction data. A shutdown input turns off all four drivers of the H-bridge output. A high side current limit and the programmable low side current limit protect the amplifier from shorts to supply or ground in addition to load shorts. The H-bridge output IGBTs are protected from thermal overloads by directly sensing the temperature of the die. The 12-pin hermetic MO-127 power package occupies only 3 square inches of board space.

12-pin Power DIP
PACKAGE STYLE CR

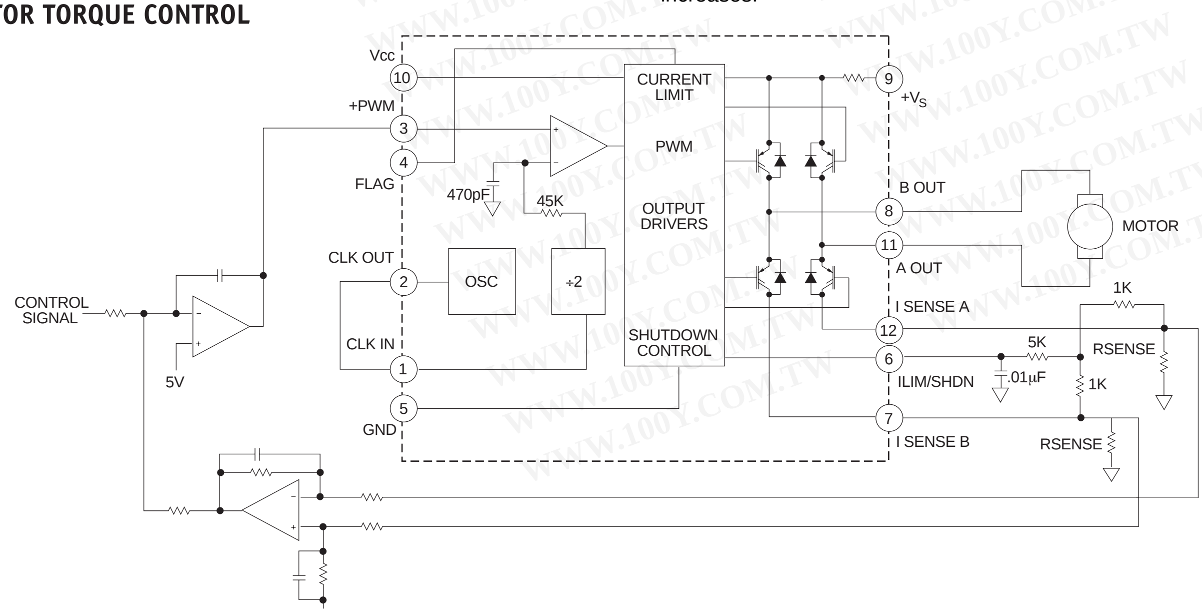
EXTERNAL CONNECTIONS



Case tied to pin 5. Allow no current in case. Bypassing of supplies is required. Package is Apex MO-127 (STD). See Outline Dimensions/Packages in Apex data book.

*See text. As +PWM goes more positive, A OUT duty cycle increases.

BLOCK DIAGRAM AND TYPICAL APPLICATION
MOTOR TORQUE CONTROL



ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$	500V
SUPPLY VOLTAGE, V_{CC}	16V
POWER DISSIPATION, internal[1]	250W
TEMPERATURE, pin solder - 10s	300°C
TEMPERATURE, junction[2]	150°C
TEMPERATURE, storage	–65 to +150°C
OPERATING TEMPERATURE RANGE, case	–55 to +125°C
INPUT VOLTAGE, +PWM	0 TO +11V
INPUT VOLTAGE, I_{LIM}	0 TO +10V

SPECIFICATIONS

PARAMETER	TEST CONDITIONS[2]	MIN	TYP	MAX	UNITS
CLOCK (CLK)					
CLK OUT, high level[4]	$I_{OUT} \leq 1mA$	4.8		5.3	V
CLK OUT, low level[4]	$I_{OUT} \leq 1mA$	0		.4	V
CLK IN, low level[4]		0		.9	V
CLK IN, high level[4]		3.7		5.4	V
FREQUENCY		44.10	45.00	46.90	kHz
ANALOG INPUT (+PWM)					
center voltage			5		V
P-P voltage	0/100% modulation		4		V
FLAG					
FLAG, high level			10		V
FLAG, low level			0		V
OUTPUT					
TOTAL DROP	I = 20A			5.4	V
EFFICIENCY, 20A output	V_S = 380V		98		%
SWITCHING FREQUENCY	OSC in ÷ 2	22.05	22.50	22.95	kHz
CURRENT, continuous[4]	100°C case	20			A
CURRENT, peak[4]		28			A
POWER SUPPLY					
VOLTAGE, V_S	Full temperature range	16[5]	240	500	V
VOLTAGE, V_{CC}	Full temperature range	14	15	16	V
CURRENT, V_{CC}	I_{OUT} = 0			80	mA
CURRENT, V_{CC}, shutdown				50	mA
CURRENT, V_S	No Load			90	mA
I_{LIM}/SHUTDOWN					
TRIP POINT		90		110	mV
INPUT CURRENT				100	nA
THERMAL[3]					
RESISTANCE, junction to case	Full temperature range, for each die			1	°C/W
RESISTANCE, junction to air	Full temperature range		12		°C/W
TEMPERATURE RANGE, case	Meets full range specifications	–25		+85	°C

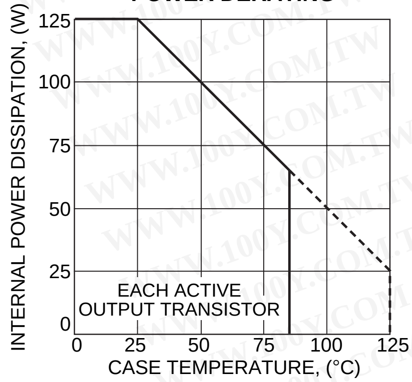
NOTES:
1. Each of the two active output transistors can dissipate 125W.
2. Unless otherwise noted: T_C = 25°C, V_S, V_{CC} at typical specification.
3. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF. For guidance, refer to the heatsink data sheet.
4. Guaranteed but not tested.
5. If 100% duty cycle is not required $V_{S(MIN)}$ = 0V.

CAUTION

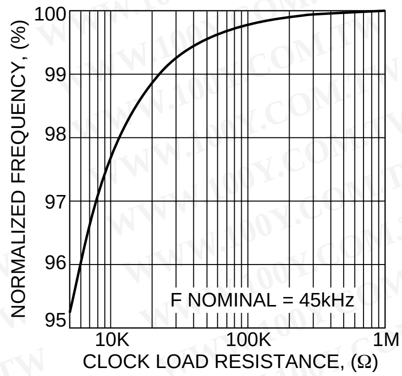
The SA08 is constructed from static sensitive components. ESD handling procedures must be observed.

The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

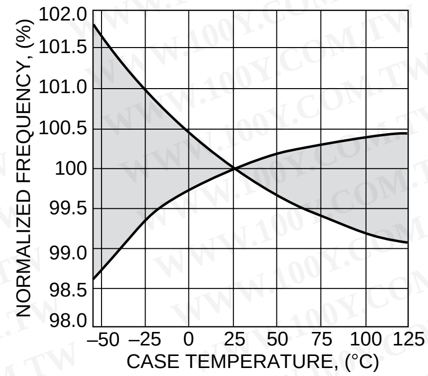
POWER DERATING



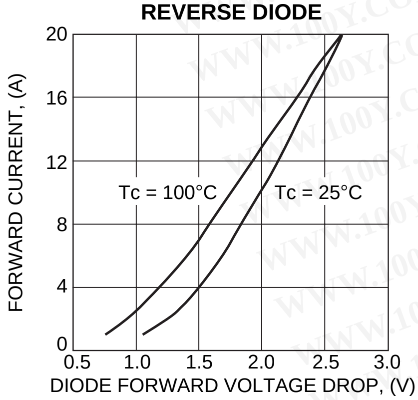
CLOCK LOADING



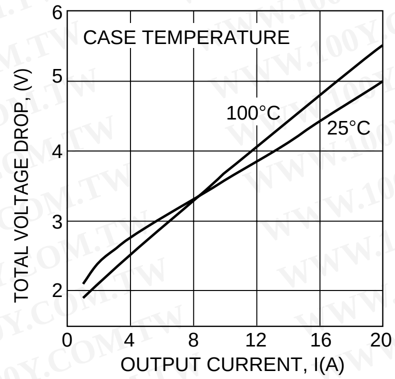
CLOCK FREQUENCY OVER TEMP



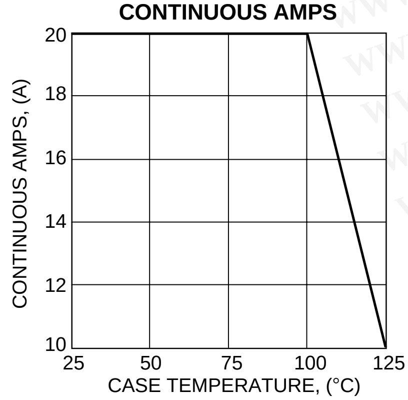
REVERSE DIODE



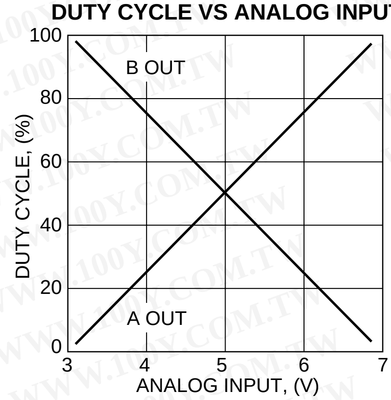
TOTAL VOLTAGE DROP



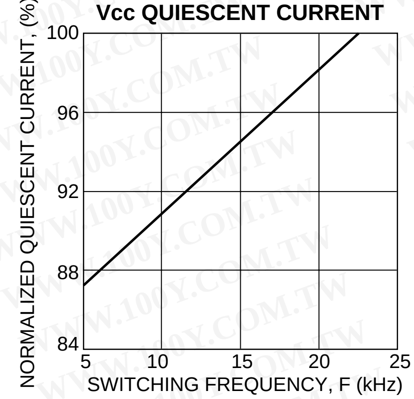
CONTINUOUS AMPS



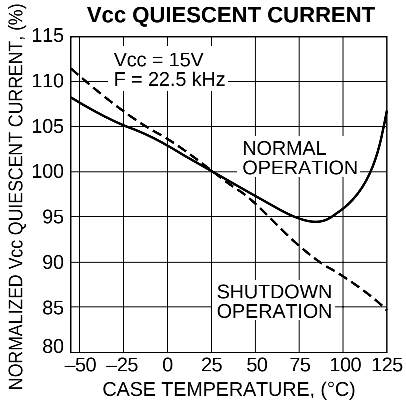
DUTY CYCLE VS ANALOG INPUT



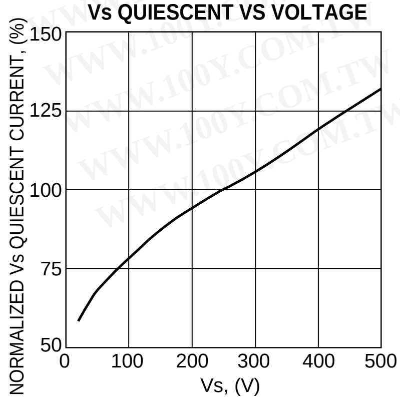
Vcc QUIESCENT CURRENT



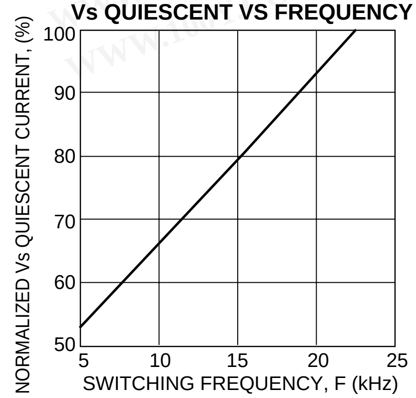
Vcc QUIESCENT CURRENT



Vs QUIESCENT VS VOLTAGE



Vs QUIESCENT VS FREQUENCY



GENERAL

Please read Application Note 30 on "PWM Basics". Refer to Application Note 1 "General Operating Considerations" for helpful information regarding power supplies, heat sinking and mounting. Visit www.apexmicrotech.com for design tools that help automate pwm filter design; heat sink selection; Apex's complete Application Notes library; Technical Seminar Workbook; and Evaluation Kits.

CLOCK CIRCUIT AND RAMP GENERATOR

The clock frequency is internally set to a frequency of approximately 45kHz. The CLK OUT pin will normally be tied to the CLK IN pin. The clock is divided by two and applied to an RC network which produces a ramp signal. An external clock signal can be applied to the CLK IN pin for synchronization purposes, but must be 45 kHz +/- 2%.

FLAG OUTPUT

Whenever the SA08 has detected a fault condition, the flag output is set high (10V). When the programmable low side current limit is exceeded, the FLAG output will be set high. The FLAG output will be reset low on the next clock cycle. This reflects the pulse-by-pulse current limiting feature. When the internally-set high side current limit is tripped or the thermal limit is reached, the FLAG output is latched high. See PROTECTION CIRCUITS below.

PROTECTION CIRCUITS

A fixed internal current limit senses the high side current. Should either of the outputs be shorted to ground the high side current limit will latch off the output transistors. The temperature of the output transistors is also monitored. Should a fault condition raise the temperature of the output transistors to 165°C the thermal protection circuit latch off the output transistors. The latched condition can be cleared by either recycling the V_{cc} power or by toggling the I LIMIT/SHDN input with a 10V pulse. See Figures A and B. The outputs will remain off as long as the shutdown pulse is high (10V).

CURRENT LIMIT

There are two load current sensing pins, I SENSE A and I SENSE B. The two pins can be shorted in the voltage mode connection but both must be used in the current mode connection (see figures A and B). It is recommended that R_{LIMIT} resistors be non-inductive. Load current flows in the I SENSE pins. To avoid errors due to lead lengths connect the I LIMIT/SHDN pin directly to the R_{LIMIT} resistors (through the filter network and shutdown divider resistor) and connect the R_{LIMIT} resistors directly to the GND pin.

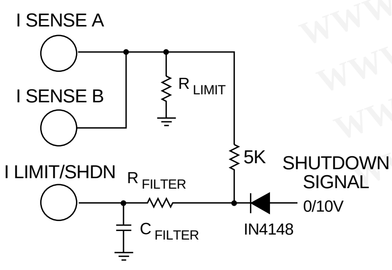


FIGURE A. CURRENT LIMIT WITH SHUTDOWN VOLTAGE MODE.

Switching noise spikes will invariably be found at the I SENSE pins. The noise spikes could trip the current limit threshold which is only 100 mV. R_{FILTER} and C_{FILTER} should be adjusted so as to reduce the switching noise well below 100 mV to prevent false current limiting. The sum of the DC level plus the noise peak will determine the current limiting value. As in most switching circuits it may be difficult to determine the true noise amplitude without careful attention to grounding of the oscilloscope probe. Use the shortest possible ground lead for the probe and connect exactly at the GND terminal of the amplifier. Suggested starting values are C_{FILTER} = .1uF, R_{FILTER} = 5k .

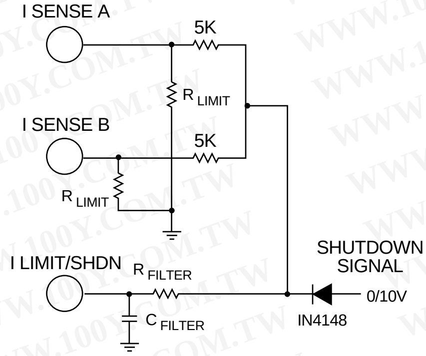


FIGURE B. CURRENT LIMIT WITH SHUTDOWN CURRENT MODE.

The required value of R_{LIMIT} in voltage mode may be calculated by:

$$R_{LIMIT} = .1\ V / I_{LIMIT}$$

where R_{LIMIT} is the required resistor value, and I_{LIMIT} is the maximum desired current. In current mode the required value of each R_{LIMIT} is 2 times this value since the sense voltage is divided down by 2 (see Figure B). If R_{SHDN} is used it will further divide down the sense voltage. The shutdown divider network will also have an effect on the filtering circuit.

BYPASSING

Adequate bypassing of the power supplies is required for proper operation. Failure to do so can cause erratic and low efficiency operation as well as excessive ringing at the outputs. The Vs supply should be bypassed with at least a 1μF ceramic capacitor in parallel with another low ESR capacitor of at least 10μF per amp of output current. Capacitor types rated for switching applications are the only types that should be considered. The bypass capacitors must be physically connected directly to the power supply pins. Even one inch of lead length will cause excessive ringing at the outputs. This is due to the very fast switching times and the inductance of the lead connection. The bypassing requirements of the Vcc supply are less stringent, but still necessary. A .1μF to .47μF ceramic capacitor connected directly to the Vcc pin will suffice.

STARTUP CONDITIONS

The high side of the IGBT output bridge circuit is driven by bootstrap circuit and charge pump arrangement. In order for the circuit to produce a 100% duty cycle indefinitely the low side of each half bridge circuit must have previously been in the ON condition. This means, in turn, that if the input signal to the SA08 at startup is demanding a 100% duty cycle, the output may not follow the command and may be in a tri-state condition. The ramp signal must cross the input signal at some point to correctly determine the output state. After the ramp crosses the input signal level one time, the output state will be correct thereafter.