SA18

FEATURES

- HALF BRIDGE IGBT OUTPUT
- WIDE SUPPLY RANGE—16-500V
- 20A TO 100° C CASE
- 3 PROTECTION CIRCUITS
- SYNCHRONIZED OR EXTERNAL OSCILLATOR
- FLEXIBLE FREQUENCY CONTROL

APPLICATIONS

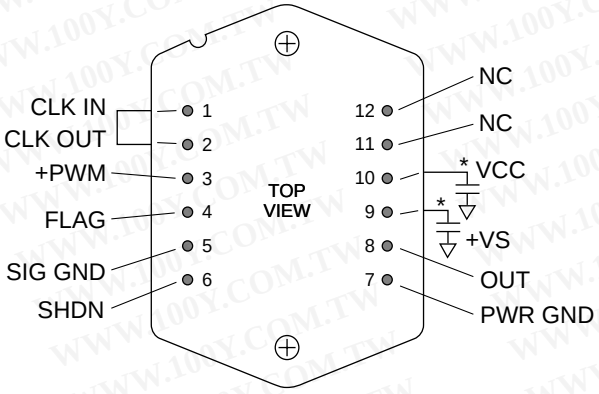
- MOTORS
- REACTIVE LOADS
- LOW FREQUENCY SONAR
- LARGE PIEZO ELEMENTS
- OFF-LINE DRIVERS
- C-D WELD CONTROLLER

12-pin Power DIP
PACKAGE STYLE CR

DESCRIPTION

The SA18 is a pulse width modulation amplifier that can supply 10KW to the load. An internal oscillator requires no external components. The clock input stage divides the oscillator frequency by two, which provides the switching frequency of 22.5 kHz. External oscillators may also be used to lower the switching frequency or to synchronize multiple amplifiers. A shutdown input turns off both drivers of the half bridge output. A high side current limit protects the amplifier from shorts to ground in addition to load shorts. The output IGBTs are protected from thermal overloads by directly sensing the temperature of the die. The 12-pin hermetic MO-127 power package occupies only 3 square inches of board space.

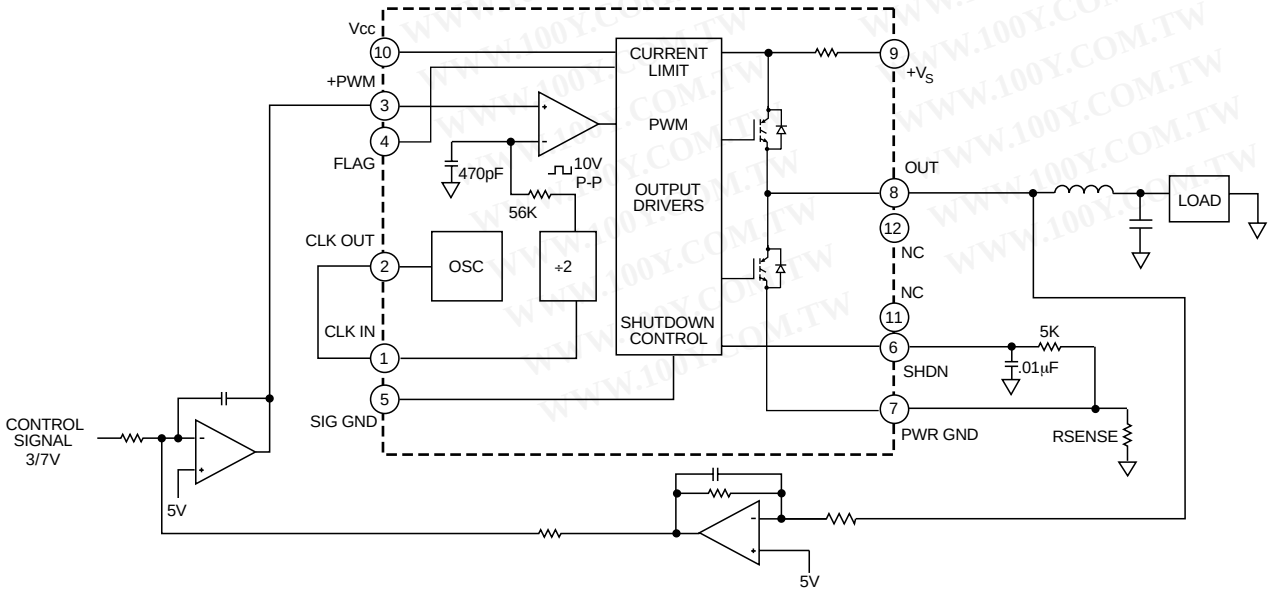
EXTERNAL CONNECTIONS



Case tied to pin 5. Allow no current in case. Bypassing of supplies is required. Package is Apex MO–127 (STD). See Outline Dimensions/Packages in Apex data book.

As +PWM goes more positive, out duty cycle increases.
*See text.

BLOCK DIAGRAM AND TYPICAL APPLICATION
VOLTAGE CONTROLLED VOLTAGE SOURCE



ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$	500V
SUPPLY VOLTAGE, V_{CC}	16V
POWER DISSIPATION, internal[1]	125W
TEMPERATURE, pin solder - 10s	300°C
TEMPERATURE, junction[2]	150°C
TEMPERATURE, storage	–65 to +150°C
OPERATING TEMPERATURE RANGE, case	–55 to +125°C
INPUT VOLTAGE, +PWM	0 TO +11V
INPUT VOLTAGE, SHDN	0 TO +11V

SPECIFICATIONS

PARAMETER	TEST CONDITIONS[2]	MIN	TYP	MAX	UNITS
CLOCK (CLK)					
CLK OUT, high level[4]	$I_{OUT} \le 1mA$	4.8		5.3	V
CLK OUT, low level[4]	$I_{OUT} \le 1mA$	0		.4	V
CLK IN, low level[4]		0		.9	V
CLK IN, high level[4]		3.7		5.4	V
FREQUENCY		44.10	45.00	45.9	kHz
ANALOG INPUT (+PWM)					
center voltage			5		V
P-P voltage	0/100% modulation		4		V
FLAG					
FLAG, high level			10		V
FLAG, low level			0		V
OUTPUT					
TOTAL DROP	I = 20A			2.7	V
EFFICIENCY, 20A output	V_S = 380V		98		%
SWITCHING FREQUENCY	OSC in ÷ 2	22.05	22.50	22.95	kHz
CURRENT, continuous[4]	100°C case	20			A
CURRENT, peak[4]		28			A
POWER SUPPLY					
VOLTAGE, V_S		15	240	500	V
VOLTAGE, V_{CC}		14	15	16	V
CURRENT, V_{CC}	I_{OUT} = 0			80	mA
CURRENT, V_{CC}, shutdown				50	mA
CURRENT, V_S	No Load			45	mA
I_{LIM}/SHUTDOWN					
TRIP POINT		90		110	mV
INPUT CURRENT				100	nA
THERMAL[3]					
RESISTANCE, junction to case				1	°C/W
RESISTANCE, junction to air			12		°C/W

NOTES: 1. Each of the two output transistors can dissipate 125W, but only one is on at any time.
2. Unless otherwise noted: T_C = 25°C, V_S, V_{CC} at typical specification.
3. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF. For guidance, refer to the heatsink data sheet.
4. Guaranteed but not tested.

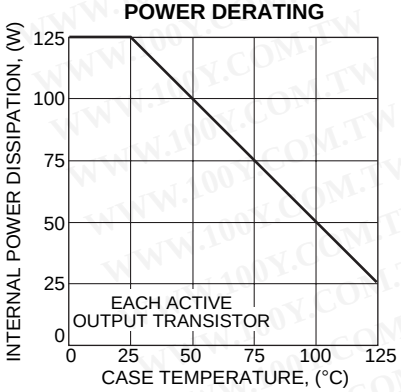
CAUTION

The SA18 is constructed from static sensitive components. ESD handling procedures must be observed.

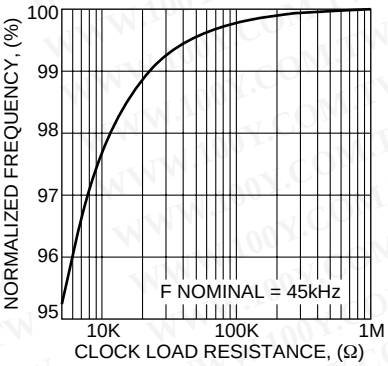
The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

TYPICAL PERFORMANCE GRAPHS

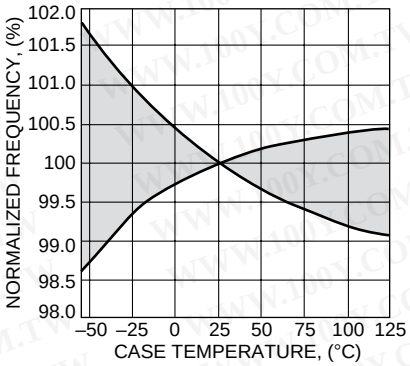
POWER DERATING



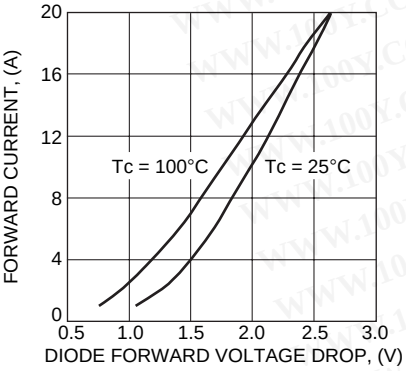
CLOCK LOADING



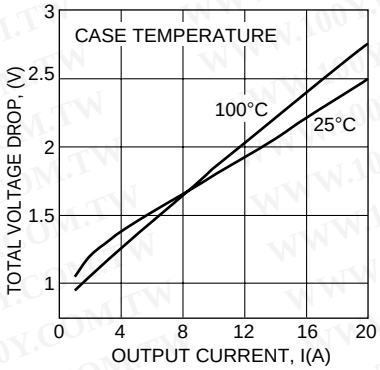
CLOCK FREQUENCY OVER TEMP



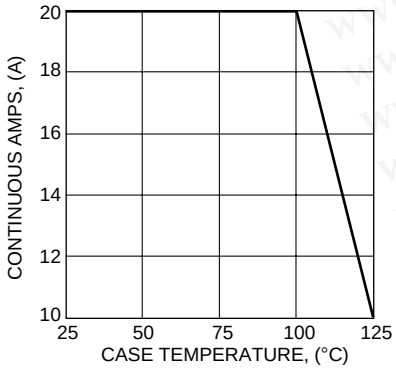
REVERSE DIODE



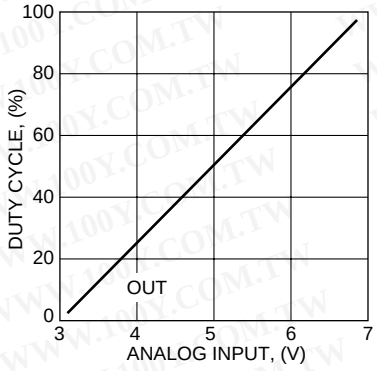
TOTAL VOLTAGE DROP



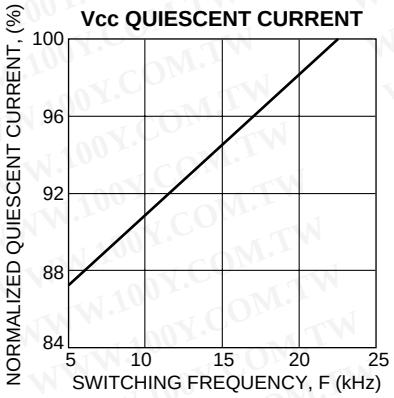
CONTINUOUS AMPS



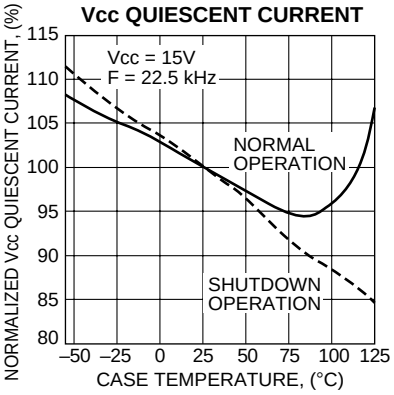
DUTY CYCLE VS ANALOG INPUT



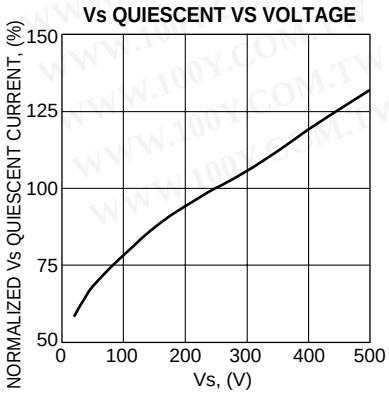
Vcc QUIESCENT CURRENT



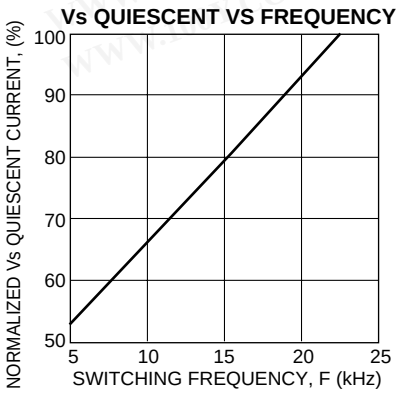
Vcc QUIESCENT CURRENT



Vs QUIESCENT VS VOLTAGE



Vs QUIESCENT VS FREQUENCY



GENERAL

Please read Application Note 30 on "PWM Basics". Refer to Application Note 1 "General Operating Considerations" for helpful information regarding power supplies, heat sinking and mounting. Visit www.apexmicrotech.com for design tools that help automate pwm filter design and heat sink selection. The "Application Notes" and "Technical Seminar" sections contain a wealth of information on specific types of applications. Information on package outlines, heat sinks, mounting hardware and other accessories are located in the "Packages and Accessories" section. Evaluation Kits are available for most Apex product models, consult the "Evaluation Kit" section for details. For the most current version of all Apex product data sheets, visit www.apexmicrotech.com.

CLOCK CIRCUIT AND RAMP GENERATOR

The clock frequency is internally set to a frequency of approximately 45kHz. The CLK OUT pin will normally be tied to the CLK IN pin. The clock is divided by two and applied to an RC network which produces a ramp signal. An external clock signal can be applied to the CLK IN pin for synchronization purposes, but must be 45 kHz +/- 2%.

FLAG OUTPUT

Whenever the SA18 has detected a fault condition, the flag output is set high (10V). When the programmable low side current limit is exceeded, the FLAG output will be set high. The FLAG output will be reset low on the next clock cycle. This reflects the pulse-by-pulse current limiting feature. When the internally-set high side current limit is tripped or the thermal limit is reached, the FLAG output is latched high. See PROTECTION CIRCUITS below.

PROTECTION CIRCUITS

A high side current monitor will latch off the output transistors when the high side current rises to approximately 150% of rated output. The temperature of the output transistors is also monitored. When either of the output transistors reaches approximately 165°C both are latched off. In either case, it will be necessary to remove the fault condition and recycle power to Vcc to restart the circuit. A short to +Vs can be protected against by inserting a sensing resistor into the PWR GND circuit as shown in Figure A.

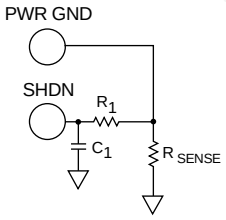


FIGURE A. PROTECTING AGAINST SHORTS TO +Vs.

In Figure A, the sense resistor inserted into the PWR GND connection is tied to the SHDN pin. When the current from a short to +Vs develops 100 mV across the sense resistor the shutdown circuit will shut off the output transistors for the remainder of the switching cycle. The SA18 will restart at the beginning of a new cycle and retest for this condition. This circuit does not test for shorts to ground. The RC circuit R_1, C_1 filters out any switching spikes and may need to be adjusted to ignore normal current spikes in the application circuit.

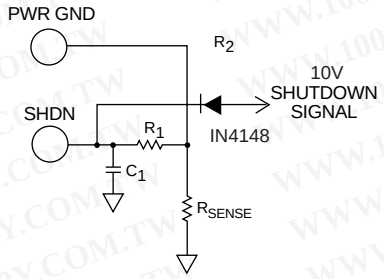


FIGURE B. ADDING SHUTDOWN CONTROL.

An external shutdown command can be mixed with the protection circuit of Figure A. In figure B a 10V shutdown command signal is injected directly into the shutdown pin (SHDN). As long as the shutdown command remains high both output transistors will remain off.

BYPASSING

Adequate bypassing of the power supplies is required for proper operation. Failure to do so can cause erratic and low efficiency operation as well as excessive ringing at the outputs. The Vs supply should be bypassed with at least a 1μF ceramic capacitor in parallel with another low ESR capacitor of at least 10μF per amp of output current. Capacitor types rated for switching applications are the only types that should be considered. The bypass capacitors must be physically connected directly to the power supply pins. Even one inch of lead length will cause excessive ringing at the outputs. This is due to the very fast switching times and the inductance of the lead connection. The bypassing requirements of the Vcc supply are less stringent, but still necessary. A .1μF to .47μF ceramic capacitor connected directly to the Vcc pin will suffice.

STARTUP CONDITIONS

The high side of the IGBT output bridge circuit is driven by bootstrap circuit and charge pump arrangement. In order for the circuit to produce a 100% duty cycle indefinitely the low side of each half bridge circuit must have previously been in the ON condition. This means, in turn, that if the input signal to the SA18 at startup is demanding a 100% duty cycle, the output may not follow the command and may be in a tri-state condition. The ramp signal must cross the input signal at some point to correctly determine the output state. After the ramp crosses the input signal level one time, the output state will be correct thereafter.