



勝特力材料 886-3-5753170
勝特力电子(上海) 86-21-54151736
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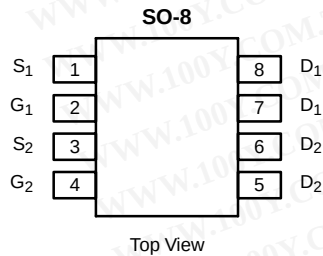
Si4980DY
Vishay Siliconix

Dual N-Channel 80-V (D-S) MOSFET

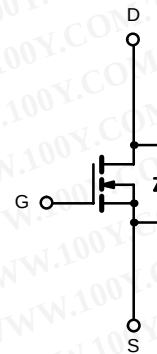
PRODUCT SUMMARY

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
80	0.075 @ $V_{GS} = 10$ V	3.7
	0.095 @ $V_{GS} = 6.0$ V	3.2

TrenchFET®
Power MOSFETs



Ordering Information: Si4980DY
Si4980DY-T1 (with Tape and Reel)



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	80	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	I_D	3.7	A
		2.9	
Pulsed Drain Current	I_{DM}	30	
Continuous Source Current (Diode Conduction) ^a	I_S	1.7	
Maximum Power Dissipation ^a	P_D	2.0	W
		1.3	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	62.5	$^\circ\text{C/W}$

Notes

a. Surface Mounted on FR4 Board, $t \leq 10$ sec.

**SPECIFICATIONS ($T_J = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	2			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}, V_{GS} = \pm 20\ \text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 80\ \text{V}, V_{GS} = 0\ \text{V}$			1	μA
		$V_{DS} = 80\ \text{V}, V_{GS} = 0\ \text{V}, T_J = 55^\circ\text{C}$			20	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} = 5\ \text{V}, V_{GS} = 10\ \text{V}$	20			A
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = 10\ \text{V}, I_D = 3.7\ \text{A}$		0.062	0.075	Ω
		$V_{GS} = 6.0\ \text{V}, I_D = 3.2\ \text{A}$		0.071	0.095	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15\ \text{V}, I_D = 3.7\ \text{A}$		12		S
Diode Forward Voltage ^a	V_{SD}	$I_S = 1.7\ \text{A}, V_{GS} = 0\ \text{V}$			1.2	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = 40\ \text{V}, V_{GS} = 10\ \text{V}, I_D = 3.7\ \text{A}$		15	30	nC
Gate-Source Charge	Q_{gs}			4		
Gate-Drain Charge	Q_{gd}			3.2		
Gate Resistance	R_g		1		5.1	Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 40\ \text{V}, R_L = 40\ \Omega$ $I_D \approx 1\ \text{A}, V_{GEN} = 10\ \text{V}, R_G = 6\ \Omega$		10	20	ns
Rise Time	t_r			10	20	
Turn-Off Delay Time	$t_{d(off)}$			30	60	
Fall Time	t_f			10	20	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 1.7\ \text{A}, di/dt = 100\ \text{A}/\mu\text{s}$		75	110	

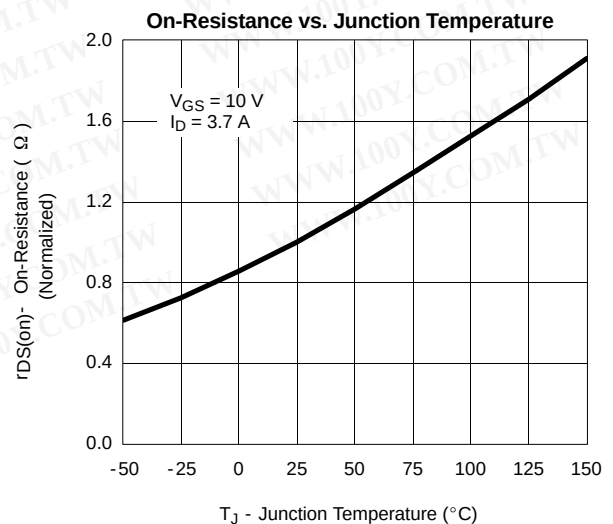
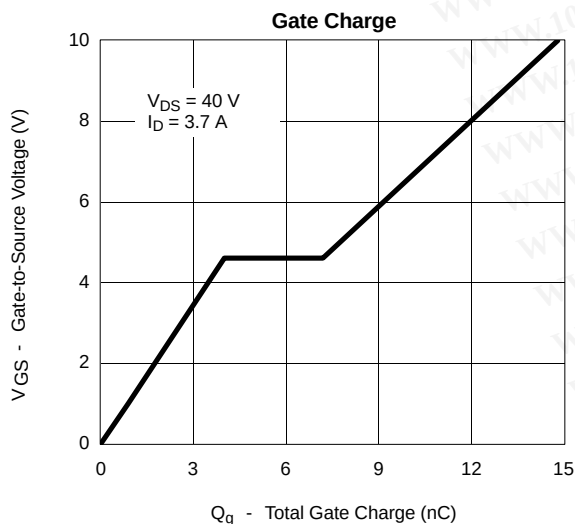
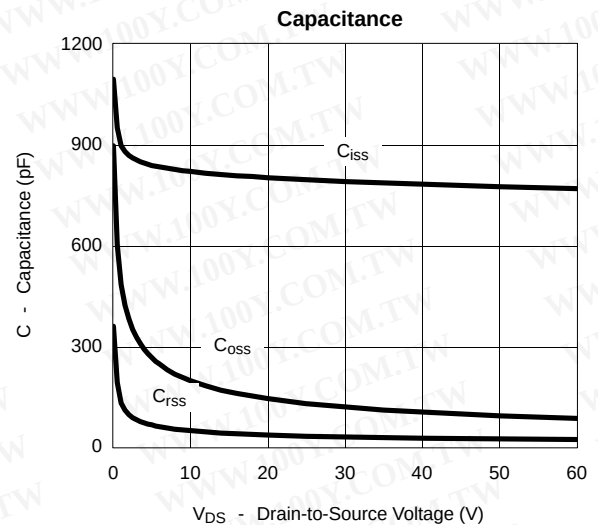
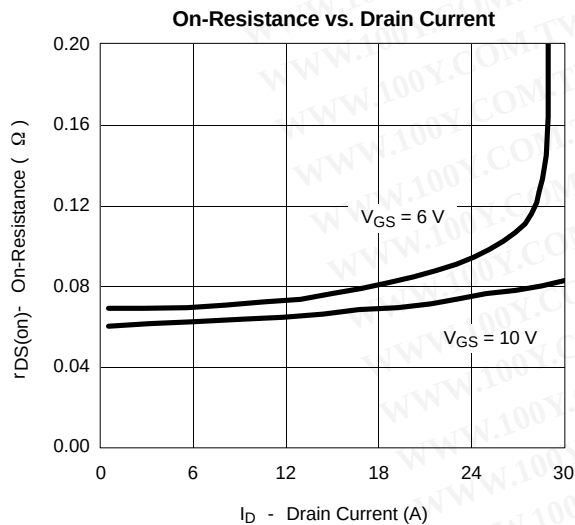
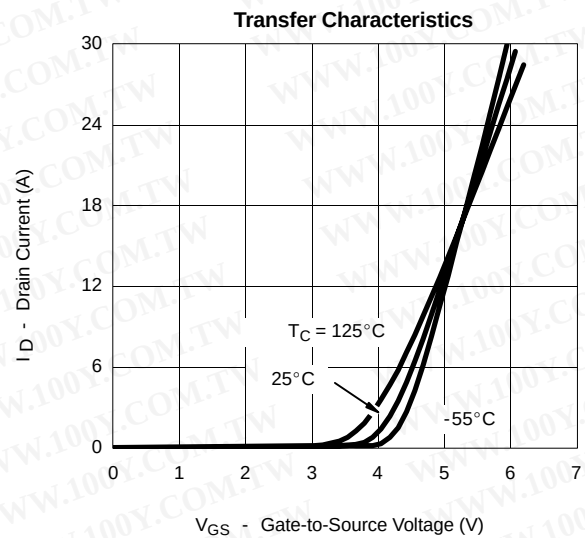
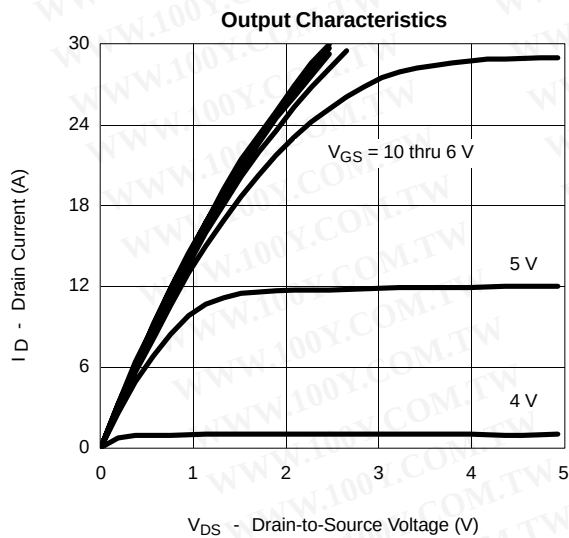
Notes

- a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
b. For design aid only; not subject to production testing.

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TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)



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