DM134B、DM135B

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16-Bit Constant Current LED Drivers with 3.3v ~ 5v Supply Voltage

DM134B、DM135B

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General Description

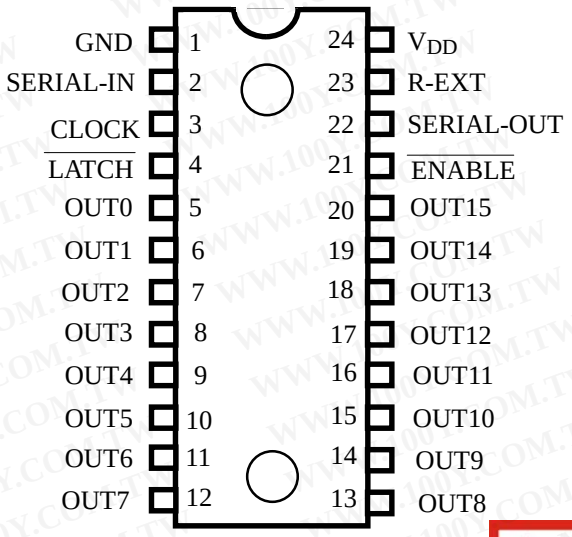
The DM134B、DM135B are constant current drivers specifically designed for LED display applications. The value of constant current can be varied using an external resistor. The devices include a 16-bit shift register, latches, and constant current drivers on a single Silicon CMOS chip.

Features

- 3.3V~5V CMOS Compatible Input
- Maximum Clock Frequency: 25MHz (Cascade Operation)
- Maximum Output Voltage: 17V
- Package: DIP24, SOP24, SSOP24, QFN32
- Package and Pin Layout: Pin layout and functionality are similar to those of the ST2221C. (Each characteristic value is different.)
- Constant Current Matching: (Ta = 25°C、V_{DD} = 5.0V)
  Chip-to-Chip: ± 10.0%
  Bit-to-Bit:
  DM134B:± 4.0% @ I_{OUT} = 30 ~ 90mA
  ± 6.0% @ I_{OUT} = 20 ~ 30mA
  DM135B:± 4.0% @ I_{OUT} = 20 ~ 60mA
  ± 6.0% @ I_{OUT} = 5 ~ 20mA

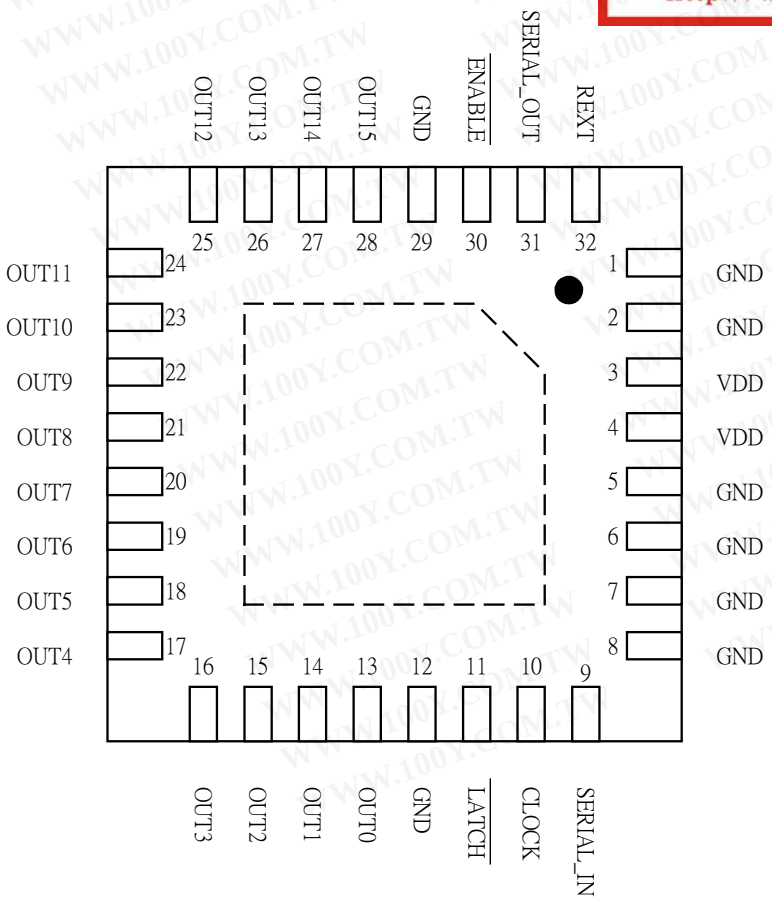
Pin Connection (Top view)

DIP24、SOP24、SSOP24

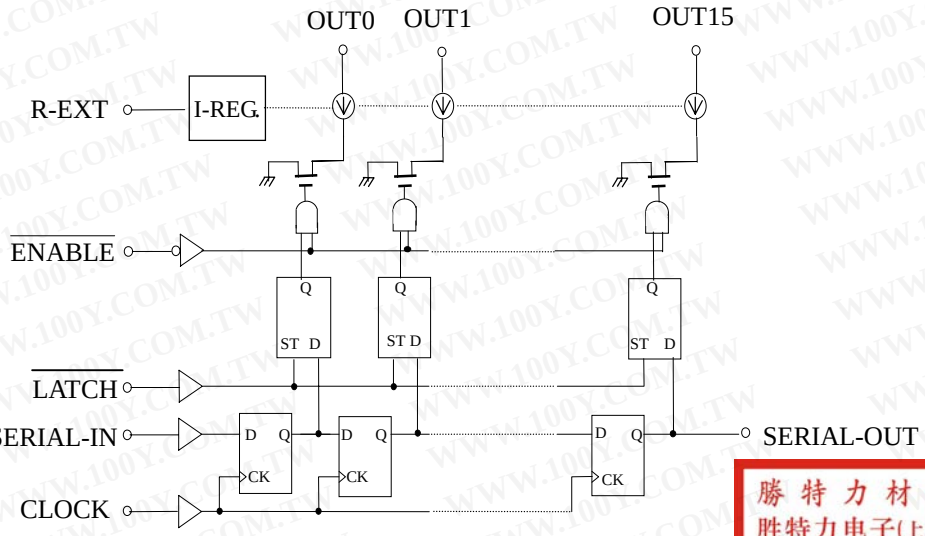


Pin Connection (Bottom view)

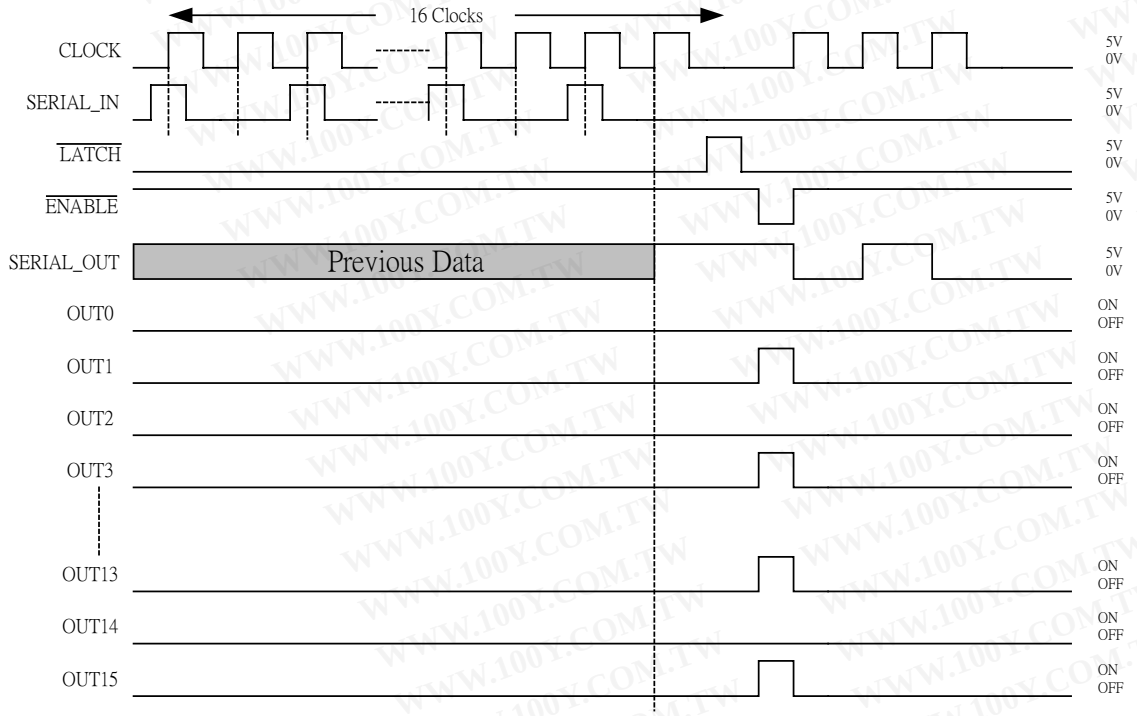
QFN32



Block Diagram



Timing Diagram



(Note) Latches are level sensitive (not edge triggered).

$\overline{\text{LATCH}}$-terminal = H level, latches become transparent; $\overline{\text{LATCH}}$-terminal = L level, latches hold data.

$\overline{\text{ENABLE}}$-terminal = H level, all outputs (OUT0~15) are off.

An external resistor is connected between R-EXT and GND for setting up the value of constant current.

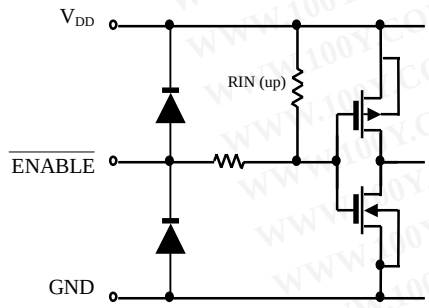
SERIAL-OUT changes state on the rising edges of clock.

Pin Description

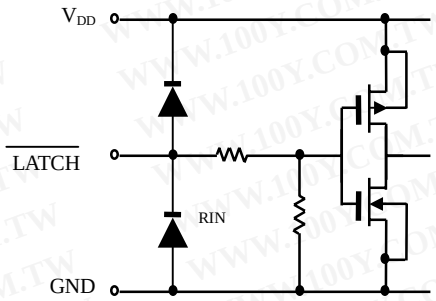
PIN No.	PIN NAME	FUNCTION
1	GND	Ground terminal
2	SERIAL-IN	Input terminal of a data shift register
3	CLOCK	Input terminal of a clock for shift register
4	$\overline{\text{LATCH}}$	Input terminal of data strobe
5~20	OUT0~15	Output terminals
21	$\overline{\text{ENABLE}}$	Input terminal of output enable (active low)
22	SERIAL-OUT	Output terminal of a data shift register
23	R-EXT	Input terminal of an external resistor
24	V_{DD}	5V Supply voltage terminal

Equivalent Circuit of Inputs and Outputs

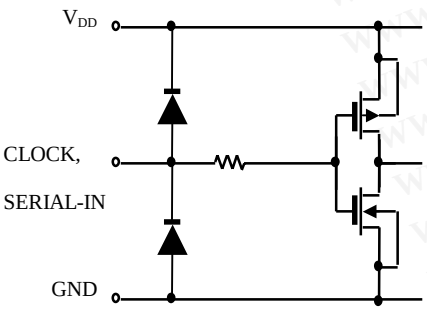
1. $\overline{\text{ENABLE}}$ terminal



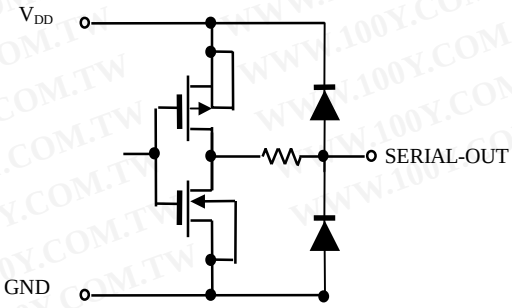
2. $\overline{\text{LATCH}}$ terminal



3. CLOCK, SERIAL-IN terminal



4. SERIAL-OUT terminal



Maximum Ratings (Ta = 25°C, $Tj_{(max)}$ = 150°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	VDD	0 ~ 7.0	V
Input Voltage	VIN	-0.4 ~ VDD+0.4	V
Output Current	IOUT	90 (DM134B)	mA
		60 (DM135B)	
Output Voltage	VOUT	-0.3 ~ 17	V
Clock Frequency	fCLK	25	MHz
GND Terminal Current	IGND	1440 (DM134B)	mA
		960 (DM135B)	
Power Dissipation (On 4-layer PCB)	PD	2.5 (DIP-24 : Ta=25°C)	W
		1.58 (SOP-24 : Ta=25°C)	
		1.39 (SSOP-24 : Ta=25°C)	
		3.08 (QFN-32 : Ta=25°C)	
Thermal Resistance (On 4-layer PCB)	Rth(j-a)	50.0 (DIP-24)	°C/W
		79.2 (SOP-24)	
		90.2 (SSOP-24)	
		40.6 (QFN-32)	
Operating Temperature	Topr	-40 ~ 85	°C
Storage Temperature	Tstg	-55 ~ 150	°C

Recommended Operating Condition

CHARACTERISTIC	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	VDD	—	3.0	5.0	5.5	V
Output Voltage	VOUT	—	—	—	17	V
Operating temperature	T_{OPR}	—	-40	—	85	℃
Output Current	IOH	SERIAL-OUT	—	—	1.0	mA
	IOL	SERIAL-OUT	—	—	-1.0	
Input Voltage	VIH	—	0.7VDD	—	VDD+0.3	V
	VIL	—	-0.3	—	0.3VDD	
$\overline{\text{LATCH}}$ Pulse Width	tw LAT	VDD = 3.0 ~ 5.5 V	15	—	—	ns
CLOCK Pulse Width	tw CLK		15	—	—	ns
Set-up Time for DATA	tsetup(D)		20	—	—	ns
Hold Time for DATA	thold(D)		20	—	—	ns
Set-up Time for LATCH	tsetup(L)		15	—	—	ns
Clock Frequency	fCLK	Cascade operation	—	—	25	MHz

Electrical Characteristics (VDD = 5.0 V, Ta = 25°C unless otherwise noted)

CHARACTERISTIC	SYMBOL		CONDITION		MIN.	TYP.	MAX.	UNIT
Input Voltage "H" Level	VIH		—		0.7VDD	—	VDD	V
Input Voltage "L" Level	VIL		—		GND	—	0.3VDD	
Output Leakage Current	IOH		VOH = 17 V		—	—	1.0	uA
Output Voltage (S - OUT)	VOL		IOL = 1.0 mA		—	—	0.4	V
	VOH		IOH = -1.0 mA		4.6	—	—	
Output Current (Bit-Bit)	ΔIout	DM134B	VOUT = 1.2V (1 channel on)	REXT = 377Ω	—	±1.5	±4	%
		DM135B		REXT = 900Ω				
Output Current (Chip-Chip)	Iout	DM134B	VOUT = 1.2V (1 channel on)	REXT = 377Ω	36.0	40.0	44.0	mA
		DM135B		REXT = 900Ω	18.0	20.0	22.0	
Output Voltage Regulation	I_{DM134B}		Vout = 1.2V ~ 5.0V (% / Vout)	REXT = 377Ω	—	0.1	0.5	% / V
	I_{DM135B}			REXT =900Ω				
Supply Voltage Regulation	% / VDD		Vdd = 3.0V ~ 5.5V		—	1	3	% / V
Pull-Up Resistor	RIN(up)		—		150	300	600	KΩ
Pull-Down Resistor	RIN(down)		—		100	200	400	KΩ
Supply Current "OFF"	Idd (off)	DM134B	REXT = OPEN, all outputs off		—	2	4	mA
			REXT = 210Ω, all outputs off		—	14	28	
		DM135B	REXT = OPEN, all outputs off		—	2	4	
			REXT = 300Ω, all outputs off		—	14	28	
Supply Current "ON"	Idd (on)	DM134B	REXT = 210Ω, all outputs on		—	14	28	
		DM135B	REXT = 300Ω, all outputs on		—	14	28	

Switching Characteristics (Ta = 25 °C unless otherwise noted)

DM134B

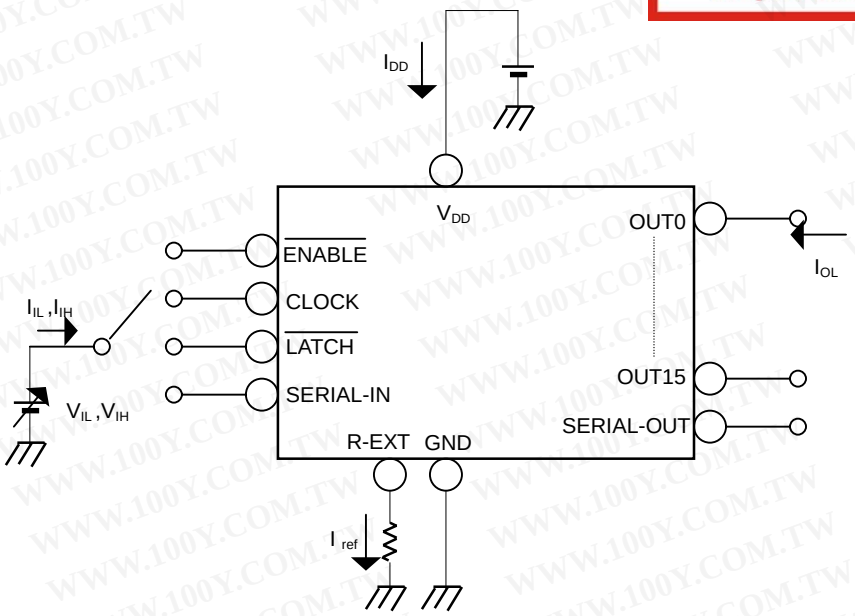
CHARACTERISTIC		SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Propagation Delay Time ("L" to "H")	$\overline{\text{ENABLE}}$-OUTn	t_{PLH}	VDD=5.0V VIH=VDD VIL=GND REXT=210Ω VL=5.0V RL=47Ω CL=15pF	—	20	40	ns
	CLK-SOUT			—	20	25	
Propagation Delay Time ("H" to "L")	$\overline{\text{ENABLE}}$-OUTn	t_{PHL}		—	50	100	ns
	CLK-SOUT			—	20	25	
Output Current Rise Time		t_{or}		—	550	800	ns
Output Current Fall Time		t_{of}		—	20	40	ns

DM135B

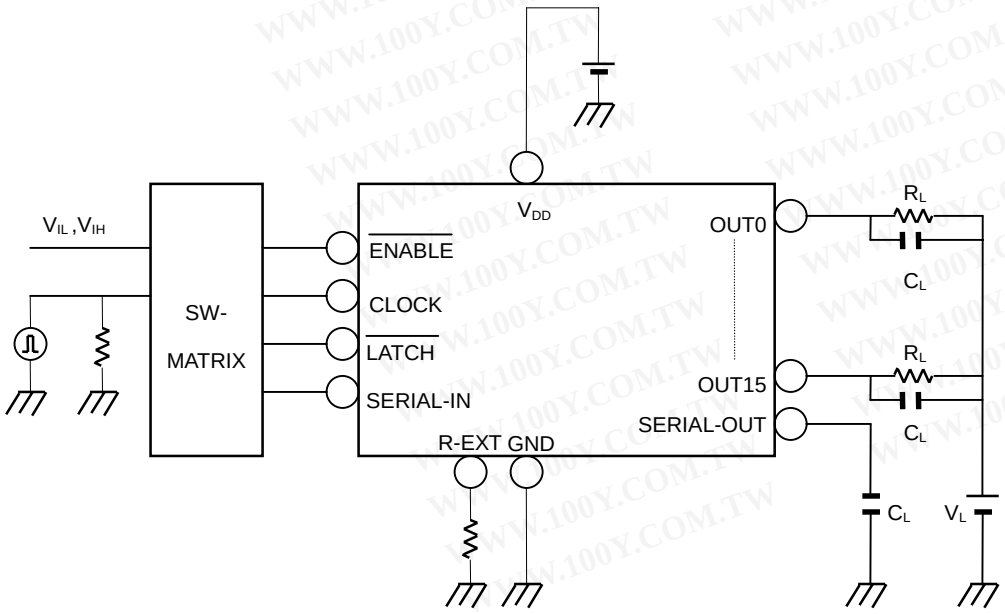
CHARACTERISTIC		SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Propagation Delay Time ("L" to "H")	ENABLE-OUTn	t_{PLH}	VDD=5.0V VIH=VDD VIL=GND REXT=630Ω VL=5.0V RL=150Ω CL=13pF	—	20	40	ns
	CLK-SOUT			—	20	25	
Propagation Delay Time ("H" to "L")	$\overline{\text{ENABLE}}$-OUTn	t_{PHL}		—	30	60	ns
	CLK-SOUT			—	20	25	
Output Current Rise Time		t_{or}		25	50	100	ns
Output Current Fall Time		t_{of}		15	30	60	ns

Test Circuit

DC characteristic

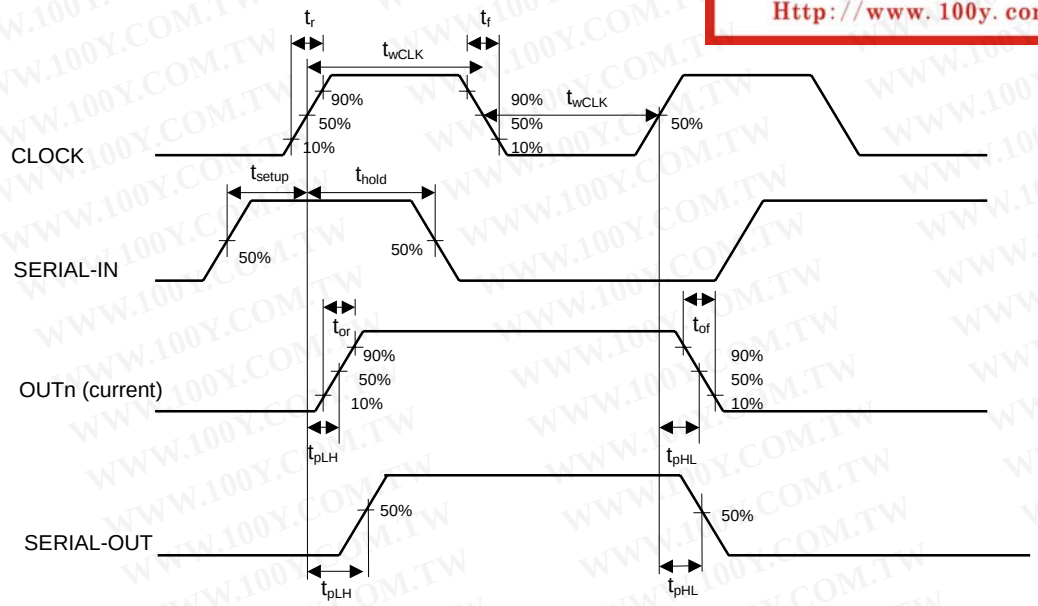


AC characteristic

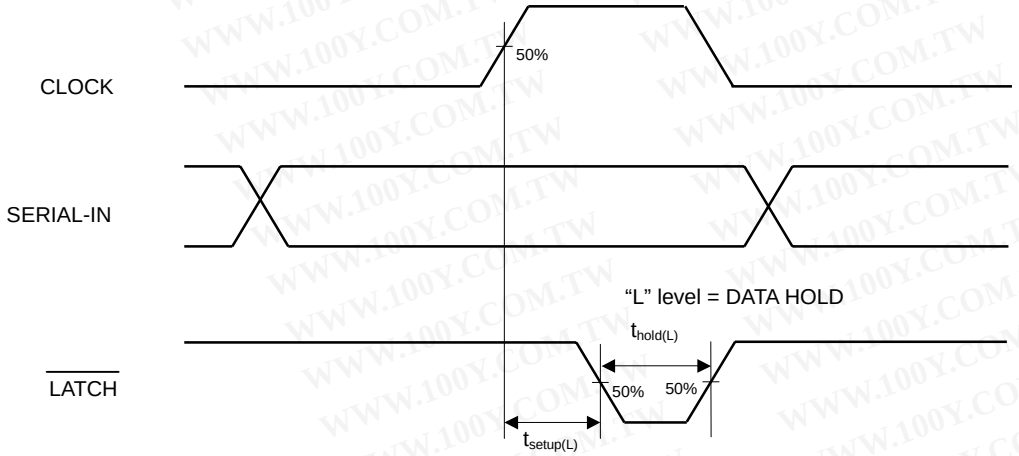


Timing Diagram

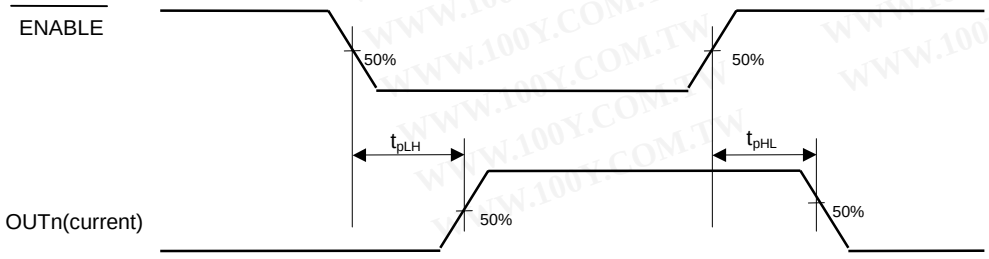
1. CLOCK-SERIAL-IN, SERIAL-OUT, OUTn (current)



2. CLOCK-$\overline{\text{LATCH}}$

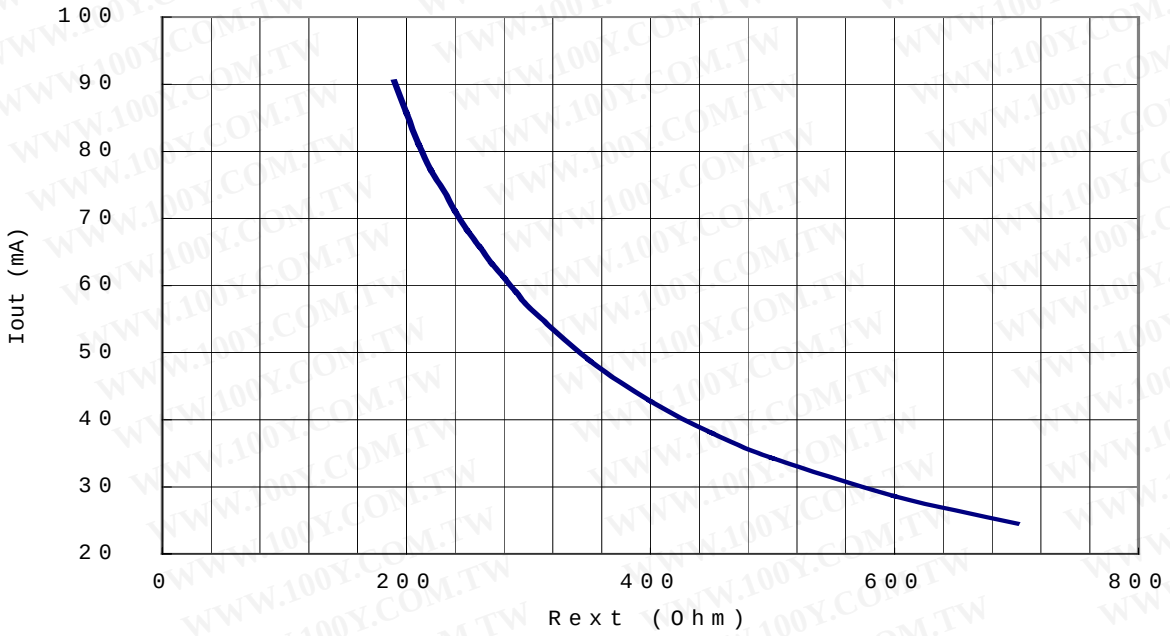


3. $\overline{\text{ENABLE}}$-OUTn (current)

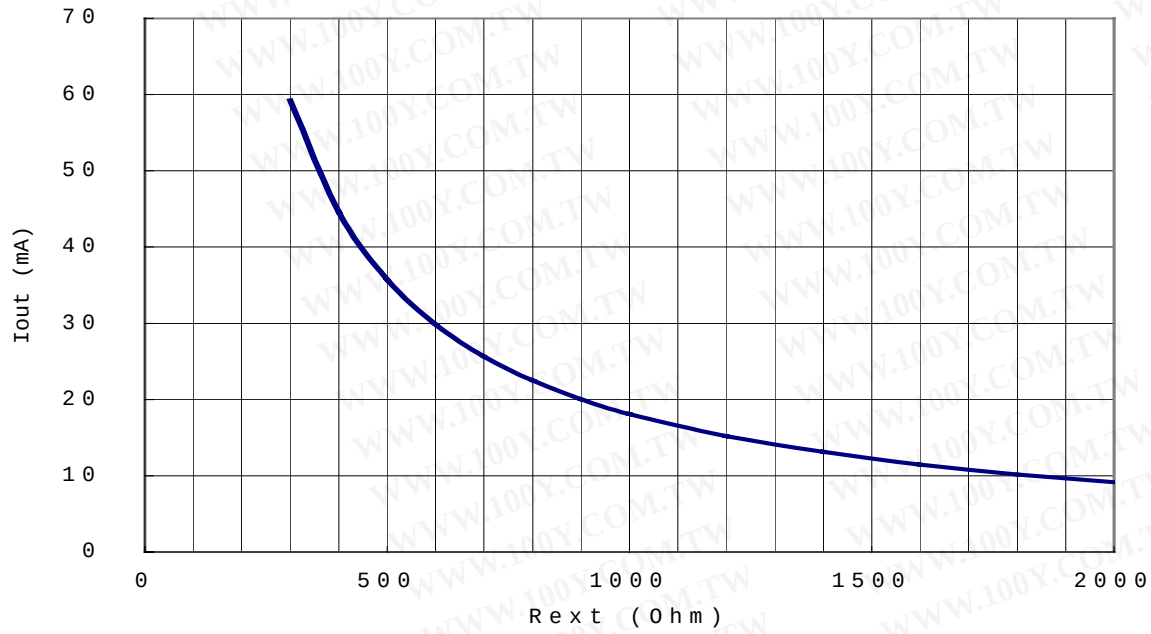


Output Current vs. External Resistor

DM134B



I

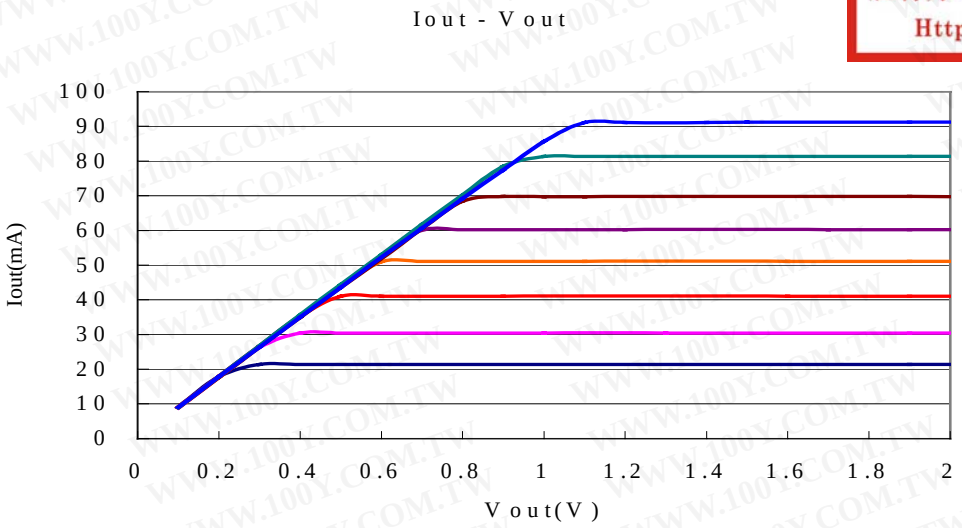


Conditions: Vref=1.30V
DM134B:Iout ≈ Vref / Rext * 13.1,
DM135B:Iout ≈ Vref / Rext * 13.9.

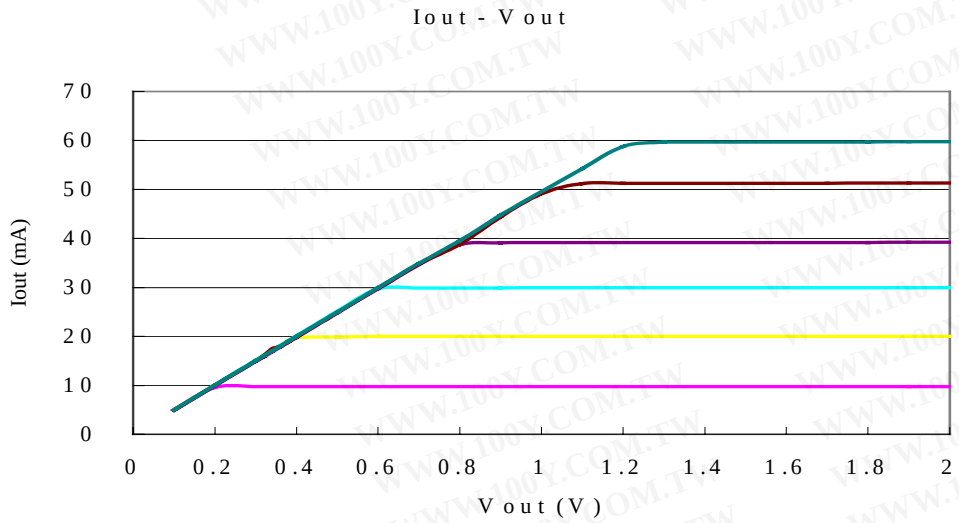
Note: The resistor should be placed as close to the Rext terminal as possible to avoid the noise influence.

Output Current Performance vs. Output Voltage

DM134B

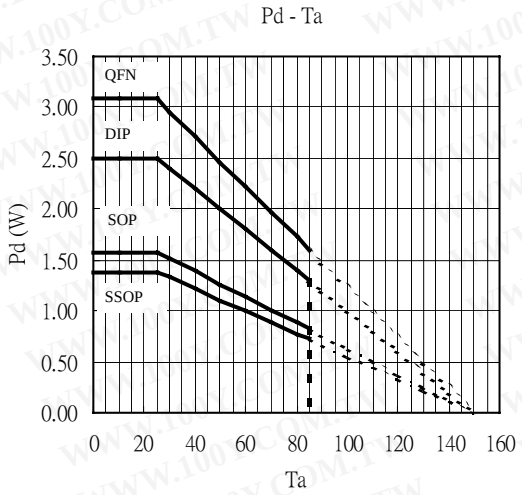


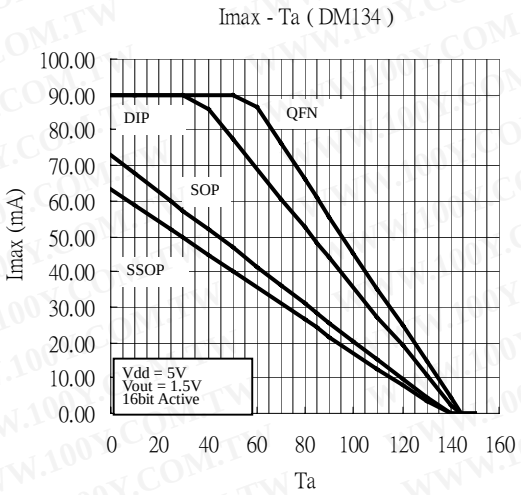
DM135B

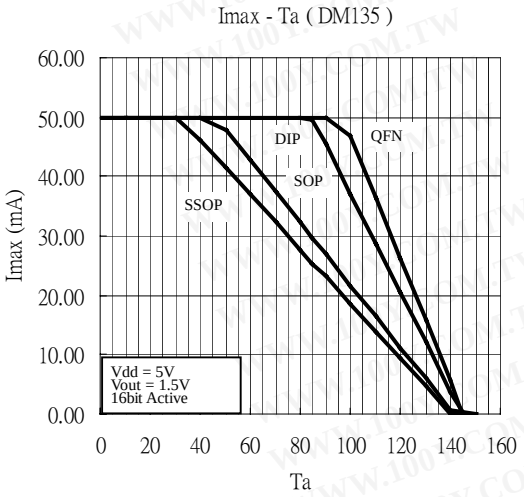


Note:

In order to obtain a good constant current output, a suitable output voltage is necessary. Users can get related information about the minimum output voltage from the above graphs. Even under the same output current condition, the minimum output voltage required for each part is different.







Note

As the power dissipation of a semiconductor chip is limited by its package and ambient temperature, this device requires a maximum output current given by an operating condition. The maximum allowable power consumption (Pd (max)) of this device is calculated as follows:

$$Pd(\max)(Watt) = \frac{(\text{Tj (junction temperature) (max)} - \text{Ta (ambient temperature)})(^{\circ}C)}{\text{Rth}\ (^{\circ}C/Watt)}$$

Based on the Pd (max), the maximum allowable current can be calculated as follows:

$$\text{Iout} = (\text{Pd} - V_{DD} \cdot I_{DD}) / (\#\ \text{outputs} \cdot \text{Vo} \cdot \text{Duty})$$

System Configuration Example

[1] Output current (I_{OUT})

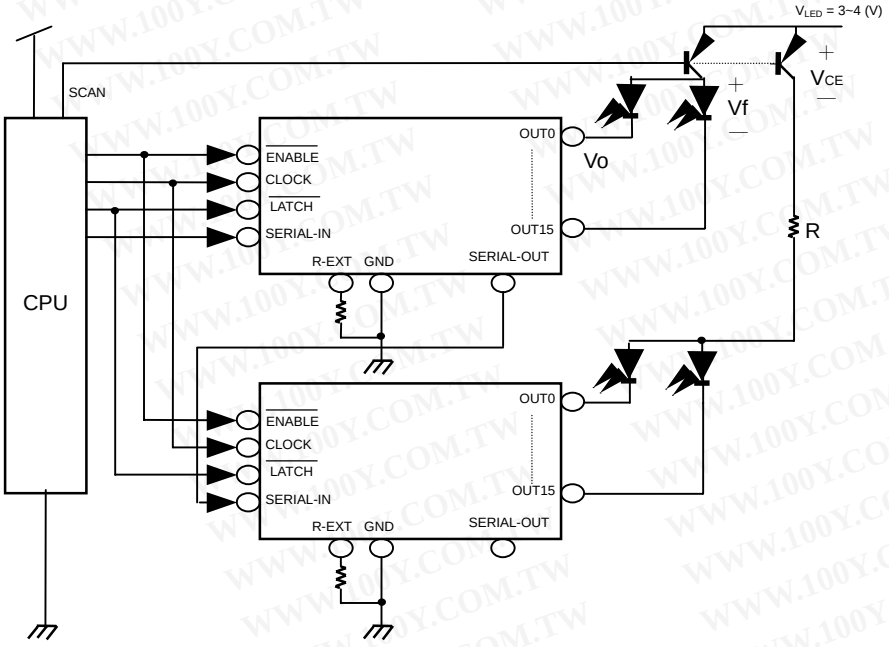
Sink current is set by the external resistor as shown in the figure of Iout vs. Rext.

[2] LED supply voltage (V_{LED}) setup

$$V_{LED} = V_{CE}(T_r V_{sat}) + V_f(\text{LED forward voltage}) + V_O(\text{IC output voltage})$$

To prevent too much power from dissipating by the higher V_{LED} of the device, an additional R can be used to reduce the Vout when the outputs consume current is as follows:

$$R = \frac{V_{LED} - V_{CE} - V_f - V_O(\min)}{I_O(\max) * Bit(\max)}$$



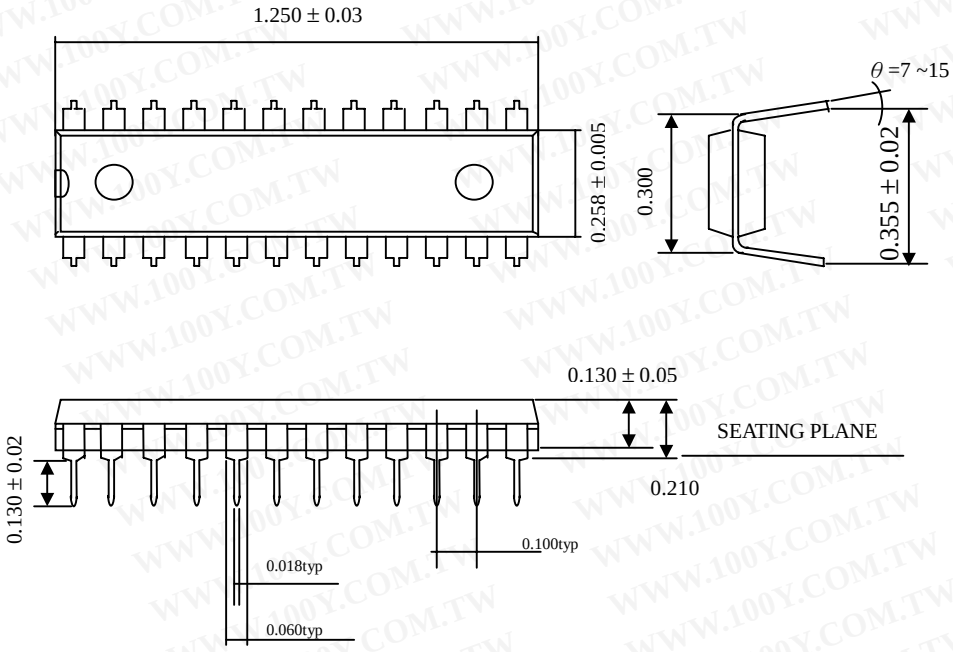
Note

This device has only one ground pin shared by signal, output sink current, and power ground. It is advisable to pattern the ground layout with minimized inductance so that the switching noise induced by the input signals and the output sink current would not cause chip malfunction. To prevent drivers' outputs from damaging by overshoot stresses, it is also advisable not to turn off the drivers and scan transistors simultaneously. For the QFN package, the IC's thermal pad, which is internally connected to the bottom side of chip, should be connected to GND. In addition, a good PCB layout pattern of the thermal pad is required in order to have a better performance in thermal effect.

Package Outline

P-DIP 24

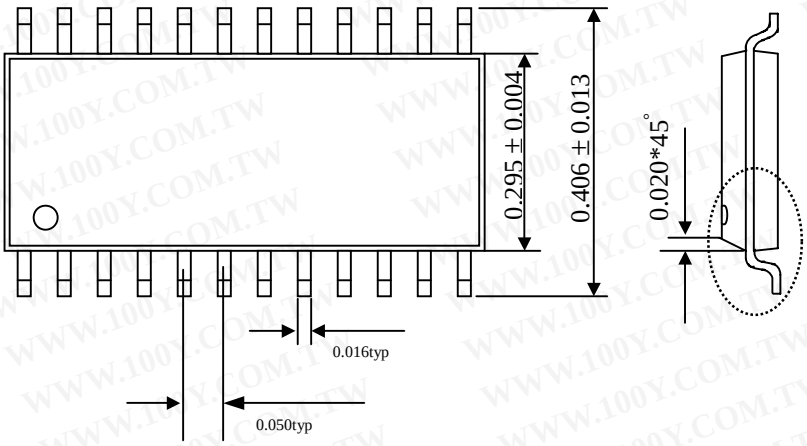
UNIT：INCH

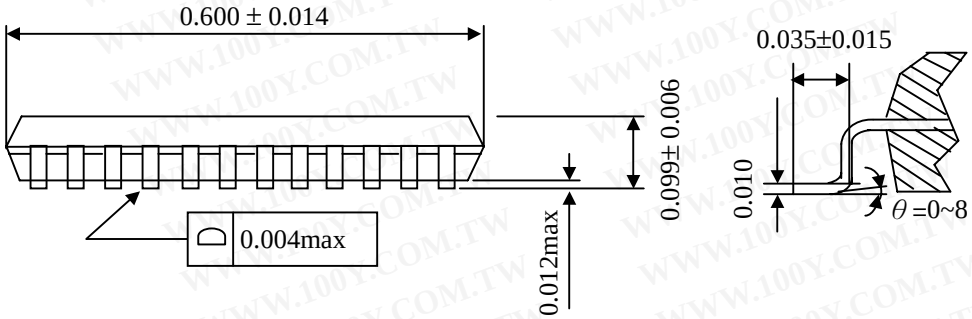


Package Outline

SOP24

UNIT：INCH

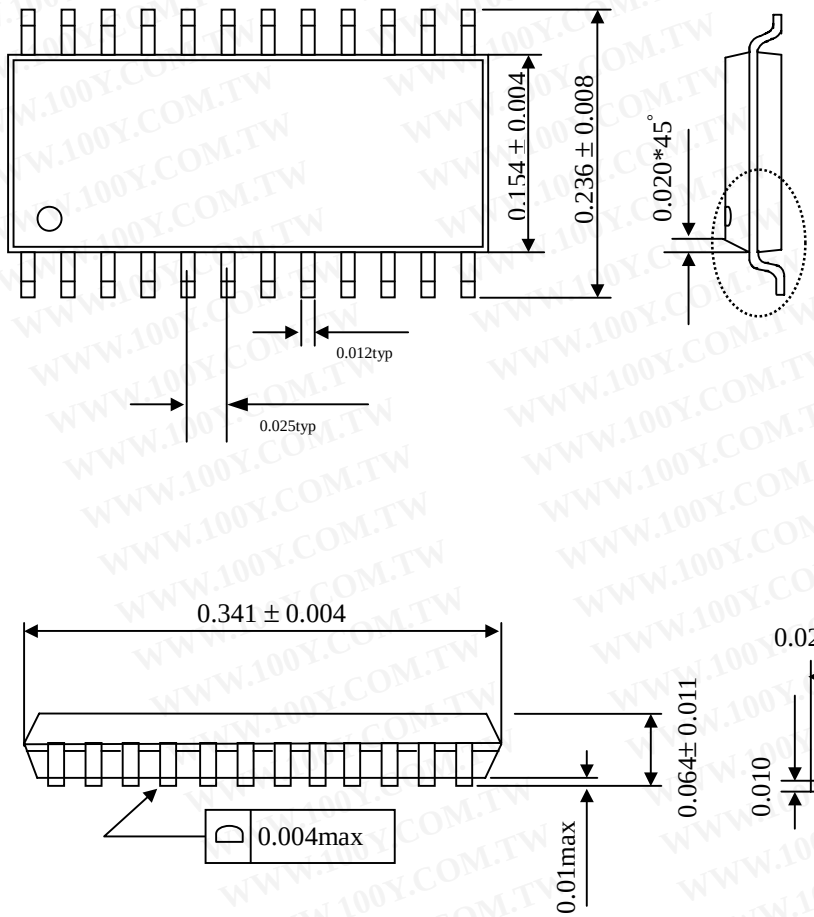




Package Outline

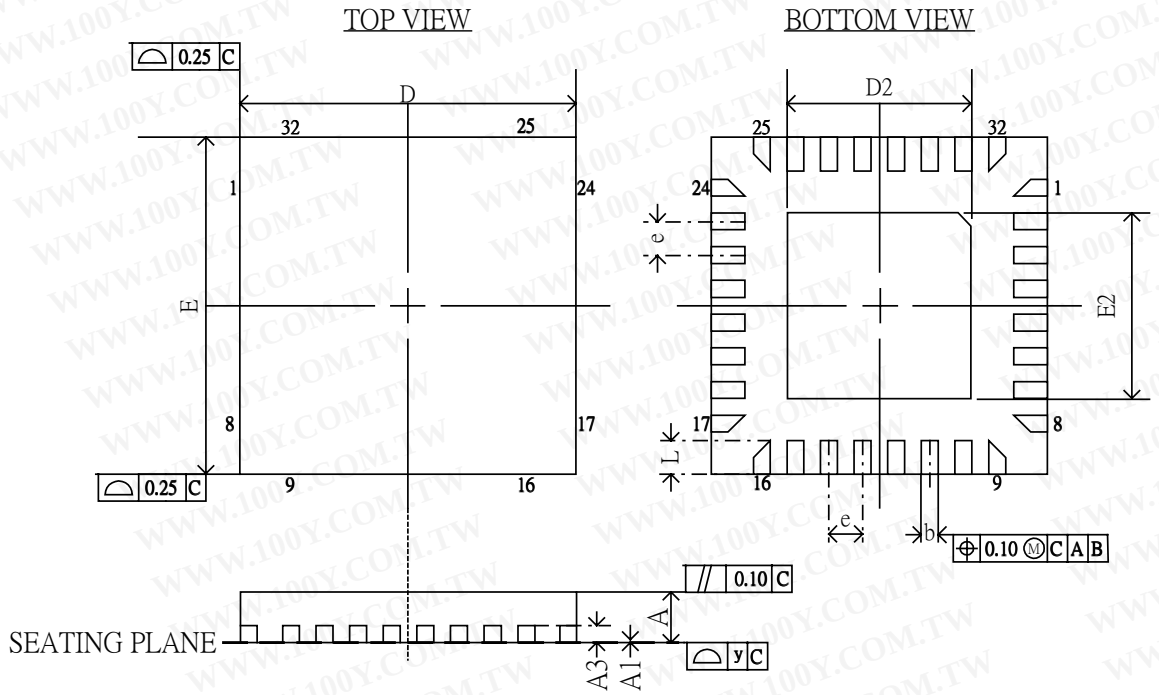
SSOP24

UNIT：INCH



Package Outline

QFN32



SYMBOL	DIMENSION (mm)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	27.6	29.5	31.5
A1	0	0.02	0.05	0	0.79	1.97
A3		0.25 REF			9.84 REF	
b	0.18	0.23	0.30	7.09	9.06	11.81
D		5.00 BSC			196.85 BSC	
D2	1.25	2.70	3.25	49.21	106.30	127.95
E		5.00 BSC			196.85 BSC	
E2	1.25	2.70	3.25	49.21	106.30	127.95
e		0.50 BSC			19.69 BSC	
L	0.30	0.40	0.50	11.81	15.75	19.69
y		0.10			3.94	

Note: 1.DIMENSIONING AND TOLERANCING CONFORM TO ASME Y145.5M-1994.

2. REFER TO JEDEC STD. MO-220 WHHD-2 ISSUE A

The products listed herein are designed for ordinary electronic applications, such as electrical appliances, audio-visual equipment, communications devices and so on. Hence, it is advisable that the devices should not be used in medical instruments, surgical implants, aerospace machinery, nuclear power control systems, disaster/crime-prevention equipment and the like. Misusing those products may directly or indirectly endanger human life, or cause injury and property loss.
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