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1. Scope:

The specifications are applicable to all series of chip type multi-layer ceramic capacitor.

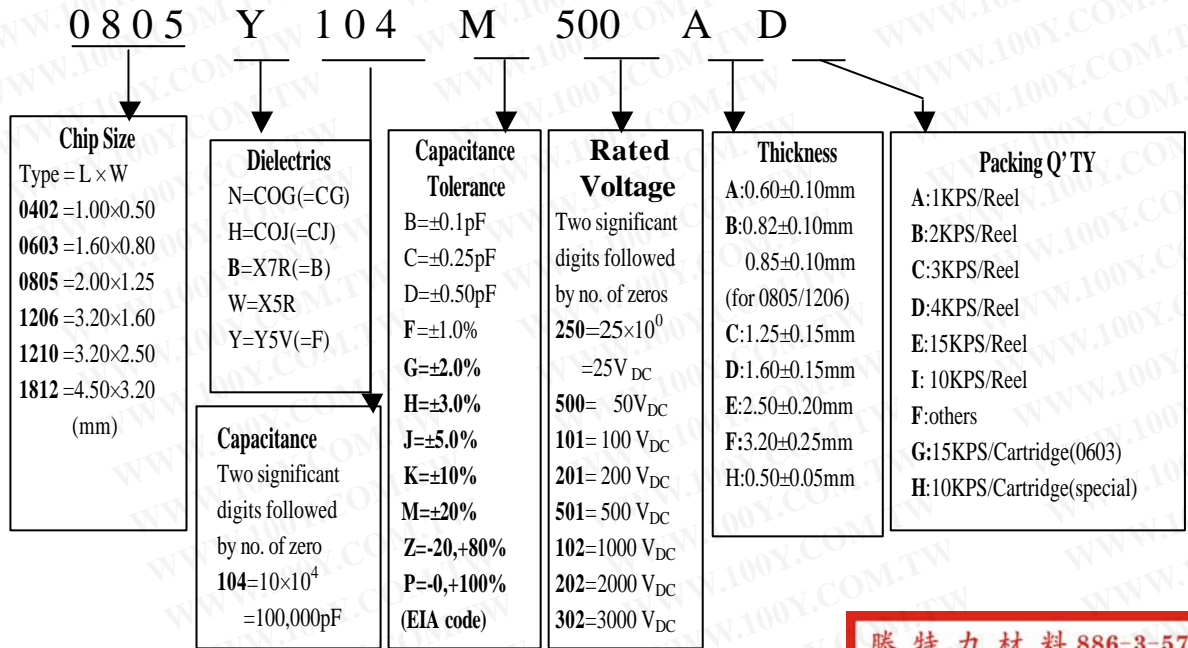
Include Dielectrics: NPO, X7R,X5R and Y5V

Chip Size: 0402, 0603, 0805, 1206, 1210, 1812.

Capacitance: 0.5 pF~47.0μF

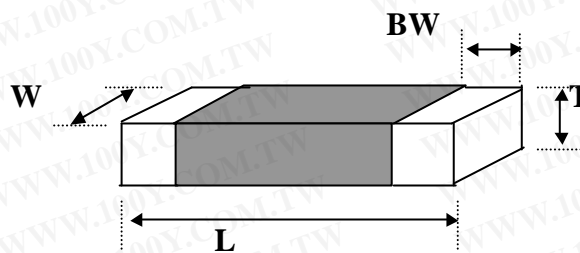
2. Part Numbering System:

(example)



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3. Dimensions:



Type	L (mm)	W (mm)	BW (mm)	T (mm)						
				(A)	(B)	(C)	(D)	(E)	(F)	(H)
0402	1.00±0.10	0.50±0.05	0.19±0.10	—	—	—	—	—	—	0.50±0.05
0603	1.60±0.10	0.82±0.10	0.29±0.15	—	0.82±0.10	—	—	—	—	—
0805	2.00±0.10	1.25±0.10	0.41±0.25	0.600±0.10	0.85±0.10	1.25±0.15	—	—	—	—
1206	3.20±0.15	1.60±0.10	0.47±0.25	0.600±0.10	0.85±0.10	1.25±0.15	1.60±0.15	—	—	—
1210	3.20±0.20	2.50±0.20	0.50±0.25	—	—	1.25±0.15	1.60±0.15	2.50±0.20	—	—
1812	4.50±0.50	3.20±0.25	0.60±0.35	—	—	1.25±0.15	1.60±0.15	2.50±0.20	3.20±0.25	—

4. Capacitance Range:

Y5V																								
Cp / Vdc	0402				0603				0805				1206				1210				1812			
	50	25	16	10	50	25	16	10	50	25	16	10	50	25	16	10	50	25	16	10	50	25	16	10
103	H																							
153	H																							
223	H	H			B																			
333		H			B																			
473		H	H		B			B																
683		H	H		B	B		B																
104			H		B	B		B				B												
154				H	B			B				B												
224				H	B	B		B	B			B				C								
334				H		B		B	B			B				C			C					
474						B		C	B	B		B	B			C			C					
684						B	B	C	B	B		B	B			C			C					
105							B	C	C	B		C	B	B		C	C		C					
155										C	B		B	B		C	C		C	C				
225										C	B		C	B		C	C	C	C	C				
335											B			B	B	D	C	C		C	C			
475											C			C	C	E	D	C		D	C	C		
106															D		E	D	C	E	D	C		
226																	E	D		E	D			
336																		E			E			
476																								
107																								

Tolerance Y5V:M(±20%),Z(-20,+80%) Thickness:A:0.60±0.10mm B:0.82±0.10mm 0.85±0.10mm(for 0805/1206) C:1.25±0.15mm D:1.60±0.15mm E:2.50±0.20mm F:3.20±0.25mm H:0.50±0.05mm
Above capacitance for reference only ,actual cap. range depends on the standard products.

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X7R(16V)/X5R(=10V)																								
Cp \ Vdc	0402				0603				0805				1206				1210				1812			
	50	25	16	10	50	25	16	10	50	25	16	10	50	25	16	10	50	25	16	10	50	25	16	10
221	H				B				B				B											
271	H				B				B				B											
331	H				B				B				B											
391	H				B				B				B											
471	H				B				B				B											
561	H				B				B				B											
681	H				B				B				B											
821	H				B				B				B											
102	H				B				B				B											
122	H				B				B				B											
152	H				B				B				B											
182	H				B				B				B											
222	H				B				B				B											
272	H				B				B				B											
332	H				B				B				B										C	
392	H				B				B				B										C	
472	H				B				B				B										C	
562		H			B				B				B										C	
682		H			B				B				B										C	
822		H			B				B				B										C	
103		H	H		B				B				B										C	
123			H		B				B				B										C	
153			H		B				B				B										C	
183			H		B				B				B										C	
223			H		B				B				B										C	
273			H		B				B				B										C	
333			H		B	B			B				B										C	
393			H		B	B			B				B										C	
473			H	H	B	B			B				B										C	
563				H		B	B		B				B										C	
683				H		B	B		B				B										C	
823				H		B	B		B				B										C	
104				H		B	B		B	B	B		B										C	
124						B			C	B	B		C	B									C	
154						B			C	C	B		C	B									C	
184						B			C	C	B		C	B									C	
224						B	B		C	C	B		C	B									C	
274							B		C	C			C	B									C	
334									C	C			C	C									C	
394										B			C	C	B								C	
474										B			C	D	B								C	
564										C				D	B								C	
684										C				D	C								C	
824											C			D	C								D	
105											C			D	C								D	
125															D								D	C
155															D								D	C
225															D								D	D
335																							D	
475																							D	
565																								D
685																								E

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NPO(COJ)																										
		0402				0603				0805				1206				1210				1812				
$C_p \setminus V_{DC}$		50	25	16	10	50	25	16	10	50	25	16	10	50	25	16	10	50	25	16	10	50	25	16	10	
0R5	H																									
1R0	H					B				B				B												
2R0	H					B				B				B												
3R0	H	H				B				B				B												
4R0	H	H				B				B				B												
5R0	H	H				B				B				B												
6R0	H	H				B				B				B												
7R0	H	H				B				B				B												
8R0	H	H				B	B			B				B												
9R0	H	H				B	B	B		B				B												
100	H	H				B	B	B		B	B			B												
120		H				B	B	B		B	B			B												
150		H				B	B	B		B	B			B												
180		H				B	B	B		B	B			B												
200		H				B	B	B		B	B			B												
220		H				B	B	B		B	B			B												
270		H				B	B	B		B	B			B												
300		H				B	B	B		B	B			B												
330		H	H			B	B	B		B	B			B												
390			H			B	B			B	B			B												
470						B	B			B	B			B												
560						B	B			B	B			B												
680						B	B			B	B			B												
820										B				B												
101										B				B												

Tolerance NPO (0.5 ~ 5.0pF) : C ($\pm 0.25pF$) NPO ($\geq 10pF$): F($\pm 1\%$),G($\pm 2\%$),H($\pm 3\%$),J($\pm 5\%$),K($\pm 10\%$)
 NPO (5.1 ~ 9.9pF) : D($\pm 0.50pF$)
 Thickness: A:0.60 \pm 0.10mm B:0.82 \pm 0.10mm 0.85 \pm 0.10mm(for 0805/1206) C:1.25 \pm 0.15mm D:1.60 \pm 0.15mm
 E:2.50 \pm 0.20mm F:3.20 \pm 0.25mm H:0.50 \pm 0.05mm
 Above capacitance for reference only ,actual cap. range depends on the standard products.

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NPO(COG)																								
Cp \ Vdc	0402				0603				0805				1206				1210				1812			
	50	25	16	10	50	25	16	10	50	25	16	10	50	25	16	10	50	25	16	10	50	25	16	10
0R5																								
1R0					B			B																
2R0					B			B																
3R0					B			B																
4R0					B			B																
5R0					B			B																
6R0					B			B																
7R0					B			B																
8R0	H				B			B																
9R0	H				B			B																
100	H				B			B																
120	H				B			B																
150	H				B			B																
180	H				B			B																
200	H				B			B																
220	H				B			B																
270	H				B			B																
300	H				B			B																
330	H	H			B			B																
390	H	H			B			B									B							
470	H	H			B			B									B							
560	H	H			B			B									B							
680	H	H			B			B					B				B							
820	H	H			B		B	B					B				B							
101	H	H			B		B	B					B				B							
121	H	H			B		B	B					B				B							
151	H	H			B		B	B					B				B							
181	H	H			B		B	B					B				B							
201	H	H			B		B	B					B				B							
221	H	H	H		B		B	B					B				B							
271	H	H	H		B		B	B					B				B							
331			H		B		B	B					B				B							
391			H		B		B	B					B				B							
471			H		B		B	B					B				B							
561					B		B	B					B				B							
681					B		B	B					B				B							
821					B		B	B					B				B							
102					B	B	B	B					B				B					B		
152						B		B	B				B				B					B		
222						B		B	B				B				B					B		
332								B	B				B				B					B		
392								B	B				B				B					B		
472									C	B			C				C					B		
562										C			C				C					B		
682										C			C				C					C		
103													C	C			C					C		
223													C	C			C					C		
473																	C							

Tolerance NPO (0.5 ~ 5.0pF) : C (±0.25pF) NPO (10pF): F(±1%),G(±2%),H(±3%),J(±5%),K(±10%)
 NPO (5.1 ~ 9.9pF) : D(±0.50pF)
 Thickness: A:0.60±0.10mm B:0.82±0.10mm 0.85±0.10mm(for 0805/1206) C:1.25±0.15mm D:1.60±0.15mm
 E:2.50±0.20mm F:3.20±0.25mm H:0.50±0.05mm
 Above capacitance for reference only ,actual cap. range depends on the standard products.

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5. Operating Temperature Range:

NPO : -55 ~ +125
 X7R : -55 ~ +125
 X5R : -55 ~ +85
 Y5V : -30 ~ +85

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6. Storage:

- 6.1 Keep the storage environment conditions as following:
 Temperature : 40
 Humidity : 85% RH
- 6.2 Don't open the tape until the parts are to be used ,and store them within one year since the date printed on the reel.
- 6.3 Use the chips within 3 months after the tape is opened.
- 6.4 For product of high dielectric constant (Class2&3 , characteristics B/W & Y),the Electro static capacity changes with the passage of time due to the inherent characteristics of ceramic dielectric materials. The changed capacity reverts to nominal at the temperature it reaches during the soldering process.

7. Specification and Test Condition:

7.1 Capacitance (Cp):

Dielectrics	Specification	Testing Condition
NPO	Within the specified tolerance C:±0.25pF,D:±0.5pF,J:±5%,k:±10%	1.0±0.2Vrms,1MHz±10% (C>1000pF,1KHz±10%) at 25 ,24 hrs after annealing
X7R/X5R	Within the specified tolerance J:±5%,K:±10%,M:±20%	1.0±0.2Vrms,1KHz±10% at 25 ,24 hrs after annealing
Y5V	Within the specified tolerance M:±20%;Z:-20%,+80%	1.0±0.2Vrms,1KHz±10% at 25 ,24 hrs after annealing

7.2 Dissipation Factor (DF):

Dielectrics	Specification	Testing Conditions
NPO	Cp<30pF, Q 400+20Cp; Cp 30pF, Q 1000 (Q=1/DF)	1.0±0.2Vrms,1MHz±10% at 25 (Cp>1000pF,1KHz±10%)
X7R/X5R	Rated voltage 50V, DF 2.5%(Tan 0.025) Rated voltage = 25V, 16V, DF 3.5%(Tan 0.035) Rated voltage = 10V, 6.3V, DF 5.0%(Tan 0.05)	1.0±0.2Vrms,1KHz±10%,at 25
Y5V	Rated voltage 50V, DF 5.0%(Tan 0.05) Rated voltage =25V, DF 7.0%(Tan 0.07) Rated voltage = 16V, DF 9.0%(Tan 0.09) Rated voltage = 10V, DF 12.5%(Tan 0.125) Rated voltage = 6.3V, DF 15.0%(Tan 0.15)	1.0±0.2Vrms,1KHz±10%,at 25

7.3 Insulation Resistance (IR):

Dielectrics	Specification	Testing Conditions
NPO	IR 10G or R x C 500M -uF Whichever is smaller	Rated voltage for 60±5secs ,at 25
X7R/X5R Y5V	IR 10G or R x C 100M -uF Whichever is smaller	

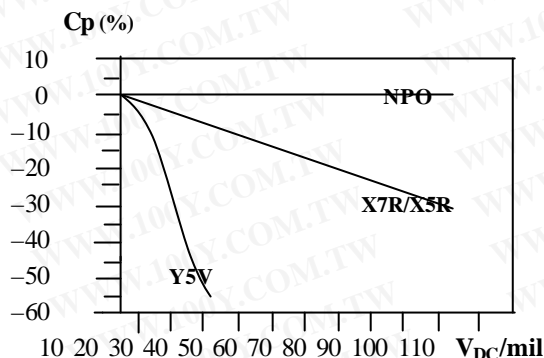
7.4 Dielectric Strength (Flash):

Dielectrics	Specification	Testing Conditions
NPO X7R/X5R Y5V	No remarkable visual damage or flash over during test	300% of rated voltage for class1 capacitors, and 250% of rated voltage for class2 & 3 capacitors. Duration of application: 1 to 5 secs. Charging and discharging current less than 50mA. This condition is suitable to rated voltages no greater than 200V.
NPO X7R	No remarkable visual damage or flash over during test	500V – 200% of rated voltage for 1 to 5 Secs. 1000V - 150% of rated voltage for 1 to 5 Secs. 2000V or above – 120% of rated voltage for 1 to 5 Secs.

1/2-KV to 5-KV parts are to be tested in a non-corrosive dielectric fluid or potted.

7.5 DC Voltage Coefficients:

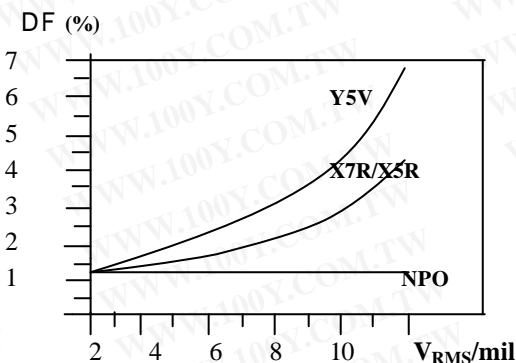
The materials X7R/X5R, Y5V (except NPO) are sensitive to DC voltage. In all cases an eventual decrease in dielectric constant occurs with DC bias, which is more severe with dielectrics of higher dielectric constant. This behavior is attributed to a constraint of the DC voltage on the response of the polarizing mechanisms which give rise to the dielectric constant of the material.



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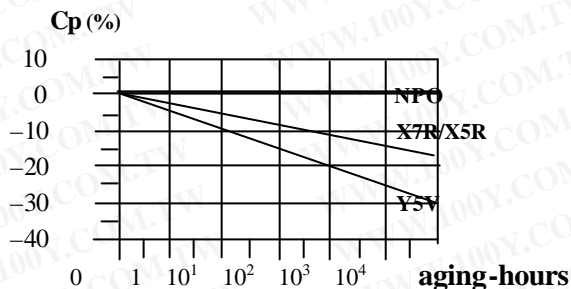
7.6 AC Voltage Coefficient:

The increase of dielectric constant with AC test voltage is accompanied by a marked increase in the dissipation factor (X7R/X5R and Y5V, except NPO), as illustrated below. The multi-layer construction of chip capacitors, with thin dielectric layers, precludes application in circuitry with large AC voltage and high current, as dielectric losses become quite significant from 5 Vrms/mil voltage stress.



7.7 Aging Rate:

There are capacitance aging rate of dielectrics (X7R/X5R and Y5V, except NPO). It means the capacitance of X7R and Y5V will decrease after lots of hours, as following charts:



- Example:
- (1) **X7R** at 10³ hours
 Cp = -10%, Decades = 3
 Aging Rate = $-10 \div 3 = -3.33$ (% decade-hours)
 - (2) **Y5V** at 10³ hours
 Cp = -20%, Decades = 3
 Aging Rate = $-20 \div 3 = -6.67$ (% decade-hours)

Dielectrics	Specification	Testing Conditions
NPO	No capacitance change	Without electric load and keeping at 25
X7R/X5R	Capacitance change less than 3.5%/decade-hours	
Y5V	Capacitance change less than 7%/decade-hours	

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8.Environment Test:

8.1 Breakdown Voltage (BDV):

Dielectrics	Specification	Testing Conditions
NPO X7R/X5R Y5V	More than 8 times of rated voltage. This spec is suitable to the rated voltages no greater than 100V.	By increment rate 300 V _{DC} /sec. until chip breakdown
NPO X7R	200V: 5 times of rated voltage 500V: 2.5 times of rated voltage 1000V: 2 times of rated voltage 2000V: 1.5 times of rated voltage >2000V: 1.2 times of rated voltage	By increment rate 300 V _{DC} /sec. until chip breakdown

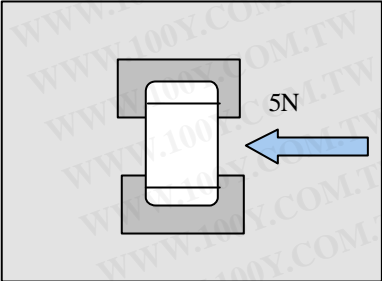
1/2-KV to 5-KV parts are to be tested in a non-corrosive dielectric fluid or potted.

8.2 Temperature Coefficient of Capacitance (TCC):

Dielectrics	Specification	Testing Conditions																
NPO H(CJ) (COJ)	Cp change within ±120ppm/ (for high frequency use)	Measure capacitance under follow table list temperature: <table border="1"> <thead> <tr> <th>Step</th> <th>NPO,X7R</th> <th>Y5V</th> <th>X5R</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>-55</td> <td>-30</td> <td>-55</td> </tr> <tr> <td>2</td> <td>25</td> <td>25</td> <td>25</td> </tr> <tr> <td>3</td> <td>125</td> <td>85</td> <td>85</td> </tr> </tbody> </table> (Related STD JIS C 5101-1998)	Step	NPO,X7R	Y5V	X5R	1	-55	-30	-55	2	25	25	25	3	125	85	85
	Step		NPO,X7R	Y5V	X5R													
1	-55		-30	-55														
2	25		25	25														
3	125	85	85															
N(CG) (COG)	Cp change within ±30ppm/ (for nominal use)																	
X7R/X5R	Cp change within ±15%																	
Y5V	Cp change within +50%,-82%																	

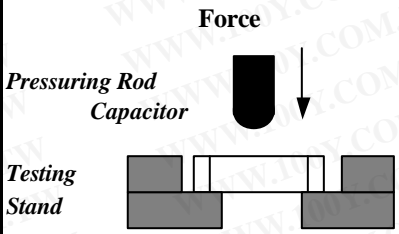
8.3 Adhesion:

Dielectrics	Specification	Testing Conditions
NPO X7R/X5R Y5V	NO separation or indication of separation of electrode	The pressurizing force shall be 5N(=500g*f) and the duration of application shall be 10 ± 1 sec. (Related STD.:JIS C 5101-10-1999)



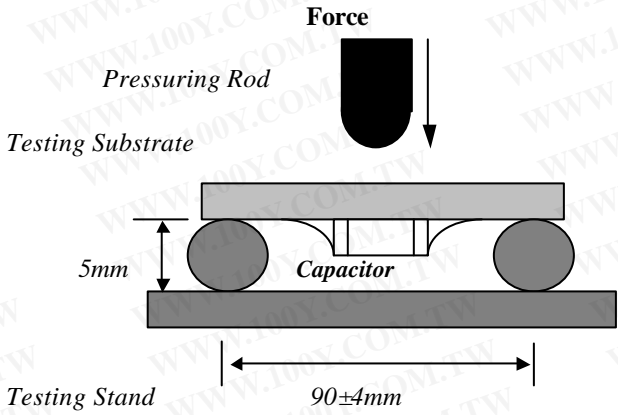
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8.4 Break Strength:

Dielectrics	Specification	Testing Conditions
NPO X7R/X5R Y5V	Thickness Force Value (AVE - 3S) A 0.5Kg B 1.0Kg C 2.0Kg D 3.5Kg E 3.5Kg F 3.5Kg H 0.4Kg	Apply force as shown and record the force figure while the capacitor breaks. 

8.5 Bending:

Dielectrics	Specification	Testing Conditions
NPO	No remarkable visual damage Cp change $\pm 5\%$ (Cp>10pF) Cp change 0.5pF (Cp 10pF)	Solder the capacitor on testing substrate and put it on testing stand. The middle part of substrate shall successively be pressurized by pressurizing rod at a rated of about 0.2±0.1mm/sec. until the deflection become means of the 1.5±0.1mm and lease the pressurizing rod after 5±1 sec. To measure the capacitance. (Related STD.:JIS C 5101-10-1999)
X7R/X5R	No remarkable visual damage Cp change $\pm 12.5\%$	
Y5V	No remarkable visual damage Cp change $\pm 30\%$	



8.6 Solder-Ability:

Dielectrics	Specification	Testing Conditions
NPO X7R/X5R Y5V	95% min. coverage of both terminal electrodes and less than 5% have pin holes or rough spots	Solder temperature: 230±5 Dipping time: 2±1 seconds. Solder: Sn/Pb=63/37 Preheating: 80~120 10~30sec Completely soak both terminal electrodes in solder (Related STD.: JIS C 5101-1998)

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8.7 Resistance to Soldering Heat:

Dielectrics	Specification	Testing Conditions
NPO (Class1)	No remarkable visual damage Cp change within $\pm 2.5\%$ or $\pm 0.25\text{pF}$ whichever is larger Cp < 30pF, Q 400+20Cp; Cp 30pF, Q 1000 IR meet initial standard value	Solder temperature: 270 \pm 5 Dipping time: 10 \pm 1 seconds Solder: Sn/Pb=63/37 Measurement to be made after being kept at room temperature for 24 \pm 2 (Class 1) or 48 \pm 4(Class 2,3)hours.
X7R/X5R (Class2)	No remarkable visual damage Cp change within $\pm 7.5\%$ DF (Tan) meet initial standard value IR meet initial standard value	Recovery for the following period under the standard condition after test. (Related STD.: JIS C 5101-10-1999)
Y5V (Class3)	No remarkable visual damage Cp change within $\pm 20\%$ DF (Tan) meet initial standard value IR meet initial standard value	

8.8 Vibration:

Dielectrics	Specification	Testing Conditions
NPO (Class1)	No remarkable visual damage Cp change within $\pm 2.5\%$ or $\pm 0.25\text{pF}$ whichever is larger Cp < 30pF, Q 400+20Cp; Cp 30pF, Q 1000	Scope of Frequency: 10 ~ 55Hz Amplitude or Acceleration: 1.5mm \pm 15% Ratio of Swoop: 10 ~55 ~10Hz about 1 min. Test time: X,Y,Z Directions each 2hr.
X7R/X5R (Class2)	No remarkable visual damage Cp change within $\pm 5\%$ DF (Tan) meet initial standard value	(Related STD.: JIS C 5101-1998) JIS C0041 MIL-STD-202-204D)
Y5V (Class3)	No remarkable visual damage Cp change within $\pm 20\%$ DF (Tan) meet initial standard value	

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8.9 Temperature Cycle:

Dielectrics	Specification	Testing Conditions
NPO	No remarkable visual damage Cp change $\pm 2.5\%$ or $\pm 0.25\text{pF}$ whichever is larger Cp 30pF,Q 1000;Cp<30pF,Q 400+20Cp (Q=1/DF) IR initial standard value of IR	To perform 1000 cycles of the stated Environment Step temperature timing 1 -55 30min. 2 25 5min. 3 125 (/85 for X5R) 30min. 4 25 5min.
X7R/X5R	No remarkable visual damage Cp change $\pm 7.5\%$ DF 2.5% for 25V Above & 3.5% for 16V (Tan 0.025 for 25V Above & 0.035 for 16V) IR initial standard value of IR	Measurement to be made after being kept at room temperature for 24 \pm 2 hours (Related STD.: JIS C 5101-1998)
Y5V	No remarkable visual damage Cp change $\pm 20\%$ DF 5% for 25V Above & 7% for 16V (Tan 0.05 for 25V Above & 0.07 for 16V) IR initial standard value of IR	To perform 1000 cycles of the stated Environment Step temperature timing 1 -30 30min. 2 25 5min. 3 85 30min. 4 25 5min. Measurement to be made after being kept at room temperature for 24 \pm 2 hours (Related STD.: JIS C 5101-1998)

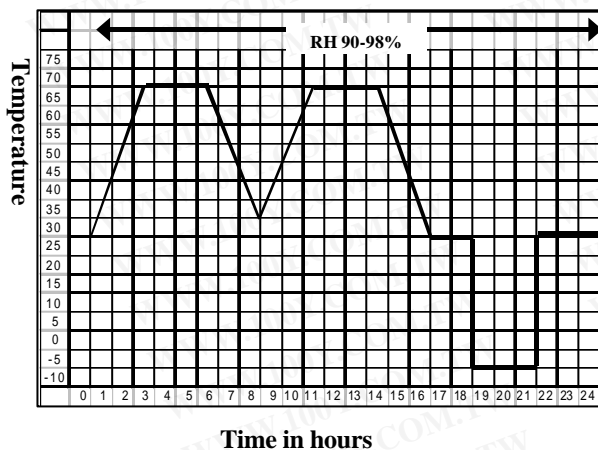
8.10 Moisture Resistance (steady state):

Dielectrics	Specification	Testing Conditions
NPO (Class1)	No remarkable visual damage Cp change $\pm 5\%$ or $\pm 0.5\text{pF}$ whichever is larger Cp 30pF,Q 350;10 Cp<30pF,Q 275+2.5C;Cp<10pF,Q 200+10Cp (Q=1/DF) R*C 50 or 1000M whichever is smaller	Testing temperature : 40 \pm 2 Humidity: 90 95% RH Testing time: 1000 hours Measurement to be made after being kept at room temperature for 24 \pm 2 (Class 1) or 48 \pm 4(Class 2,3)hours. (Related STD.: JIS C 5101-1998)
X7R /X5R (Class2)	No remarkable visual damage Cp change $\pm 12.5\%$ DF 5.0% (Tan 0.05) R*C 50 or 1000M whichever is smaller	
Y5V (Class3)	No remarkable visual damage Cp change $\pm 30\%$ DF 12.5%for10V or 6.3V(Tan 0.125) 10%for16V (Tan 0.10) 7.5%for25V Above (Tan 0.075) R*C 50 or 1000M whichever is smaller	

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8.11 Damp heat cyclic (temp. cyclic):

Dielectrics	Specification	Testing Conditions
NPO (Class1)	No remarkable visual damage Cp change $\pm 5\%$ or $\pm 0.5\text{pF}$ whichever is larger Cp 30pF,Q 200;Cp<30pF,Q 200+10Cp (Q=1/DF) R*C 50 or 1000M whichever is smaller	Testing temperature : 25 --> 2.5hrs. --> 65 (3hrs.) --> 2.5hrs. --> 25 --> 2.5hrs. --> 65 (3hrs.) --> 2.5hrs. --> 25 (2hrs.) --> -10 (3hrs.) --> 25 (3hrs.) Humidity: 90 98% RH Test cycle:10 continuous cycles Time of 1 cycle:24hrs. Measurement to be made after being kept at room temperature for 24 \pm 2 (Class 1) or 48 \pm 4(Class 2,3)hours.
X7R/X5R (Class2)	No remarkable visual damage Cp change $\pm 12.5\%$ DF 5.0% (Tan 0.05) R*C 50 or 1000M whichever is smaller	(Related STD.: JIS C 5101-1998)
Y5V (Class3)	No remarkable visual damage Cp change $\pm 30\%$ DF 12.5% for 10V or 6.3V (Tan 0.125) 10% for 16V (Tan 0.10) 7.5% for 25V Above (Tan 0.075) R*C 50 or 1000M whichever is smaller	



Stage	Time(h)	Temp.	Humidity
a	2.5	-	90~95%RH
b	3.0	65	90~95%RH
c	2.5	-	90~95%RH
d	2.5	-	90~95%RH
e	3.0	65	90~95%RH
f	2.5	-	90~95%RH
g	1~4	25	90~95%RH
h	3.0	-10	Optional
i	1~4	25	90~95%RH

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8.12 Damp heat with load :

Dielectrics	Specification	Testing Conditions
NPO (Class1)	No remarkable visual damage Cp change $\pm 7.5\%$ or $\pm 0.75\text{pF}$ whichever is larger Cp 30pF,Q 200;Cp<30pF,Q 200+10/3*Cp R*C 25 M u For 500M whichever is smaller	Testing temperature : 40 ± 2 Humidity: 90 95% RH Voltage:100% of the rated voltage Testing time: 1000 hours Measurement to be made after being kept at room temperature for 24 ± 2 (Class1) or 48 ± 4 (Class 2,3)hours. (Related STD. JIS C 5101-1998)
X7R/X5R (Class2)	No remarkable visual damage Cp change $\pm 12.5\%$ DF 5.0%;7.5%(X5R) (Tan 0.05;0.075) R*C 25 M uFor 500M whichever is smaller	
Y5V (Class3)	No remarkable visual damage Cp change $\pm 30\%$ DF 12.5% for 10V or 6.3V (Tan 0.125) 10% for 16V (Tan 0.10) 7.5% for 25V Above (Tan 0.075) R*C 25 M uFor 500M whichever is smaller	

8.13 Life Test:

Dielectrics	Specification	Testing Conditions
NPO	No remarkable visual damage Cp change $\pm 3\%$ or $\pm 0.3\text{pF}$ whichever is larger Q 350 (Cp 30pF) ; Q 275+(2.5*Cp) (10pF Cp<30pF) ; Q 200+(10*Cp) (Cp<10pF) (Cp<10pF) ;(Q=1/DF) R*C 50 or 1000M whichever is smaller	Testing temperature: 125 ± 3 200% of the rated voltage Testing time: 1000hrs Measurement to be made after being kept at room temperature for 24 ± 2 hours
X7R/X5R	No remarkable visual damage Cp change $\pm 12.5\%$ DF 4% for 25V Above & 5% for 16V(X5R) (Tan 0.04 for 25V Above & 0.05 for 16V) R*C 50 or 1000M whichever is smaller	Testing temperature: 125 ± 3 200% of the rated voltage Testing time: 1000hrs Measurement to be made after being kept at room temperature for 48 ± 2 hours
Y5V	No remarkable visual damage Cp change $\pm 30\%$ DF 7.5% for 25V Above & 10% for 16V (Tan 0.075 for 25V Above & 0.10 for 16V) R*C 50 or 1000M whichever is smaller	Testing temperature: 85 ± 3 200% of the rated voltage Testing time: 1000hrs Measurement to be made after being kept at room temperature for 48 ± 2 hours

Theory : (based upon empirical formula modelled by Prokopowicz & Vaskas)

$$t_1/t_2 = (V_2/V_1)^n * \exp(E_s/k(1/T_1 - 1/T_2))$$

E_s = Pseudo activation energy

K = Boltzman's Constant

Subscripts 1 and 2 refer to test conditions. (simplified to $t_1/t_2 = (V_2/V_1)^3 * 10 * \exp((T_1 - T_2)/20)$)

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The equivalent device-hrs:

T=Fa*n*t

T=Equivalent device hours

N=No. of devices under test

t=Test duration in hrs

Fa=Acceleration factor= $(V_{test}/V_{op})^3 * 10 * \exp((T_{test}-T_{op})/20)$

T_{test}=Test temperature

T_{op}=Operating temperature

The formula for the failure rate is:

F = n/T*k*10⁹ FITS

n = Total number of cumulative failures in the test

T = Accumulated device-hours

K = Coefficient of confidence level (n*K=0.917 if n=0)

The coefficient K at 60% confidence level can be found from Table1.

No. of Failure	K	No. of Failure	K
1	2.02	6	1.22
2	1.56	7	1.19
3	1.39	8	1.18
4	1.31	9	1.175
5	1.26	10	1.17

Table1

EX.

The predicted failure rates in failures per billion device-hrs at 15V, 25 operation, based on total number of cumulative failures at the end of normal life testing (1000hr).

Dielectrics	Rate Voltage	No. of Failure	FIT LIFE
NPO,X7R	25V	0	0.167FIT
	50V	0	0.021FIT

9. Precautions on the use of MLCC:

9.1 Suggested soldering profile:

9.1.1 Hand soldering:

when correcting chips with a soldering iron, no preheating is required if the following conditions are met.

Item	Conditions	
Chip size	2.0 × 1.33mm max.	3.2 × 1.6mm over
Temperature of iron-tip	300 max.	270 max.
Soldering iron wattage	20W max.	
Caution	Do not allow the iron-tip to directly touch the ceramic element.	

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9.1.2 Soldering:

(solder Buildup)

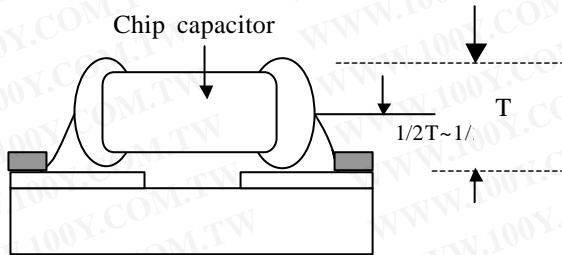
(1) Dip and iron soldering

Use as little solder as possible, and confirm that the solder is securely placed.

(2) Reflow soldering

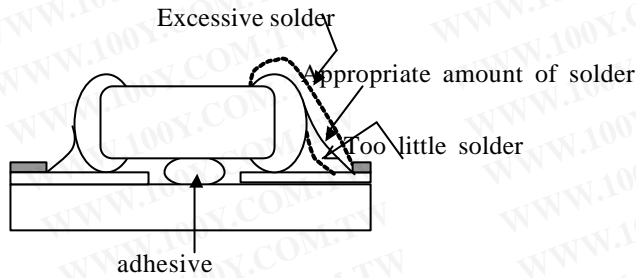
When soldering confirm that the solder is placed over 0.2 to 0.3mm of the surface of the terminations.

(3) Examples of good and bad solder application.



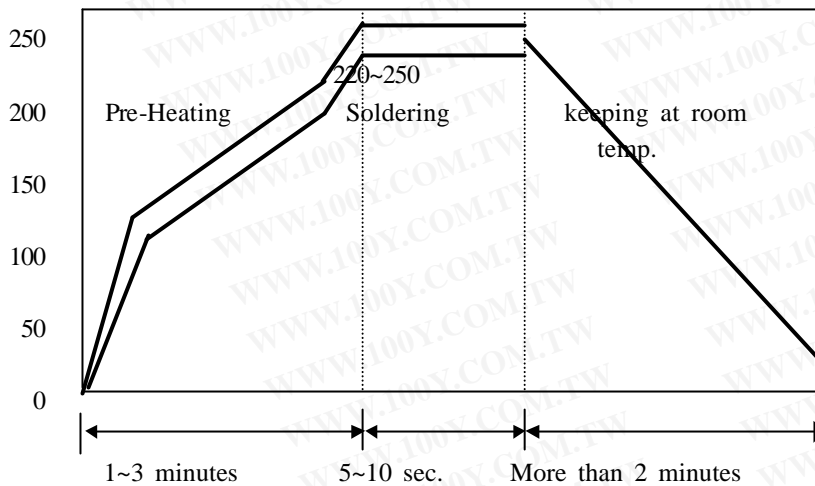
The ideal condition is to have solder mass controlled to 1/2 to 1/3 of the thick-ness of the capacitor.

Solder buildup by reflow

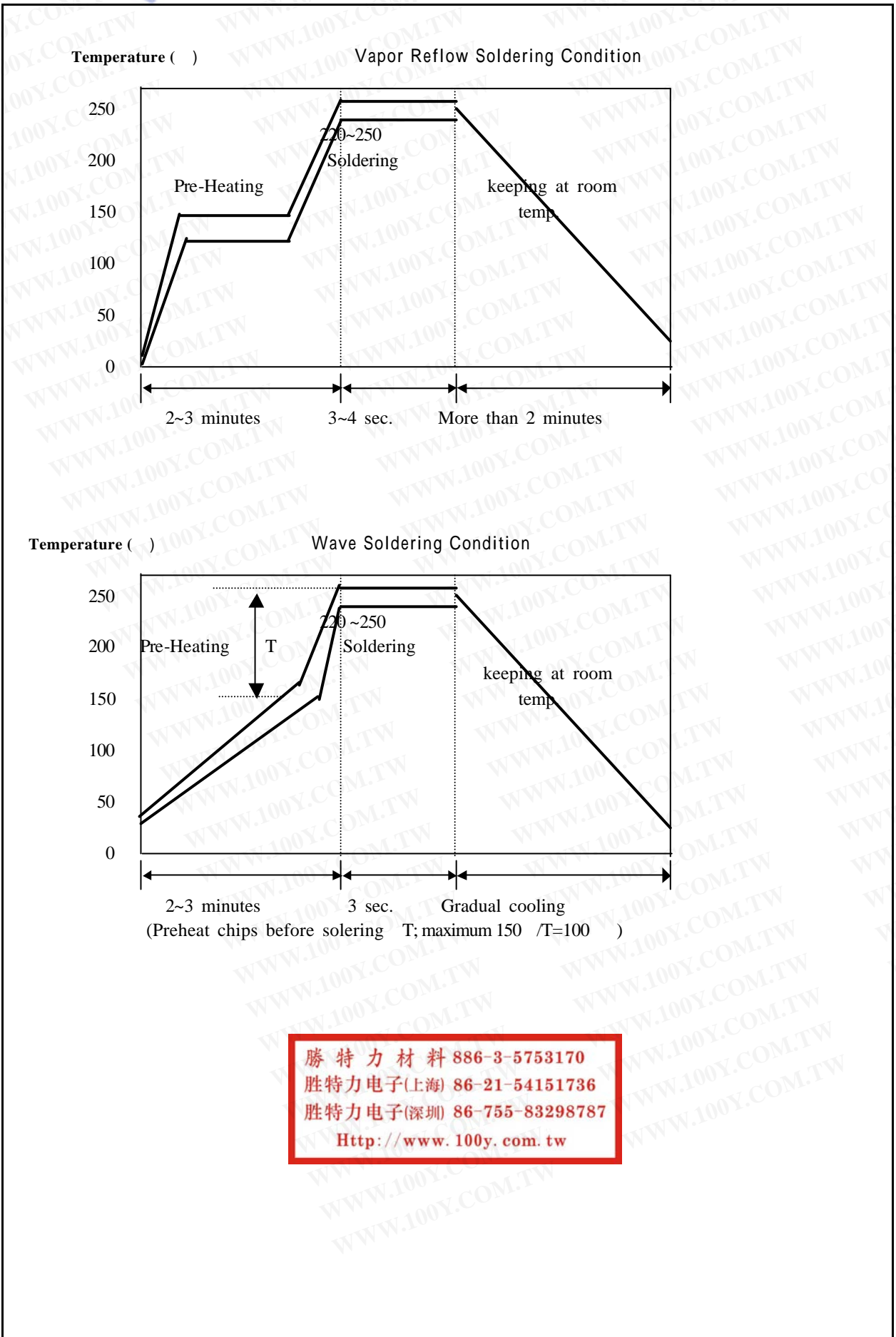


Temperature ()

Infrared Reflow Soldering Condition



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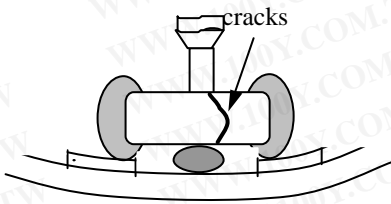
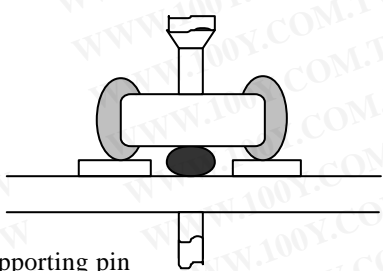
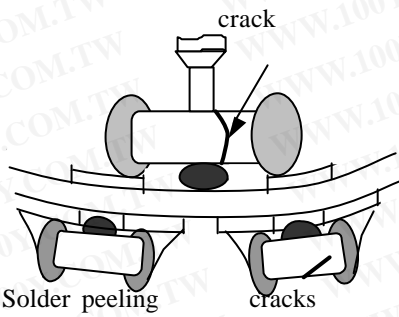
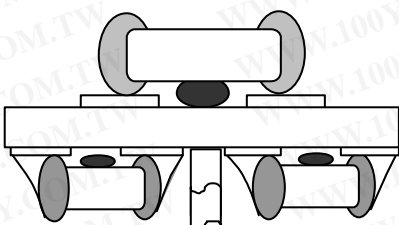


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9.2 Consideration for automatic placement:

Adjustment of mounting machine

- 1.Excessive impact load should not be imposed on the capacitors when mounting onto the PC boards.
- 2.The maintenance and inspection of the mounters should be conducted periodically.

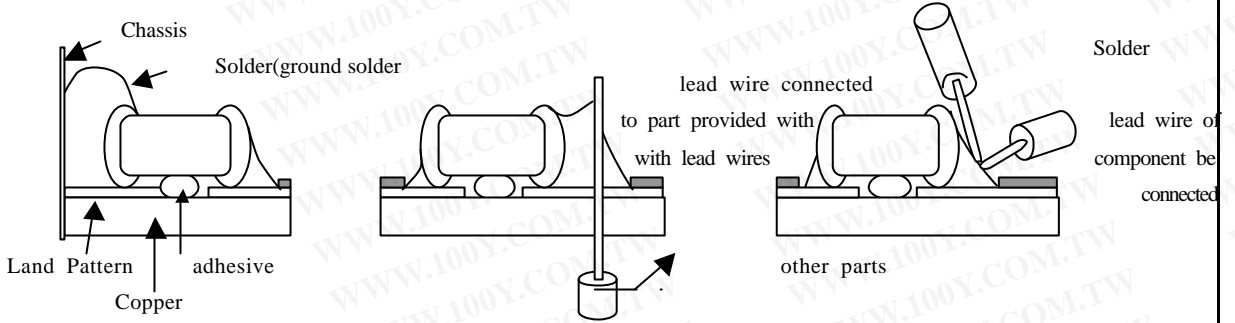
	Not recommended	Recommended
Single-sided Mounting		
Double-sided Mounting		

9.3 PCB design:

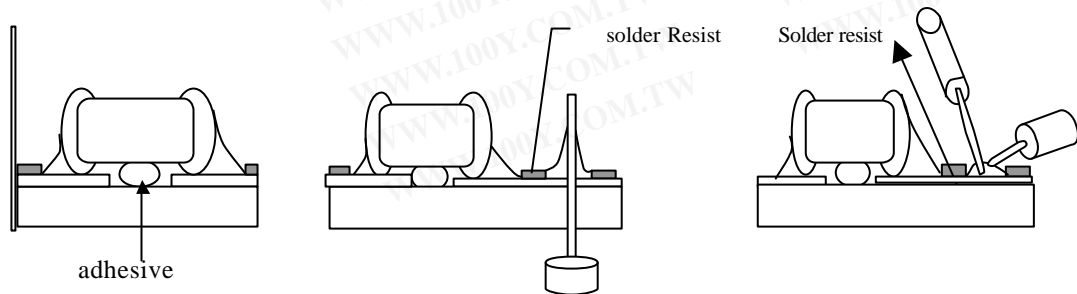
9.3.1 PCB design:

Solder buildup by folw method and soldering methods
Example of soldering to be avoid

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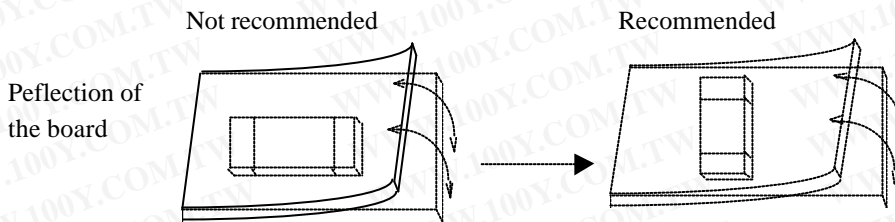


Example of correct soldering

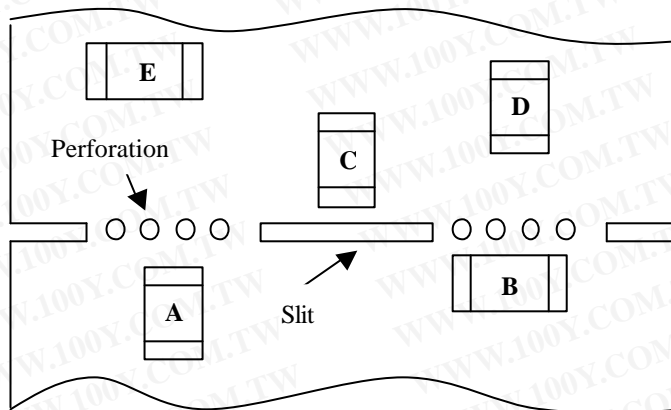


9.3.2 Pattern Configurations:

The following are examples of good and bad capacitor layout; SMD capacitors should be located to minimize any possible mechanical stress from board warp or deflection.



The example below shows recommendations for better design.



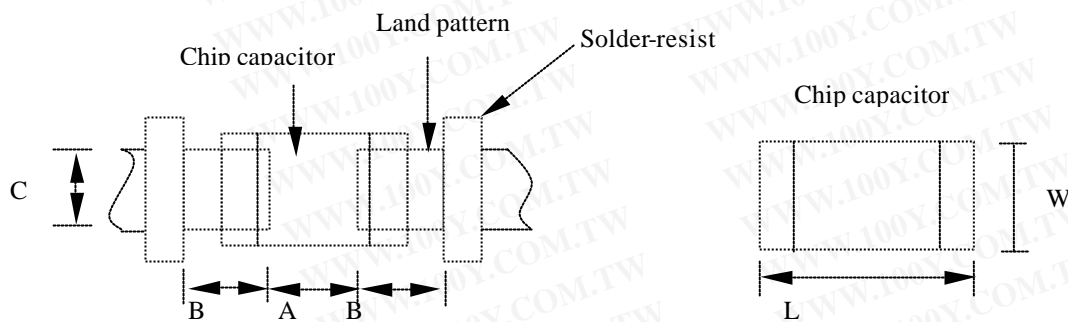
Magnitude of stress $A > B = C > D > E$

9.3.3. Design of Land-patterns :

The following diagrams and tables show some examples of recommended patterns to prevent excessive solder amounts. (larger fillets which extend above the component end terminations)

Examples of improper design are shown.

Recommended land dimensions for a typical chip capacitor land patterns for PCBs



Recommended land dimensions for wave-soldering (unit:mm)

Type		0603	0805	1206	1210
Size	L	1.6	2.0	3.2	3.2
	W	0.8	1.25	1.6	2.5
A		0.8~1.0	1.0~1.4	1.8~2.5	1.8~2.5
B		0.5~0.8	0.8~1.5	0.8~1.7	0.8~1.7
C		0.6~0.8	0.9~1.2	1.2~1.6	1.8~2.5

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Recommend land dimensions for reflow-soldering (unit:mm)

Type		0402	0603	0805	1206	1210	1812	(2220)
Size	L	1.0	1.6	2.0	3.2	3.2	4.5	5.5
	W	0.5	0.8	1.25	1.6	2.5	3.2	5.0
A		0.45~0.55	0.6~0.8	0.8~1.2	1.8~2.5	1.8~2.5	2.5~3.5	3.7~4.7
B		0.40~0.50	0.6~0.8	0.8~1.2	1.0~1.5	1.0~1.5	1.5~1.8	1.5~2.3
C		0.45~0.55	0.6~0.8	0.9~1.6	1.2~2.0	1.2~2.0	2.3~3.5	3.5~5.5

Excess solder can affect the ability of chips to withstand mechanical stresses. Therefore, please take proper precautions when land-patterns.

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10. Packing:

10.1 Bulk Packing:

Standard packing 10K & 15K pcs/cartridge; others are according to customer request.

10.2 Tape Packing:

Chip Size : 0402 , 0603 , 0805 , 1206 , 1210 , 1812.

Reel Size : 7" diameter standard and 13" available.

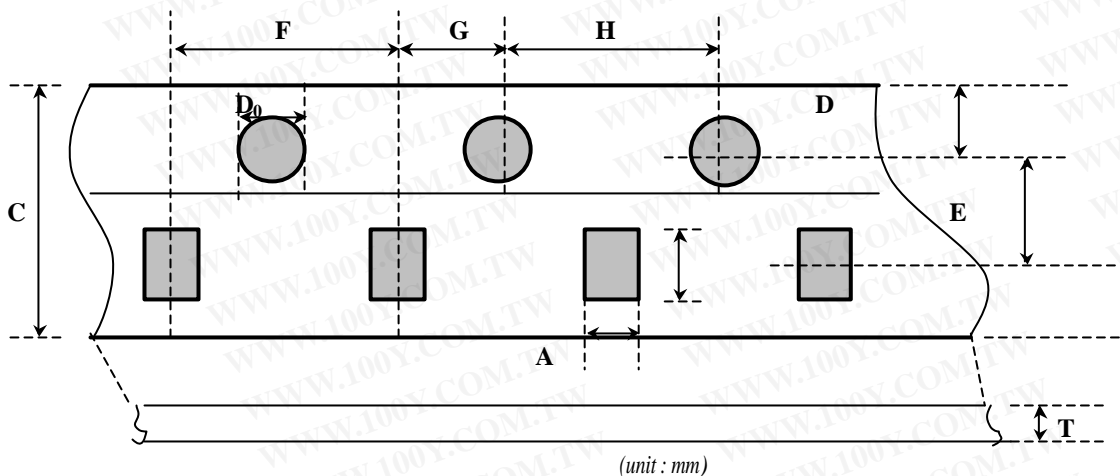
Tape width : 8mm/12mm tape width

Paper Tape: Standard taping (8mm paper width) suitable to 0603,0805and 1206, 4K pcs/reel

To 0402, 10K pcs/reel.

Plastic Tape: Suitable all sizes , particularly for chip thickness over 1mm,4K pcs/reel or 3K pcs/reel are available.

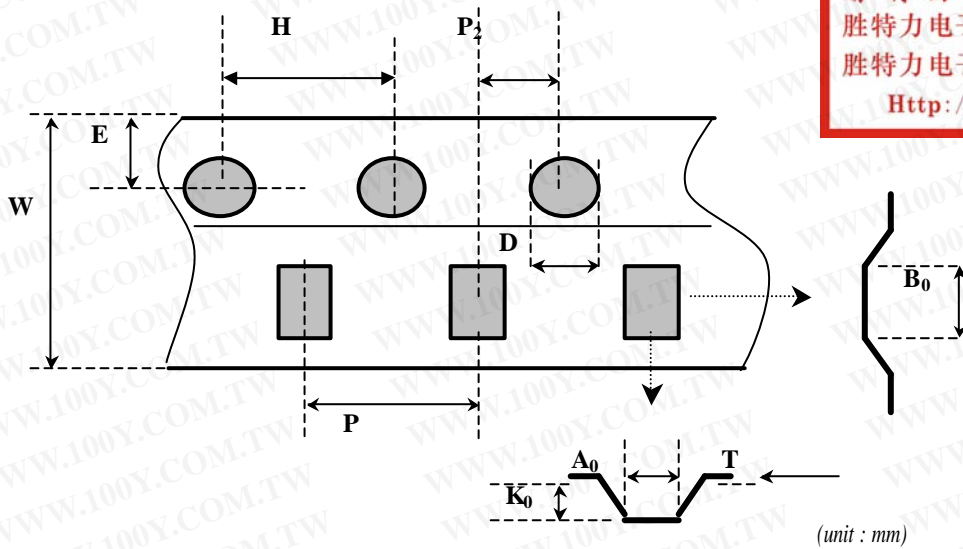
10.2.1 Dimensions of Packing Paper (paper tape):



(unit : mm)

Chip Size	0402	0603	0805	1206
Mark	H type	B type	B type	B type
A (Width of Compartment)	0.65±0.10	1.02±0.10	1.50±0.10	2.00±0.20
B (Length of Compartment)	1.15±0.10	1.81±0.10	2.30±0.10	3.50±0.20
C (Tape width)	8.00±0.10			
D (Distance between a sprocket hole and the upper edge of the tape)	1.75±0.10			
D ₀ (Diameter of sprocket hole)	1.50+0.10/-0			
E (Distance between centers of a Sprocket hole and chip hole)	3.50±0.10			
F (Compartment pitch)	2.00±0.10	4.00±0.10		
G (Distance between centers of a Sprocket hole and chip hole)	1.00±0.10	2.00±0.10		
H (Sprocket hole pitch)	4.00±0.10			
T (Paper tape thickness H type :~0.5mm ; B type :~0.82mm)	0.60±0.05	0.95±0.05	0.95±0.05	0.95±0.05

10.2.2 Dimensions of Embossed Packing (plastic tape):

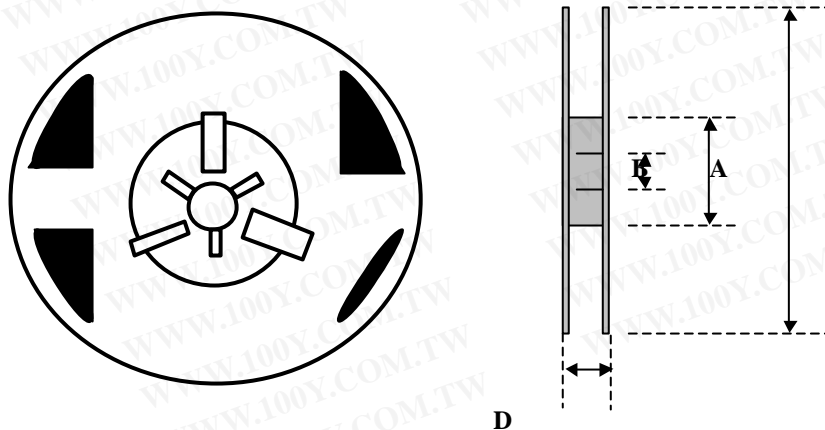


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Chip Size	0805	1206	1206	1210	1210	1812	1812
Mark	C Type	C Type	D Type	C Type	D Type	C Type	D Type
A_0 (Width of compartment)	145±0.20	1.80±0.20	1.88±0.20	2.75±0.20	2.68±0.20	3.65±0.20	3.66±0.20
B_0 (Length of compartment)	2.30±0.20	3.50±0.20	3.53±0.20	3.55±0.20	3.46±0.20	4.69±0.20	4.95±0.20
K_0 (Depth of compartment)	1.35±0.20	1.50±0.20	1.88±0.20	1.55±0.20	1.74±0.20	1.40±0.20	1.74±0.20
D (Diameter of sprocket hole)	1.50+0.10/-0						
W (Tape width)	8.00±0.20						
P (Compartment pitch)	4.00±0.10						
P_2 (Distance between centers of a Sprocket hole and chip hole)	2.00±0.10						
E (Distance between a sprocket hole and the upper edge of the tape)	1.75±0.10						
T (Tape thickness)	0.23±0.10						
H (Sprocket hole pitch)	4.00±0.10						

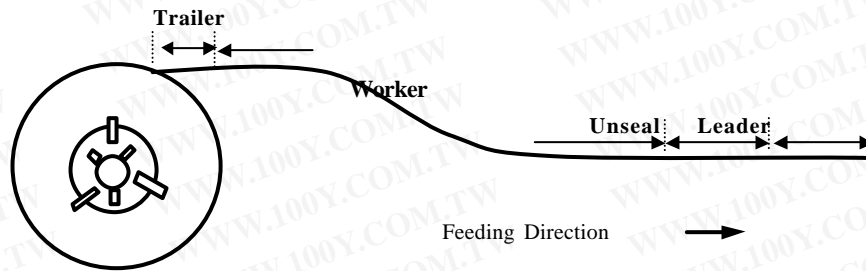
(unit : mm)

10.2.3 Dimensions of Reel: (Related STD.:EIAJ ETX-7001 / JIS C 0806 / JIS K 6870)



Reel size	A	B	C	D
7"	178.0±2.0mm	60.0±5.0mm	13.0±0.8mm	9.0±0.8mm
13"	330.0±4.0mm	50~90mm	13.5±0.8mm	9.5±0.8mm

10.2.4 Taping Figure:



packing	Chip quantity		Minimum number of Empty compartments		
	Worker (PCS)		Trailer	Unseal	Leader
Paper	A	1000	50 min.	50 min.	50 min.
	B	2000			
	C	3000			
	D	4000			
	E	15000			
	I	10000			
Emboss (plastic)	A	1000	20 min.	20 min.	20 min.
	B	2000			
	C	3000			

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10.2.5 Performance of Taping(JIS C 0806-3)

10.2.5.1.Strength of Carrier Tape and Top Cover Tape

10.2.5.1.1.Carrier Tape

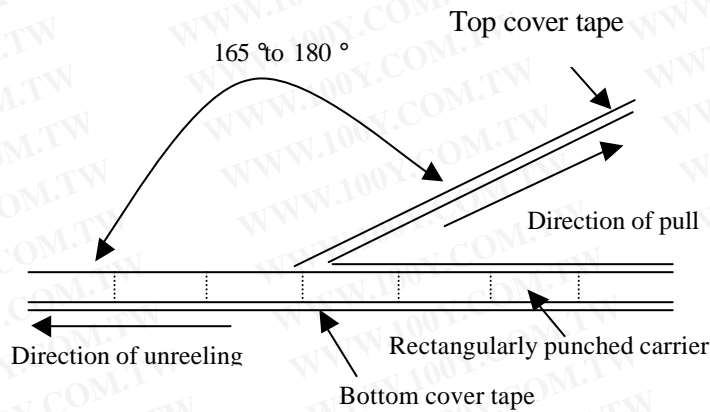
When a tensile force 1.02kgf is applied in the direction of unreeling the tape, the tape shall withstand this force.

10.2.5.1.2.Top cover Tape

When a tensile force 1.02kgf is applied to the tape, the tape shall withstand this force.

10.2.5.2. Peel Force of Top Cover Tape


Unless otherwise specified, the peel force of top cover tape shall be 10.2 to 71.4 gf when the top cover tape is pulled at a speed of 300mm/min with the angle between the taped during peel and the direction of unreeling maintained at 165 to 180 degrees as illustrated in Fig.



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10.2.6 Reel Label:

10.2.6.1 Lable:

 P/N:0603B103K500BD	
C/N: C/O: VCD: 50 TOL: +/-10% LOT	CAP: 0.01UF QTY:4K

The Contents of label

P/N	The part no of Team Young
C/N	The part no of user
C/O	The purchasing order no of User
VCD	Rated voltage
CAP	Capacitance
TOL	Tolerance
Q'TY	Quantity
LOT	The lot no of Team Young

10.2.6.2 Bar Code:

	
L/N:CA010390B P/N:3B103K	QTY:4K

The Contents of Bar code

L/N	Lot no of Team Young
P/N	Part no of Team Young
Q'TY	Quantity

11. Package:

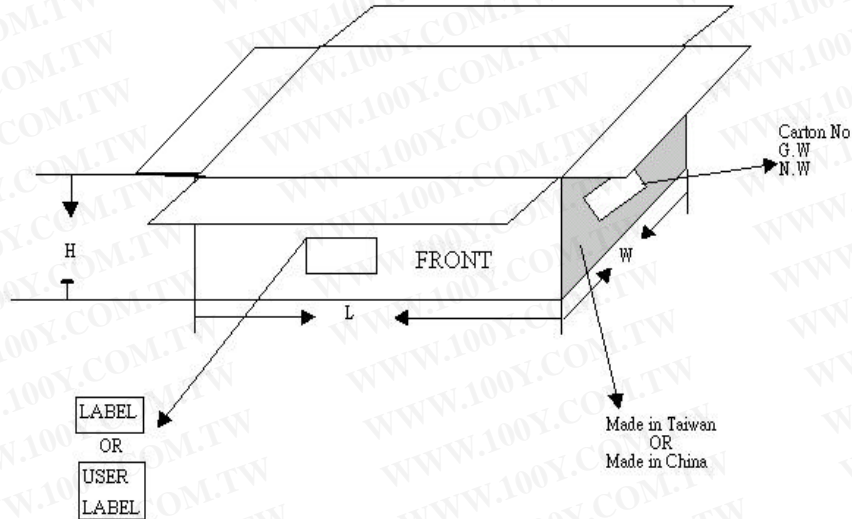
11.1 Carton:

11.1.1 Carton Size:

L	W	H
38cm	37cm	21.5cm

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11.1.2 The Quantity :200K/one carton:



1 INNER BOX=20,000PCS
 1 CARTON=20,000PCS x 10BOX=200,000PCS

11.1.3 The Label in Carton:

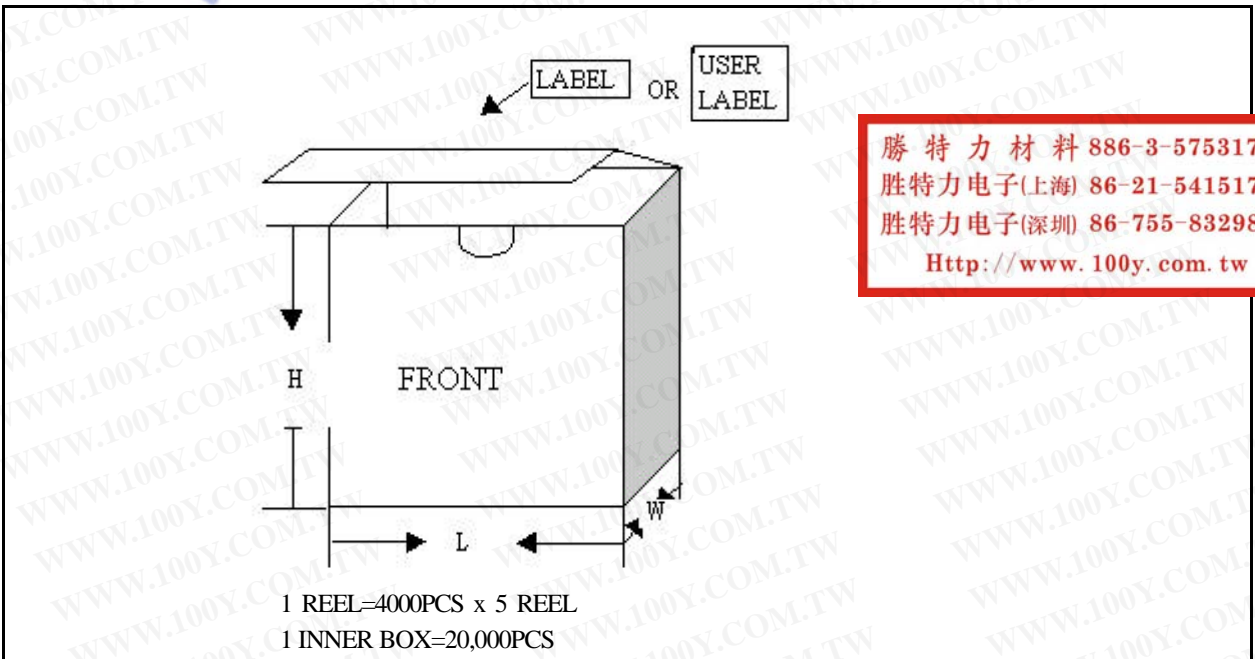
TEAM YOUNG	
P/N:0603B103K500BD	
C/N:	
C/O:	
VCD: 50	CAP: 0.01UF
TOL: +/-10%	QTY:200K
LOT	

11.2 Inner Box:

11.2.1 Size:


L	W	H
18cm	6.8cm	19cm

11.2.2 The Quantily:20K/One Box:



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11.2.3 The Label in Iner Box

 P/N:0603B103K500BD	
C/N:	
C/O:	
VCD: 50	CAP: 0.01UF
TOL: +/-10%	QTY:20K
LOT	

11.3 Country of origin and Label:

11.3.1 Label:

(example)

XXX Code	: VC**CY*****T
Produce Name	: Multi-layer Ceramic Capacitors
Maker Part no	: 0603*****
Maker Name	: Team Young Advanced Ceramics Co.,Ltd
Country of origin	: Taiwan
	: China-Kunshan
	: China-Dongguan

11.3.2 Label Location:

Reel		Inner Box		Carton	
YES	NO	YES	NO	YES	NO

12. Warranty:

Team Young will replace all chip capacitor that is defective in manufacturing, labeling or packing. You may call us toll free at **080-321-330 (080-321-331)** for assistance.

" Team Young will not use the material which has ozonosphere damage concerned ".

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