MOTOROLA

SN54/74LS160A
SN54/74LS161A
SN54/74LS162A
SN54/74LS163A

BCD DECADE COUNTERS/ 4-BIT BINARY COUNTERS

The LS160A/161A/162A/163A are high-speed 4-bit synchronous counters. They are edge-triggered, synchronously presettable, and cascadable MSI building blocks for counting, memory addressing, frequency division and other applications. The LS160A and LS162A count modulo 10 (BCD). The LS161A and LS163A count modulo 16 (binary.)

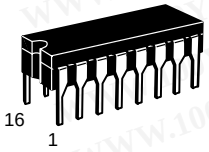
The LS160A and LS161A have an asynchronous Master Reset (Clear) input that overrides, and is independent of, the clock and all other control inputs. The LS162A and LS163A have a Synchronous Reset (Clear) input that overrides all other control inputs, but is active only during the rising clock edge.

	BCD (Modulo 10)	Binary (Modulo 16)
Asynchronous Reset	LS160A	LS161A
Synchronous Reset	LS162A	LS163A

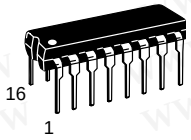
- Synchronous Counting and Loading
- Two Count Enable Inputs for High Speed Synchronous Expansion
- Terminal Count Fully Decoded
- Edge-Triggered Operation
- Typical Count Rate of 35 MHz
- ESD > 3500 Volts

BCD DECADE COUNTERS/ 4-BIT BINARY COUNTERS

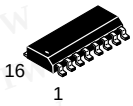
LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08

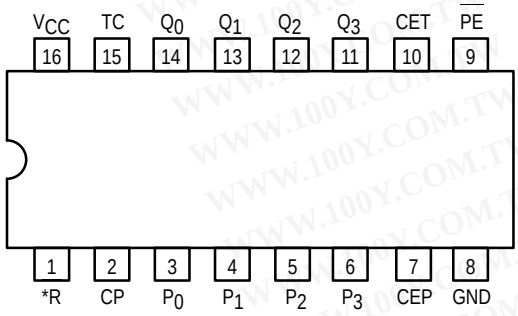


D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

SN54LSXXXJ	Ceramic
SN74LSXXXN	Plastic
SN74LSXXXD	SOIC

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

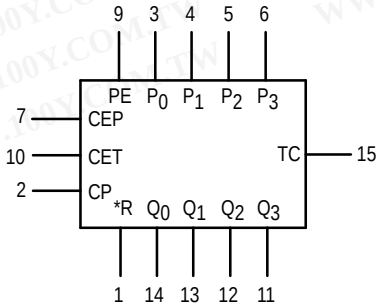
*MR for LS160A and LS161A
*SR for LS162A and LS163A

PIN NAMES

		LOADING (Note a) HIGH	LOW
$\overline{PE}$	Parallel Enable (Active LOW) Input	1.0 U.L.	0.5 U.L.
P_0-P_3	Parallel Inputs	0.5 U.L.	0.25 U.L.
CEP	Count Enable Parallel Input	0.5 U.L.	0.25 U.L.
CET	Count Enable Trickle Input	1.0 U.L.	0.5 U.L.
$\underline{CP}$	Clock (Active HIGH Going Edge) Input	0.5 U.L.	0.25 U.L.
$\underline{MR}$	Master Reset (Active LOW) Input	0.5 U.L.	0.25 U.L.
SR	Synchronous Reset (Active LOW) Input	1.0 U.L.	0.5 U.L.
Q_0-Q_3	Parallel Outputs (Note b)	10 U.L.	5 (2.5) U.L.
TC	Terminal Count Output (Note b)	10 U.L.	5 (2.5) U.L.

NOTES:
a) 1 TTL Unit Load (U.L.) = 40 µA HIGH/1.6 mA LOW.
b) The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

LOGIC SYMBOL



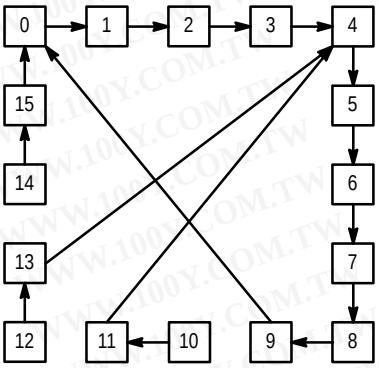
VCC = PIN 16
GND = PIN 8

*MR for LS160A and LS161A
*SR for LS162A and LS163A

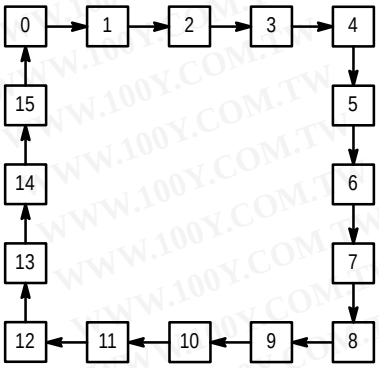
SN54/74LS160A • SN54/74LS161A
SN54/74LS162A • SN54/74LS163A

STATE DIAGRAM

LS160A • LS162A



LS161A • LS163A



LOGIC EQUATIONS

Count Enable = CEP • CET • PE
TC for LS160A & LS162A = CET • Q_0 • $\overline{Q_1}$ • $\overline{Q_2}$ • Q_3
TC for LS161A & LS163A = CET • Q_0 • Q_1 • Q_2 • Q_3
Preset = $\overline{PE}$ • CP + (rising clock edge)
Reset = $\overline{MR}$ (LS160A & LS161A)
Reset = SR • CP + (rising clock edge)
(LS162A & LS163A)

NOTE:
The LS160A and LS162A can be preset to any state, but will not count beyond 9. If preset to state 10, 11, 12, 13, 14, or 15, it will return to its normal sequence within two clock pulses.

FUNCTIONAL DESCRIPTION

The LS160A/161A/162A/163A are 4-bit synchronous counters with a synchronous Parallel Enable (Load) feature. The counters consist of four edge-triggered D flip-flops with the appropriate data routing networks feeding the D inputs. All changes of the Q outputs (except due to the asynchronous Master Reset in the LS160A and LS161A) occur as a result of, and synchronous with, the LOW to HIGH transition of the Clock input (CP). As long as the set-up time requirements are met, there are no special timing or activity constraints on any of the mode control or data inputs.

Three control inputs — Parallel Enable ($\overline{PE}$), Count Enable Parallel (CEP) and Count Enable Trickle (CET) — select the mode of operation as shown in the tables below. The Count Mode is enabled when the CEP, CET, and PE inputs are HIGH. When the $\overline{PE}$ is LOW, the counters will synchronously load the data from the parallel inputs into the flip-flops on the LOW to HIGH transition of the clock. Either the CEP or CET can be used to inhibit the count sequence. With the PE held HIGH, a LOW on either the CEP or CET inputs at least one set-up time prior to the LOW to HIGH clock transition will cause the existing output states to be retained. The AND feature of the two Count Enable inputs (CET•CEP) allows synchronous cascading without external gating and without delay accumulation over any practical number of bits or digits.

The Terminal Count (TC) output is HIGH when the Count Enable Trickle (CET) input is HIGH while the counter is in its maximum count state (HLLH for the BCD counters, HHHH for the Binary counters). Note that TC is fully decoded and will, therefore, be HIGH only for one count state.

The LS160A and LS162A count modulo 10 following a binary coded decimal (BCD) sequence. They generate a TC output when the CET input is HIGH while the counter is in state 9 (HLLH). From this state they increment to state 0 (LLLL). If loaded with a code in excess of 9 they return to their legitimate sequence within two counts, as explained in the state diagram. States 10 through 15 do *not* generate a TC output.

The LS161A and LS163A count modulo 16 following a binary sequence. They generate a TC when the CET input is HIGH while the counter is in state 15 (HHHH). From this state they increment to state 0 (LLLL).

The Master Reset ($\overline{MR}$) of the LS160A and LS161A is asynchronous. When the $\overline{MR}$ is LOW, it overrides all other input conditions and sets the outputs LOW. The $\overline{MR}$ pin should never be left open. If not used, the $\overline{MR}$ pin should be tied through a resistor to V_{CC}, or to a gate output which is permanently set to a HIGH logic level.

The active LOW Synchronous Reset ($\overline{SR}$) input of the LS162A and LS163A acts as an edge-triggered control input, overriding CET, CEP and PE, and resetting the four counter flip-flops on the LOW to HIGH transition of the clock. This simplifies the design from race-free logic controlled reset circuits, e.g., to reset the counter synchronously after reaching a predetermined value.

MODE SELECT TABLE

*SR	PE	CET	CEP	Action on the Rising Clock Edge (⌐)
L	X	X	X	RESET (Clear)
H	L	X	X	LOAD ($P_n \rightarrow Q_n$)
H	H	H	H	COUNT (Increment)
H	H	L	X	NO CHANGE (Hold)
H	H	X	L	NO CHANGE (Hold)

*For the LS162A and LS163A only.

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

LS160A and LS161A
DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits Min	Limits Typ	Limits Max	Unit	Test Conditions	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.7	3.5		V		
V_{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current MR, Data, CEP, Clock PE, CET				20 40	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
	MR, Data, CEP, Clock PE, CET				0.1 0.2	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current MR, Data, CEP, Clock PE, CET				−0.4 −0.8	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Short Circuit Current (Note 1)		−20		−100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current Total, Output HIGH Total, Output LOW				31 32	mA	V_{CC} = MAX	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

LS162A and LS163A

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits Min	Limits Typ	Limits Max	Unit	Test Conditions	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.7	3.5		V		
V_{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current Data, CEP, Clock PE, CET, SR				20 40	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
	Data, CEP, Clock PE, CET, SR				0.1 0.2	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current Data, CEP, Clock, $\overline{PE}$, $\overline{SR}$ CET				−0.4 −0.8	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Short Circuit Current (Note 1)		−20		−100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current Total, Output HIGH Total, Output LOW				31 32	mA	V_{CC} = MAX	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C)

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
f_{MAX}	Maximum Clock Frequency	25	32		MHz	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay Clock to TC		20 18	35 35	ns	
t_{PLH} t_{PHL}	Propagation Delay Clock to Q		13 18	24 27	ns	
t_{PLH} t_{PHL}	Propagation Delay CET to TC		9.0 9.0	14 14	ns	
t_{PHL}	$\overline{MR}$ or $\overline{SR}$ to Q		20	28	ns	

AC SETUP REQUIREMENTS (T_A = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t_WCP	Clock Pulse Width Low	25			ns	V_{CC} = 5.0 V
t_W	MR or SR Pulse Width	20			ns	
t_s	Setup Time, other*	20			ns	
t_s	Setup Time PE or SR	25			ns	
t_h	Hold Time, data	3			ns	
t_h	Hold Time, other	0			ns	
t_{rec}	Recovery Time MR to CP	15			ns	

*CEP, CET or DATA

DEFINITION OF TERMS

SETUP TIME (t_s) — is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) — is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

RECOVERY TIME (t_{rec}) — is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW to HIGH in order to recognize and transfer HIGH Data to the Q outputs.

AC WAVEFORMS

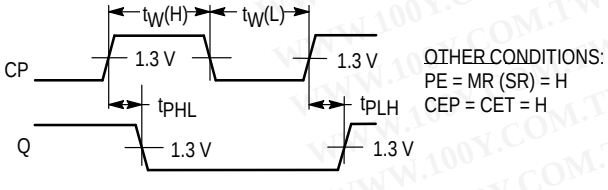


Figure 1. Clock to Output Delays, Count Frequency, and Clock Pulse Width

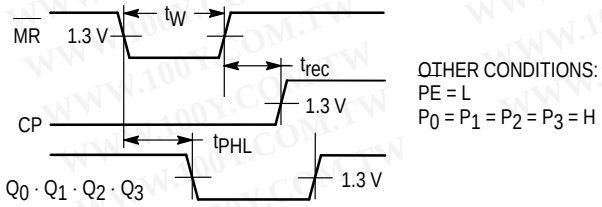


Figure 2. Master Reset to Output Delay, Master Reset Pulse Width, and Master Reset Recovery Time

AC WAVEFORMS (continued)

COUNT ENABLE TRICKLE INPUT TO TERMINAL COUNT OUTPUT DELAYS

The positive TC pulse occurs when the outputs are in the (Q_0 • Q_1 • Q_2 • Q_3) state for the LS160 and LS162 and the (Q_0 • Q_1 • Q_2 • Q_3) state for the LS161 and LS163.

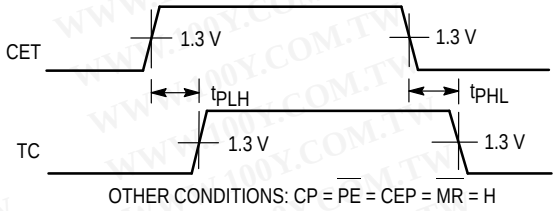


Figure 3

CLOCK TO TERMINAL COUNT DELAYS

The positive TC pulse is coincident with the output state (Q_0 • Q_1 • Q_2 • Q_3) state for the LS161 and LS163 and (Q_0 • Q_1 • Q_2 • Q_3) for the LS161 and LS163.

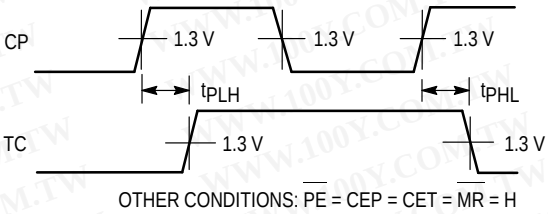


Figure 4

SETUP TIME (t_s) AND HOLD TIME (t_h) FOR PARALLEL DATA INPUTS

The shaded areas indicate when the input is permitted to change for predictable output performance.

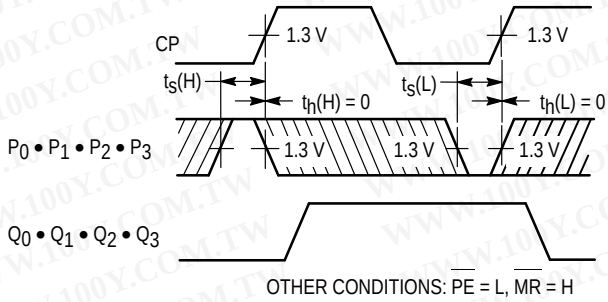


Figure 5

SETUP TIME (t_s) AND HOLD TIME (t_h) FOR COUNT ENABLE (CEP) AND (CET) AND PARALLEL ENABLE (PE) INPUTS

The shaded areas indicate when the input is permitted to change for predictable output performance.

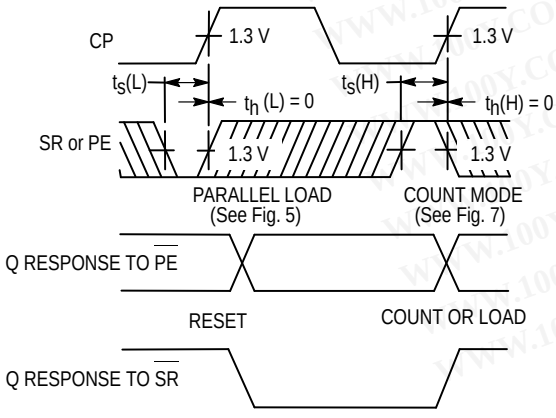


Figure 6

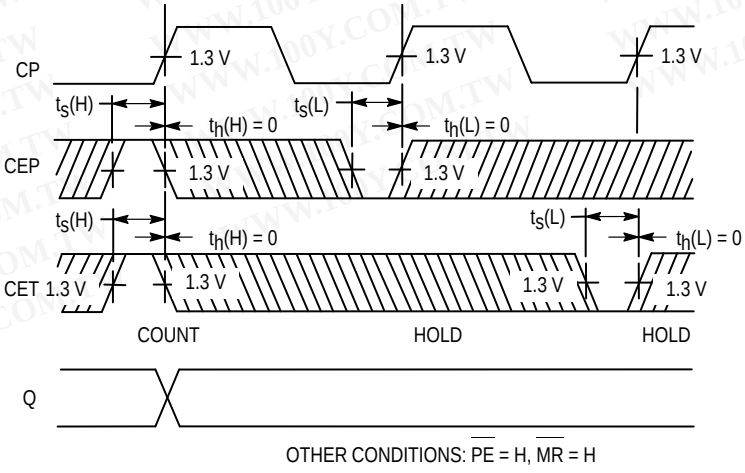


Figure 7