- Contains Eight Flip-Flops With Single-Rail Outputs
- Buffered Clock and Direct Clear Inputs
- Individual Data Input to Each Flip-Flop
- Applications Include: Buffer/Storage Registers Shift Registers Pattern Generators

#### description

These monolithic, positive-edge-triggered flipflops utilize TTL circuitry to implement D-type flip-flop logic with a direct clear input.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect ar the output.

These flip-flops are guaranteed to respond to clock frequencies ranging form 0 to 30 megahertz while maximum clock frequency is typically 40 megahertz. Typical power dissipation is 39 milliwatts per flip-flop for the '273 and 10 milliwatts for the 'LS273.

FUNCTION TABLE (each flip-flop)

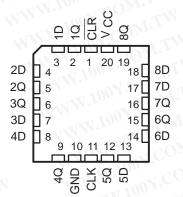
	loaonn		-/
WW.	NPUTS	ON.	OUTPUT
CLEAR	CLOCK	D	Q
	X	Х	TT.
H	1	H	Н
H	1	J L	L
н	WL100	Х	Q <sub>0</sub>

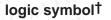
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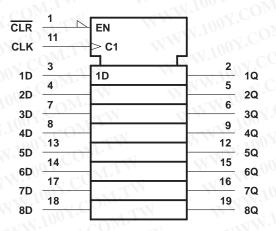
SN7427 SN74LS273 .	73 N PA	N PACKAGE
CLR [	1 20	) V <sub>CC</sub>
1Q [	2 19	) 8Q
1D ]	3 18	1 8D

9	10	100
	17	]7D
5	16	]7Q
6	15	] 6Q
7	14	] 6D
8	13	] 5D
9	12	] 5Q
10	11	] CLK
	5 6 7 8 9	5 16 6 15 7 14 8 13 9 12

SN54LS273 . . . FK PACKAGE (TOP VIEW)







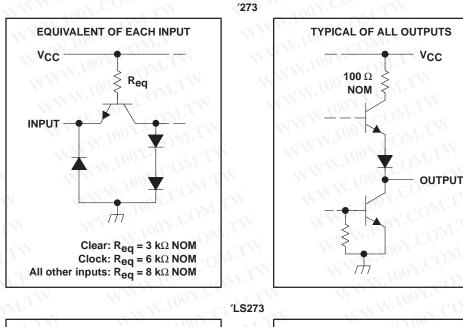
<sup>†</sup> This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12. Pin numbers shown are for the DW, J, N, and W packages.

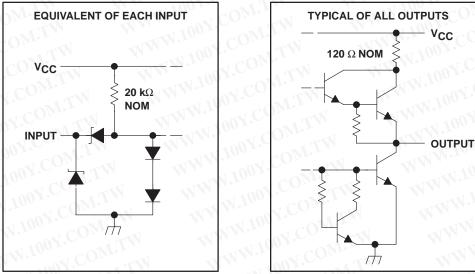
PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters. Copyright © 1988, Texas Instruments Incorporated

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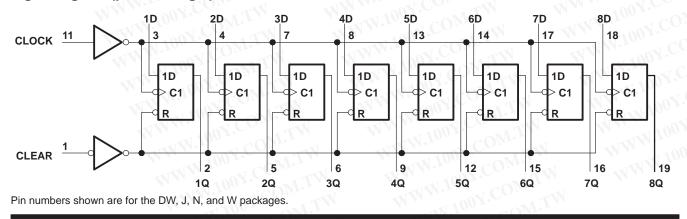
#### schematics of inputs and outputs

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logic diagram (positive logic)





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#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

- 1	Supply voltage, V <sub>CC</sub> (see Note 1)	7 V
CON	Input voltage	
	Operating free-air temperature range, T <sub>A</sub> : SN54273	
1001.00	SN74273	
	Storage temperature range	–65°C to 150°C
NW.IVOY.C	NOTE 1: Voltage values are with respect to network ground terminal.	
WW.100Y	recommended operating conditions	

# recommended operating conditions

			SN54273		<u> </u>	SN74273		UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Supply voltage, V <sub>CC</sub>	V.CON.	4.5	5	5.5	4.75	5	5.25	V
High-level output current, IOH	100 CON.1		N.10	-800	Оуг.,		-800	μΑ
Low-level output current, IOL	VI00Y. M.TW	14.	1.1	16	Mor		16	mA
Clock frequency, fclock	TW.COM TW	0		30	0	NT.	30	MHz
Width of clock or clear pulse, tw	W.ICOW. TW	16.5	MM.		16.5	WT .		ns
100 CONL	Data input	20↑	WW	1.100	20↑	Mr	N	
Setup time, t <sub>SU</sub>	Clear inactive state	25↑		N.100	25↑	M		ns
Data hold time, th	WITTON CONTRACTOR	5↑	MA	11	5↑	11	N	ns
Operating free-air temperature, TA	MM. POT CONT	-55	VIV	125	0		70	°C

↑ The arrow indicates that the rising edge of the clock pulse is used for reference.

#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

NA .	PARAMETER	NTC-	TEST C	ONDITIONS <sup>†</sup>	MIN	TYP‡	MAX	UNIT
VIH	High-level input voltage	War	1001. ON	UM W.	2	JO 7.	Mo	V
VIL	Low-level input voltage	MM	1007.00	W WILL		100X.	0.8	V
VIK	Input clamp voltage	VIII I	V <sub>CC</sub> = MIN,	lj = -12 mA	MM.	Ynn.	-1.5	V
Vон	High-level output voltage	W W	$V_{CC} = MIN,$ $V_{IL} = 0.8 V,$	V <sub>IH</sub> = 2 V, I <sub>OH</sub> = −800 μA	2.4	3.4	V.CO	V
Vol	Low-level output voltage	LM A	V <sub>CC</sub> = MIN, V <sub>IL</sub> = 0.8 V,	V <sub>IH</sub> = 2 V, I <sub>OH</sub> = 16 mA	WW	W.10	0.4	V
II	Input current at maximum input	voltage	V <sub>CC</sub> = MAX,	VI = 5.5 V	N	1.17	1	mA
	Lligh lovel input outreast	Clear	V MAX	V- 24V	N.		80	
IH	High-level input current	Clock or D	$V_{CC} = MAX,$	$V_1 = 2.4 V$	V	MAN.	40	μΑ
		Clear	Man MAN			WW	-3.2	
ΊL	Low-level input current	Clock or D	$V_{CC} = MAX,$	$V_{1} = 0.4 V$			-1.6	mA
los	Short-circuit output current§	WTI	V <sub>CC</sub> = MAX	NT. W. S.	-18	AN.	-57	mA
Icc	Supply current	CONT	V <sub>CC</sub> = MAX,	See Note 2		62	94	mA

<sup>†</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

<sup>‡</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ .

§ Not more than one output should be shorted at a time.

NOTE 2: With all outputs open and 4.5 V applied to all data and clear inputs, ICC is measured after a momentary ground, then 4.5 V, is applied WWW.100Y to clock.

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## switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C

WT	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
fmax	Maximum clock frequency	TW. CONTRACT	30	40		MHz
<sup>t</sup> PHL	Propagation delay time, high-to-low-level output from clear	C <sub>L</sub> = 15 pF, R <sub>I</sub> = 400 Ω,	I	18	27	ns
<sup>t</sup> PLH	Propagation delay time, low-to-high-level output from clock	RL = 400 \$2, See Note 3	- <b>s</b> 1	17	27	ns
<sup>t</sup> PHL	Propagation delay time, high-to-low-level output from clock	100Y. OM.T		18	27	ns
NOTE 3	B: Load circuits and voltage waveforms are shown in Section 1.	NW TO A	~			

YOULTOON	NOTE 3: Load circuits and voltage waveforms are snown in Section 1.
WW.100	absolute maximum ratings over operating free-air temperature range (unless otherwise noted)
WWW.10	Supply voltage, V <sub>CC</sub> (see Note 1)
WWW.J	Operating free-air temperature range, T <sub>A</sub> : SN54LS273 –55°C to 125°C SN74LS273 0°C to 70°C
WWW	Storage temperature range

### recommended operating conditions

		SI	N54LS27	3	SM	74LS27	'3	UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Supply voltage, VCC	WW. LOW. COM.	4.5	5	5.5	4.75	5	5.25	V
High-level output current, IOH	W.Ine COM.	-		-400		COM	-400	μΑ
Low-level output current, IOL	W		14	4	100 .	(0)	8	mA
Clock frequency, f <sub>clock</sub>	WWW INDY.CO.	0		30	0		30	MHz
Width of clock or clear pulse, t <sub>w</sub>	WWW. TONY.COM	20		NN.	20	N.CO	11	ns
Sotup time t	Data input	20↑		VIX	20↑	V.C	OMr.	
Setup time, t <sub>SU</sub>	Clear inactive state	25↑	<		25↑	JU	$\cdot 0_{M}$	ns
Data hold time, th	WW 100Y.CC	5↑			5↑	100x.		ns
Operating free-air temperature, TA	WWW. ON.C.	-55	N	125	0	Ynn	70	°C

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Nr.,	DADAMETED W.P.	TEAT CONDITIONAT	M.	SI	154LS27	/3	SI	N74LS27	73	
A.T.	PARAMETER	TEST CONDITIONS <sup>†</sup>		MIN	TYP <sup>‡</sup>	MAX	MIN	TYP‡	MAX	UNIT
VIH	High-level input voltage	1001. MITH Y	-	2	- CO	M.L	2			V
VIL	Low-level input voltage	WT A STOR	NN.	1100	1.00	0.7			0.8	V
VIK	Input clamp voltage	$V_{CC} = MIN$ , $I_I = -18 \text{ mA}$	WW	N	N.C	-1.5	W		-1.5	V
Vон	High-level output voltage	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = V <sub>IL</sub> max, I <sub>OH</sub> = -400 μA	W	2.5	3.4		2.7	3.4		V
00		$V_{CC} = MIN$ , $V_{IH} = 2 V$ , $I_{OL} = 4$	mA	N	0.25	0.4	NT.	0.25	0.4	V
VOL	Low-level output voltage	$V_{IL} = V_{IL}max$ , $I_{OL} = 8$	mA	WWI	.10	J.CO		0.35	0.5	V
lį	Input current at maximum input voltage	$V_{CC} = MAX,  V_I = 7 V$		WW	N.100	0.1	W.	N	0.1	mA
ΪH.	High-level input current	$V_{CC} = MAX,  V_I = 2.7 V$		VV	M.	20	O.	WT	20	μA
կլ	Low-level input current	$V_{CC} = MAX,  V_I = 0.4 V$			NW.	-0.4	$CO_{NI}$	In	-0.4	mA
los	Short-circuit output current§	V <sub>CC</sub> = MAX	V	-20	WW	-100	-20	1.1	-100	mA
ICC	Supply current	V <sub>CC</sub> = MAX, See Note 2	-		17	27	4 CO	17	27	mA

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

<sup>†</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

<sup>‡</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ .

§ Not more than one output should be shorted at a time and duration of short circuit should not exceed one second.

NOTE 2: With all outputs open and 4.5 V applied to all data and clear inputs, ICC is measured after a momentary ground, then 4.5 V, is applied to clock. N 100Y.COM.

# switching characteristics, $V_{CC} = 5 V$ , $T_A = 25^{\circ}C$

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
fmax	Maximum clock frequency	WW WY	30	40	UNY	MHz
<sup>t</sup> PHL	Propagation delay time, high-to-low-level output from clear	C <sub>L</sub> = 15 pF, R <sub>L</sub> = 2 kΩ,	V.W.V	18	27	ns
t <sub>PLH</sub>	Propagation delay time, low-to-high-level output from clock	RL = 2 KS2, See Note 3		17	27	ns
<sup>t</sup> PHL <	Propagation delay time, high-to-low-level output from clock	W WT	NA	18	27	ns

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