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- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- P-N-P Inputs Reduce D-C Loading
- Hysteresis at Inputs Improves Noise Margins
- Data Flow-thru Pinout (All Inputs on Opposite Side from Outputs)

description

These octal buffers and line drivers are designed to have the performance of the popular SN54LS240/SN74LS240 series and, at the same time, offer a pinout having the inputs and outputs on opposite sides of the package. This arrangement greatly enhances printed circuit board layout.

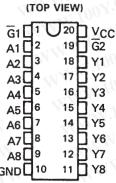
The three-state control gate is a 2-input NOR such that if either $\overline{G1}$ or $\overline{G2}$ are high, all eight outputs are in the high-impedance state.

The 'LS540 offers inverting data and the 'LS541 offers true data at the outputs.

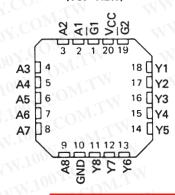
The SN54LS540 and SN54LS541 are characterized for operation over the full military temperature range of -55°C to 125°C. The SN74LS540 and SN74LS541 are characterized for operation from 0°C to 70°C.

TYPE	RATED	RATED	TYPICAL POWER					
	[†] OL	ТОН	DISSIPATION					
	(SINK	SOURCE	(ENABLED)					
	CURRENT)	CURRENT)	'LS540	'LS541				
SN54LS'	12 mA	- 12 mA	92.5 mW	120 mW				
SN74LS'	24 mA	— 15 mA	92.5 mW	120 mW				

SN54LS540, SN54LS541 . . . J OR W PACKAGE SN74LS540, SN74LS541 . . . DW OR N PACKAGE

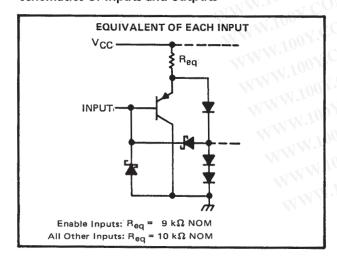


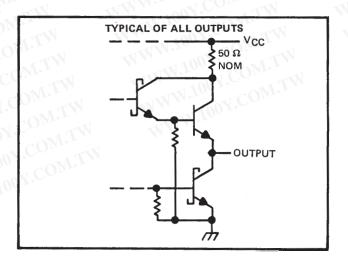
SN54LS540, SN54LS541 . . . FK PACKAGE (TOP VIEW)



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schematics of inputs and outputs





PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

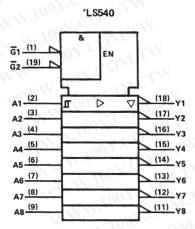


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SN54LS540, SN54LS541, SN74LS540, SN74LS541 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

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logic symbols†

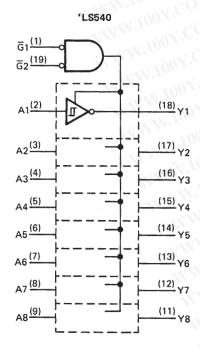


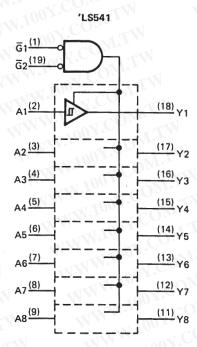
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1 (1)	&	EN	M.10		
M. J. F	`] //	J.W.1		
1 (2)		> <			
2 (3)	N		(17) Y		
3 (4)	-31		(16) Y	3	
4 (5)			(15) Y		
5 (6)			(14) Y		
6 (7)		1	(13) Y	6	
7 (8)	(17		(12) Y		
(9)	× 1	N	(11) Y		
· - c0	Mr.	-XX	-		

1 95/1

logic diagram (positive logic)





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC (see Note 1)		g.CO,	7 V
Input voltage			7 V
Operating free-air temperature range:	SN54LS540, SN54LS541	· · · · · · · · · · · · · · · · · · ·	\dots – 55°C to 125°C
	SN74LS540, SN74LS541	····	0°C to 70°C
Storage temperature range			\dots – 65° C to 150° C

NOTE 1: Voltage values are with respect to the network ground terminal.



[†] These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

recommended operating conditions

N. Indiana M. Indiana M. 100 m. O.M.	1.4	SN54LS	•	TVV.1	SN74LS	OM.	LINUT
PARAMETER	MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Supply voltage, VCC (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
High-level output current, IOH	$V_{T,T}$		-12	- 3731	1700	- 15	mA
Low-level output current, IOL	17	1	12	M. A.	- 100	24	mA
Operating free-air temperature, TA	-55	-431	125	0	11.5	70	°C

NOTE 1: Voltage values are with respect to network ground terminal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	DADAMETE	OM.	TEST SON	TEST CONDITIONS† SN54LS' SN74LS'	1.10	UNIT					
	PARAMETE	R J. Co	1EST CON	DITIONS,	MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	UNII
VIH	High-level input vo	Itage		WWW	2	N P		2	WW	4.0	V
VIL	Low-level input vol	tage	1.1	T.W.Y		COM	0.6		-1	0.6	V
VIK	Input clamp voltag	e .	VCC = MIN,	I _I = -18 mA	001.		- 1.5			- 1.5	00V
	Hysteresis (VT+ -	- V _T _)	VCC = MIN		0.2	0.4	- CV	0.2	0.4	1/1/1	V
Vari	High-level output voltage		V _{CC} = MIN, V _{IL} = V _{IL} max,	$V_{IH} = 2 V$, $I_{OH} = -3 \text{ mA}$	2.4	3.4	M. I	2.4	3.4	NNN	1100
Vон			$V_{CC} = MIN,$ $V_{IL} = 0.5 V,$	V _{IH} = 2V, I _{OH} = MAX	2	ov.C	.oM.	2		WW	W.100
VOL Low-level output v	oltaga 1001	V _{CC} = MIN,	I _{OL} = 12 mA	- TXN .1	0.25	0.4	TW	0.25	0.4	W.19	
	Low-level output voltage		V _{IH} = 2 V, V _{IL} = V _{IL} max	I _{OL} = 24 mA	- TXN	1007		LTV	0.35	0.5	
lozh	•	-state output current, h-level voltage applied		V _O = 2.7 V		N.100	20	M.T	N	20	
lozL	Off-state output current, low-level voltage applied		$V_{IH} = 2 V,$ $V_{IL} = V_{IL} \max$	V _O = 0.4 V	WW	W.10	-20	DM.	TW	- 20	μА
ij	Input current at mi	aximum	V _{CC} = MAX,	V _I = 7 V	W	NW.	0.1	201) 2013	ITW	0.1	mA
ΙΗ	High-level input cu	irrent, any input	VCC = MAX,	V _I = 2.7 V	11		20	U		20	μΑ
IIL	Low-level input cu	rrent	V _{CC} = MAX,	V ₁ = 0.4 V		- 100	-0.2	7 CO	INT.	-0.2	mA
los	Short-circuit outpu	it current§	VCC = MAX	$M_{\perp}T_{\perp}$	-40	1	-225	-40	OMIT	-225	mA
		Outrota kist	TOOY.C	'LS540		13	25	N.C	13	25	
		Outputs high	NW.IO	'LS541		18	32	05/	18	32]
	Cumply aurent	Outputs Issue	VCC = MAX,	'LS540		24	45	00 -	24	45]^
ICC	Supply current	Outputs low	Outputs open	'LS541		30	52	1007	30	52	mA
		All outputs	TWW.100	'LS540	6.1	30	52	3	30	52	
		disabled	M V 100	'LS541		32	55	100	32	55	

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

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 $^{^{\}ddagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C.

[§]Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

SN54LS540, SN54LS541, SN74LS540, SN74LS541 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

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switching characteristics, VCC = 5 V, TA = 25°C

	PARAMETER	PARAMETER TEST CONDITIONS		'LS540			'LS541		
	ALMIN ALL COLOR	TEST CONDITIONS	MIN TYP MA		MAX	MAX MIN		TYP MAX	
tPLH	Propagation delay time, low-to-high-level output	WWW.1007	COM	9	15	WW	9	0015	ns
tPHL	Propagation delay time, high-to-low-level output	$C_L = 45 \text{ pF}, R_L = 667 \text{ see Note 2}$.V.CO	9	15	W	10	18	ns
^t PZL	Output enable time to low level	M. M. 10	0 4.	25	38		25	38	ns
^t PZH	Output enable time to high level	WWW.	N.C	15	25		20	32	ns
tPLZ	Output disable time from low level	$C_L = 5 pF$, $R_L = 667 \Omega$	0 -10	10	18		10	18	ns
^t PHZ	Output disable time from high level	See Note 2	1002.	15	25		18	29	ns

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NOTE 2: Load circuits and voltage waveforms are shown in Section 1. WWW.100Y.COM.TW

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