SONY CXK58257AP/ASP/AM -70L/10L/12L -70LL/10LL/12LL*

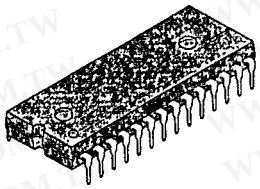
32768-word × 8-bit High Speed CMOS Static RAM

Description

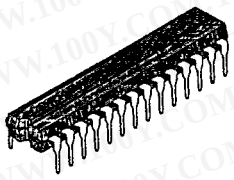
CXK58257AP/ASP/AM is 262,144 bits high speed CMOS static RAM organized as 32,768 words by 8 bits and operates from a single 5V supply. This device is suitable for use in high speed and low power applications in which battery back up for nonvolatility is required.

* 300mil DIP covers only L-version.

CXK58257AP
28 pin DIP (Plastic)



CXK58257ASP
28 pin DIP (Plastic)



CXK58257AM
28 pin SOP (Plastic)

Features

- Fast access time : (Access time)
  CXK58257AP/ASP/AM-70L, 70LL 70ns(Max.)
  CXK58257AP/ASP/AM-10L, 10LL 100ns(Max.)
  CXK58257AP/ASP/AM-12L, 12LL 120ns(Max.)
- Low power operation :
  CXK58257AP/AM-70LL, 10LL, 12LL ;
  Standby : 1 µW (Typ.)
  Operation : 15mW (Typ.)
  CXK58257AP/ASP/AM-70L, 10L, 12L ;
  Standby : 2.5 µW (Typ.)
  Operation : 15mW (Typ.)
- Single +5V supply : +5V ± 10%
- Fully static memory…No clock or timing strobe required
- Equal access and cycle time
- Common data input and output : three state output
- Directly TTL compatible : All inputs and outputs
- Low voltage data retention : 2.0V (Min.)
- Available in 28 pin 600mil DIP, 300mil DIP and 450mil SOP

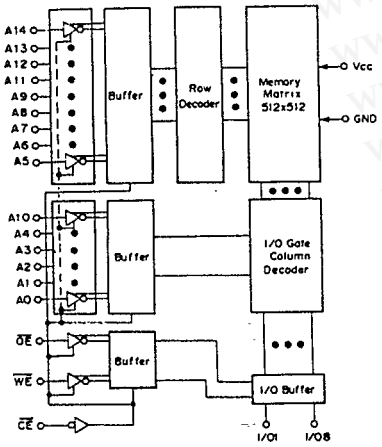
Function

32768-word × 8-bit static RAM

Structure

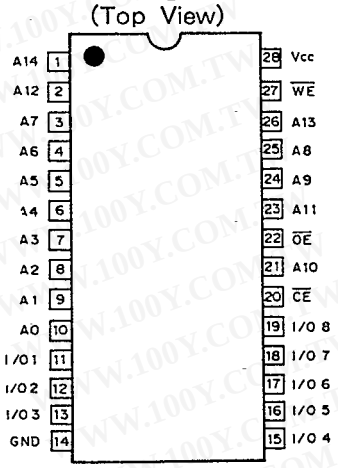
Silicon gate CMOS IC

Block Diagram



Pin Configuration

(Top View)



Pin Description

Symbol	Description
A0 to A14	Address input
I/O1 to I/O8	Data input/output
$\overline{CE}$	Chip enable input
$\overline{WE}$	Write enable input
$\overline{OE}$	Output enable input
Vcc	+5V power supply
GND	Ground

Absolute Maximum Ratings (Ta = 25°C, GND = 0V)

Item	Symbol		Rating	Unit
Supply voltage	V_{CC}		−0.5 to +7.0	V
Input voltage	V_{IN}		−0.5* to V_{CC} +0.5	V
Input and output voltage	$V_{I/O}$		−0.5* to V_{CC} +0.5	V
Allowable power dissipation	P_D	CXK58257AP/ASP	1.0	W
		CXK58257AM	0.7	
Operating temperature	Topr		0 to +70	°C
Storage temperature	Tstg		−55 to +150	°C
Soldering temperature	Tsolder		260 • 10	°C • sec

* VIN, $V_{I/O}$ = −3.0V Min. for pulse width less than 50ns.

Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O1 to I/O8	V_{CC} Current
H	×	×	Not selected	High Z	I_{SB1}, I_{SB2}
L	H	H	Output disable	High Z	I_{CC1}, I_{CC2}
L	L	H	Read	Data out	I_{CC1}, I_{CC2}
L	×	L	Write	Data in	I_{CC1}, I_{CC2}

× : "H" or "L"

DC Recommended Operating Conditions (Ta = 0 to +70°C, GND = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input high voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
Input low voltage	V_{IL}	−0.3*	—	0.8	V

* V_{IL} = −3.0V Min. for pulse width less than 50ns.

Electrical Characteristics

• DC and operating characteristics

(Vcc = 5V ± 10%, GND = 0V, Ta = 0 to +70°C)

Item	Symbol	Test conditions		−70L/10L/12L			−70LL/10LL/12LL			Unit
				Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Input leakage current	I_{LI}	V_{IN} = GND to V_{CC}		−0.5	—	0.5	−0.5	—	0.5	µA
Output leakage current	I_{LO}	$\overline{CE}$ = V_{IH} or $\overline{OE}$ = V_{IH} $V_{I/O}$ = GND to V_{CC}		−0.5	—	0.5	−0.5	—	0.5	µA
Operating power supply current	I_{CC1}	$\overline{CE}$ = V_{IL}, V_{IN} = V_{IH} or V_{IL}, I_{OUT} = 0mA		—	3	10	—	3	10	mA
		$\overline{CE}$ ≦ 0.2V V_{IN} ≦ 0.2V or ≧ V_{CC} − 0.2V		—	1	5	—	1	5	
Average operating current	I_{CC2}	Cycle = Min, Duty = 100%, I_{OUT} = 0mA	70L/70LL	—	30	50	—	30	50	mA
			10L/10LL	—	23	50	—	23	50	
			12L/12LL	—	20	50	—	20	50	
Standby current	I_{SB1}	$\overline{CE}$ ≧ V_{CC} − 0.2V	0 to 70°C	—	—	25	—	—	5	µA
			0 to 40°C	—	—	5	—	—	1	
			25°C	—	0.5	2	—	0.2	0.5	
	I_{SB2}	$\overline{CE}$ = V_{IH}		—	0.4	2	—	0.4	2	mA
Output high voltage	V_{OH}	I_{OH} = −1.0mA		2.4	—	—	2.4	—	—	V
Output low voltage	V_{OL}	I_{OL} = 2.1mA		—	—	0.4	—	—	0.4	V

* V_{CC} = 5V, Ta = 25°C

I/O capacitance

(Ta = 25°C, f = 1MHz)

Item	Symbol	Test conditions	Min.	Max.	Unit
Input capacitance	C_{IN}	V_{IN} = 0V	—	6	pF
I/O capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	—	8	pF

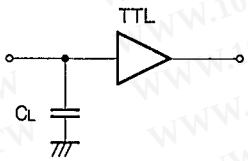
Note) This parameter is sampled and is not 100% tested.

AC characteristics

● AC test conditions

(V_{CC} = 5V ± 10%, Ta = 0 to +70°C)

Item		Conditions
Input pulse high level		V_{IH} = 2.2V
Input pulse low level		V_{IL} = 0.8V
Input rise time		tr = 5ns
Input fall time		tf = 5ns
Input and output reference level		1.5V
Output load conditions	10L/10LL/12L/12LL	C_L* = 100pF, 1TTL
	70L/70LL	C_L* = 30pF, 1TTL



* C_L includes scope and jig capacitances.

• Read cycle

Item	Symbol	−70L/70LL		−10L/10LL		−12L/12LL		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t_{RC}	70	—	100	—	120	—	ns
Address access time	t_{AA}	—	70	—	100	—	120	ns
Chip enable access time	t_{CO}	—	70	—	100	—	120	ns
Output enable to output valid	t_{OE}	—	35	—	50	—	60	ns
Output hold from address change	t_{OH}	20	—	20	—	20	—	ns
Chip enable to output in low Z ($\overline{CE}$)	t_{LZ}	10	—	10	—	10	—	ns
Output enable to output in low Z ($\overline{OE}$)	t_{OLZ}	5	—	5	—	5	—	ns
Chip disable to output in high Z ($\overline{CE}$)	t_{HZ}*	0	30	0	30	0	30	ns
Chip disable to output in high Z ($\overline{OE}$)	t_{OHZ}*	0	30	0	30	0	30	ns

* t_{HZ} and t_{OHZ} are defined as the time required for outputs to turn to high impedance state and are not referred to as output voltage levels.

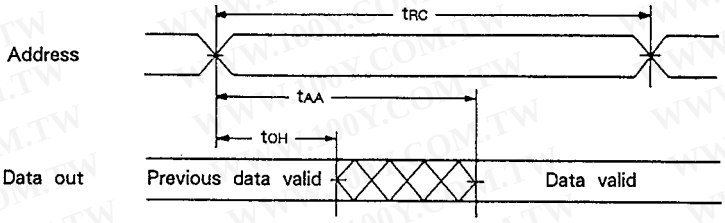
• Write cycle

Item	Symbol	−70L/70LL		−10L/10LL		−12L/12LL		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t_{WC}	70	—	100	—	120	—	ns
Address valid to end of write	t_{AW}	65	—	80	—	100	—	ns
Chip enable to end of write	t_{CW}	65	—	80	—	100	—	ns
Data to write time overlap	t_{DW}	30	—	35	—	40	—	ns
Data hold from write time	t_{DH}	0	—	0	—	0	—	ns
Write pulse width	t_{WP}	50	—	60	—	70	—	ns
Address setup time	t_{AS}	0	—	0	—	0	—	ns
Write recovery time ($\overline{WE}$)	t_{WR}	0	—	0	—	0	—	ns
Write recovery time ($\overline{CE}$)	t_{WR1}	0	—	0	—	0	—	ns
Output active from end of write	t_{OW}	10	—	10	—	10	—	ns
Write to output in high Z	t_{WHZ}*	0	25	0	25	0	25	ns

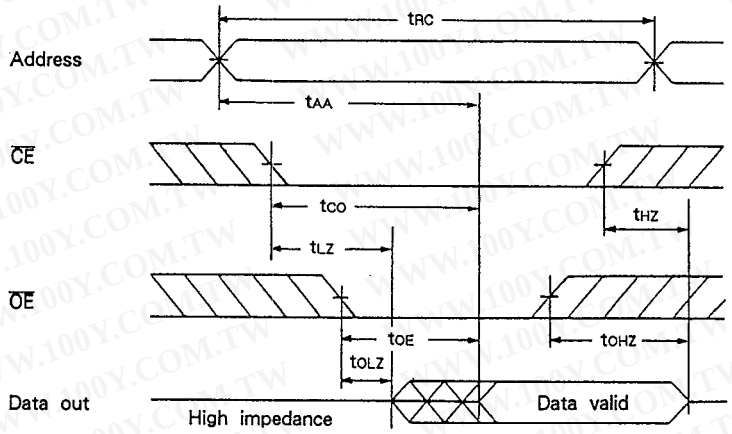
* t_{WHZ} is defined as the time required for outputs to turn to high impedance state and is not referred to as output voltage level.

Timing Waveform

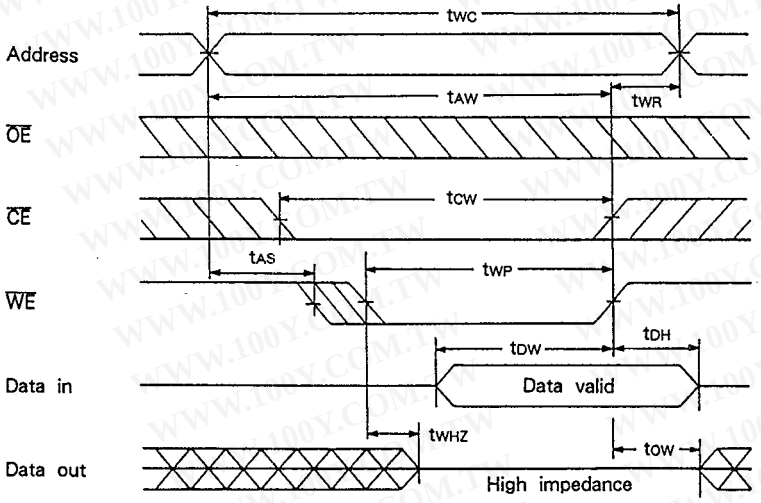
• Read cycle (1) : $\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}



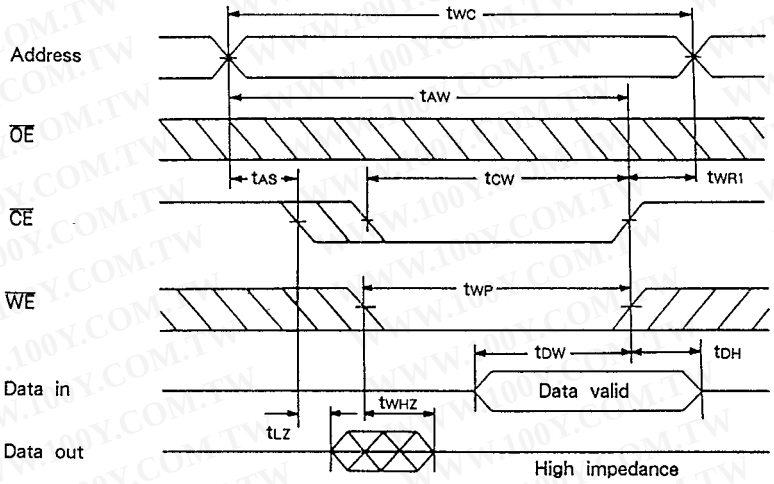
• Read cycle (2) : $\overline{WE}$ = V_{IH}



• Write cycle (1) : $\overline{WE}$ control



• Write cycle (2) : $\overline{CE}$ control



During I/O pins are in the output state, the data input signals of opposite phase to the output must not be applied.

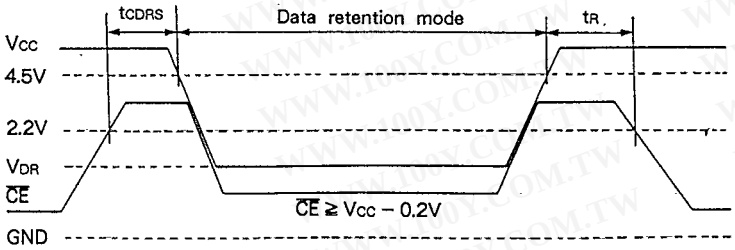
Data Retention Characteristics

(Ta = 0 to 70°C)

Item	Symbol	Test conditions		−70L/10L/12L			−70LL/10LL/12LL			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	
Data retention voltage	V_{DR}	$\overline{CE} \geqq V_{CC} - 0.2V$		2.0	—	5.5	2.0	—	5.5	V
Data retention current	I_{CCDR1}	$V_{CC} = 3.0V$ $\overline{CE} \geqq 2.8V$	Ta = 0 to 70°C	—	—	10	—	—	3	µA
			Ta = 0 to 40°C	—	—	2	—	—	0.6	
			25°C	—	0.25	1	—	0.1	0.3	
	I_{CCDR2}	$V_{CC} = 2.0$ to $5.5V$ $\overline{CE} \geqq V_{CC} - 0.2V$		—	0.5	25	—	0.2	5	µA
Data retention setup time	t_{CDRS}	Chip disable to data retention mode		0	—	—	0	—	—	ns
Recovery time	t_R			t_{RC}*	—	—	t_{RC}*	—	—	ns

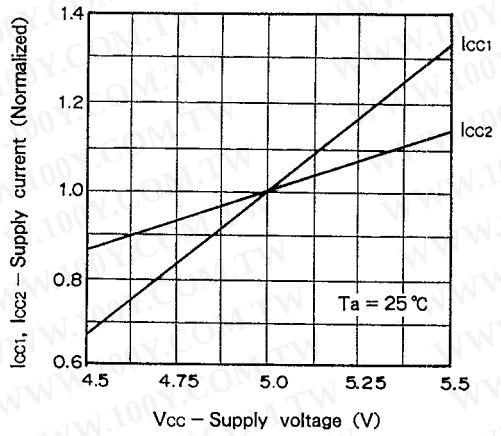
* t_{RC} : Read cycle time

Data retention waveform

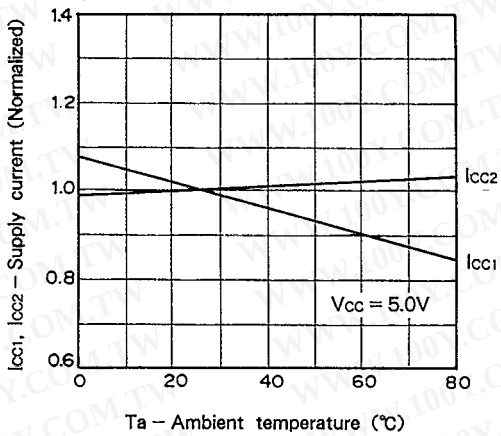


Example of Representative Characteristics

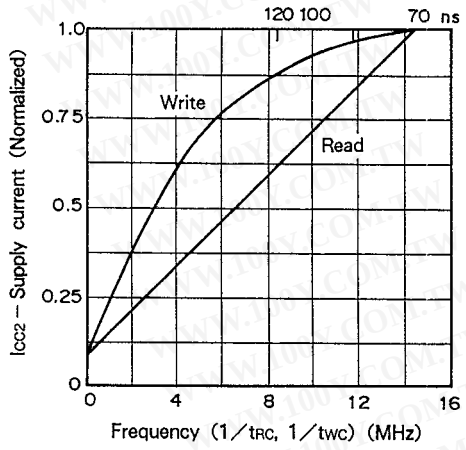
Supply current vs. Supply voltage



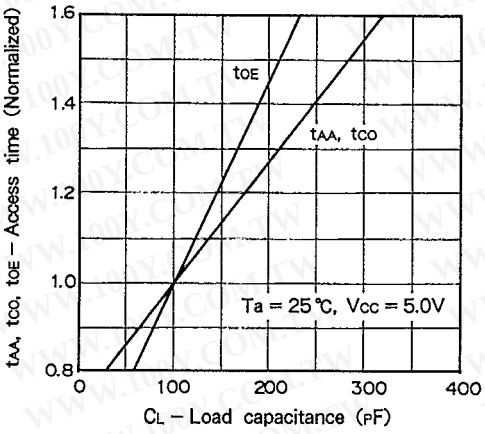
Supply current vs. Ambient temperature



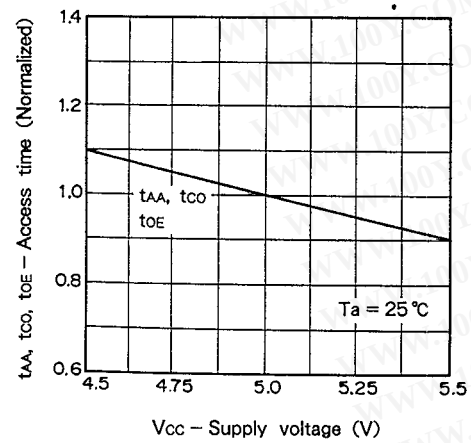
Supply current vs. Frequency



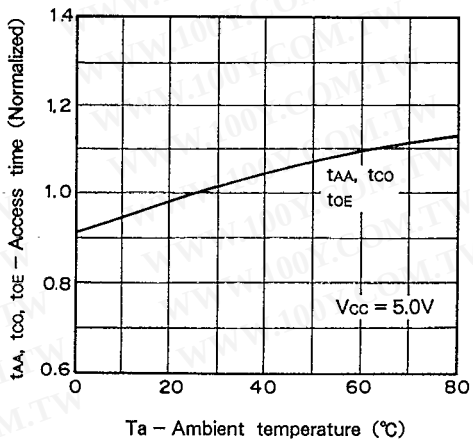
Access time vs. Load capacitance



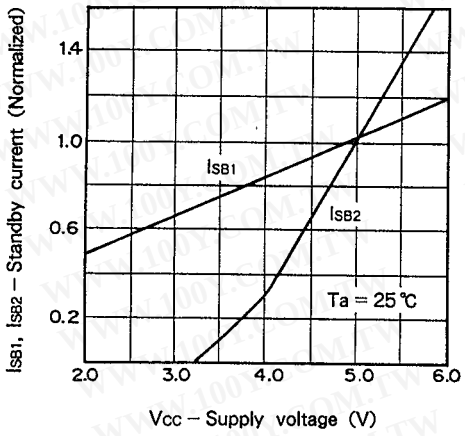
Access time vs. Supply voltage



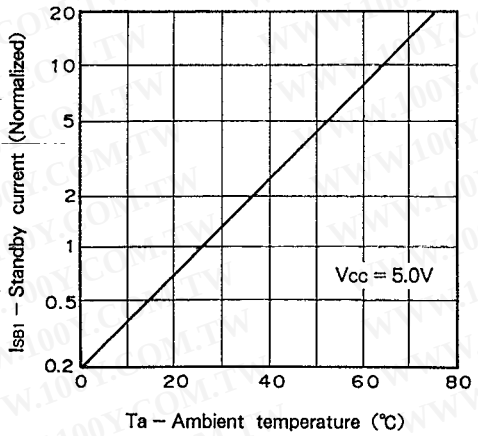
Access time vs. Ambient temperature



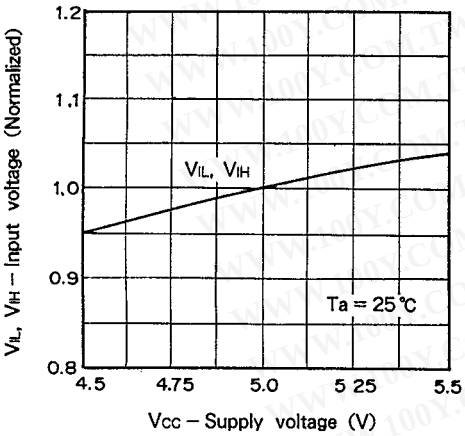
Standby current vs. Supply voltage



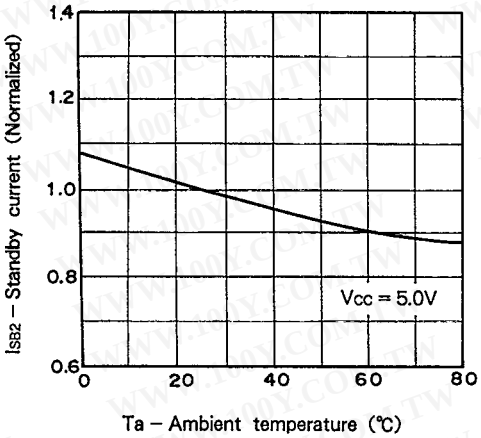
Standby current vs. Ambient temperature



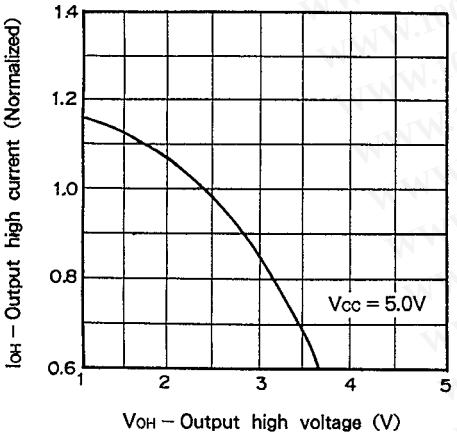
Input voltage level vs. Supply voltage



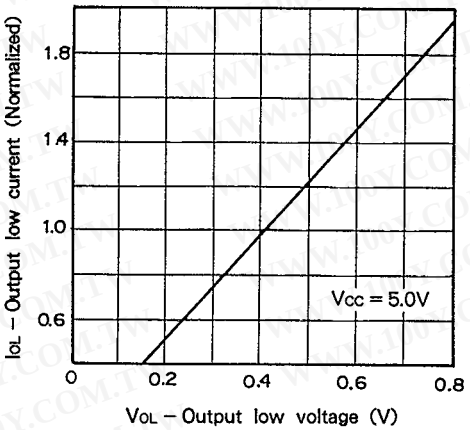
Standby current vs. Ambient temperature



Output high current vs. Output high voltage

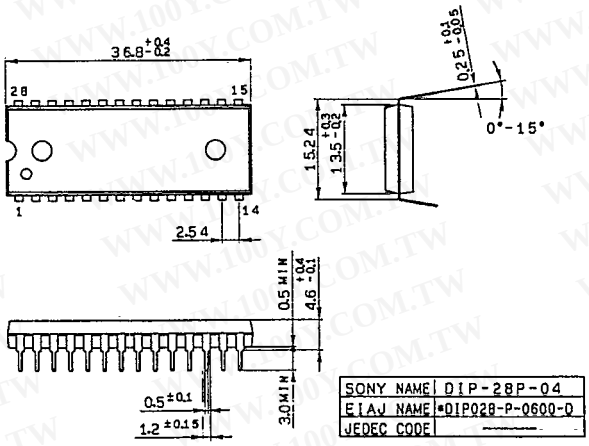


Output low current vs. Output low voltage

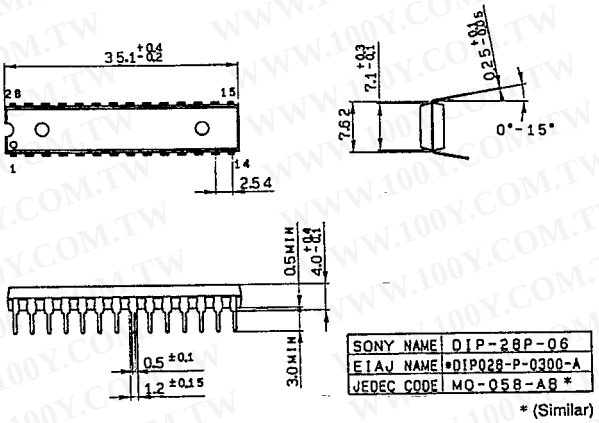


Package Outline Unit : mm

CXK58257AP 28pin DIP (Plastic) 600mil 4.2g



CXK58257ASP 28pin DIP (Plastic) 300mil 2.0g



* (Similar)

CXK58257AM 28pin SOP (Plastic) 450mil 0.7g