SDLS940A - MARCH 1974 - REVISED MARCH 1988

'90A, 'LS90 . . . Decade Counters

'92A, 'LS92 . . . Divide By-Twelve Counters

'93A, 'LS93 . . . 4-Bit Binary Counters

1.1007	TYPICAL
TYPES	POWER DISSIPATION
'90A	145 mW
'92A, '93A	130 mW
'LS90, 'LS92, 'LS93	45 mW

description

Each of these monolithic counters contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-five for the '90A and 'LS90, divide-by-six for the '92A and 'LS92, and the divide-by-eight for the '93A and 'LS93.

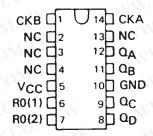
All of these counters have a gated zero reset and the '90A and 'LS90 also have gated set-to-nine inputs for use in BCD nine's complement applications.

To use their maximum count length (decade, divide-by-twelve, or four-bit binary) of these counters, the CKB input is connected to the Ω_A output. The input count pulses are applied to CKA input and the outputs are as described in the appropriate function table. A symmetrical divide-by-ten count can be obtained from the '90A or 'LS90 counters by connecting the Ω_D output to the CKA input and applying the input count to the CKB input which gives a divide-by-ten square wave at output Ω_A .

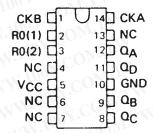
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SN5490A, SN54LS90 . . . J OR W PACKAGE SN7490A . . . N PACKAGE SN74LS90 . . . D OR N PACKAGE (TOP VIEW) CKB 🗆 1 14 CKA RO(1) 2 13 NC RO(2) 43 12 QA 11 QD NC □4 10 GND VCC 5 R9(1) 6 9 QB R9(2) 7 8 QC

SN5492A, SN54LS92 . . . J OR W PACKAGE SN7492A . . . N PACKAGE SN74LS92 . . . D OR N PACKAGE (TOP VIEW)

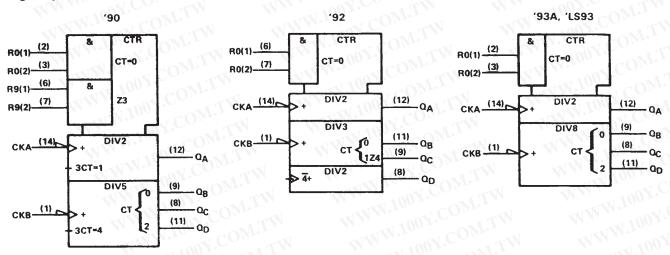


SN5493A, SN54LS93 . . . J OR W PACKAGE SN7493 . . . N PACKAGE SN74LS93 . . . D OR N PACKAGE (TOP VIEW)



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logic symbols†



[†]These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

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SN5490A, SN5492A, SN5493A, SN54LS90, SN54LS92, SN54LS93 SN7490A, SN7492A, SN7493A, SN74LS90, SN74LS92, SN74LS93 DECADE, DIVIDE-BY-TWELVE AND BINARY COUNTERS

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'90A, 'LS90 **BCD COUNT SEQUENCE**

(See Note A)

COUNT	TI	OUT	PUT	
COUNT	ap	QC	QΒ	QA
0	Vr.	L	_d L	L
10	41	L	L	Н
2.0	L	L	H	L
3	L	N.F.	Н	Н
4	L	H	L	L
50	·L	Н	L	Н
6	VLC	Н	H	ζÚ
700	Ļ	H	Н	Н
8	Н	L	L	L
9	H	·Ł	L	н

'92A, 'LS92 **COUNT SEQUENCE**

(See Note C)

4111	-14	OUT	PUT	-11
COUNT	(19)	UUI		
11.11	Q_D	QC	QB	QA
0	L	L	L.	L
1	L	L	L	H
2	L	L	Н	L
3	L	L	Н	H
4	L	H	L	L
5	L	Н	(.L ⁰⁾	H
6	H	L	L	OF
7	H	E	L	Н
8	н	L	H	F
9	н	L	Н	H
10	н	H	L	L
11	н	H	L	Н

'92A, 'LS92, '93A, 'LS93 RESET/COUNT FUNCTION TABLE

RESET	RESET INPUTS		OUT	PUT	-xxI 1
R ₀₍₁₎	R ₀₍₂₎	α _D	ac	QB	QA
Н	Н	L	L	L	L
L	X		CO	JNT	
X	L		CO	TNL	

- NOTES: A. Output Q_A is connected to input CKB for BCD count.

 B. Output Q_D is connected to input CKB. count.
 - C. Output Q_A is connected to input CKB.
 - D. H = high level, L = low level, X = irrelevant

'90A, 'LS90 BI-QUINARY (5-2) (See Note B)

201 117	-41	OUT	PUT	-
COUNT	QA	QD	ac	QB
0	L	L	L	JE
1	L	ď.	L	Н
2	T.	L	Н	OL.
3	₹ L T	L	Н	Н
4	L	Н	L	L
5	H	L	L	L
N 6	н∍	L	L	Н
7	н	L	H	L
8	н	L	Н	H
9	н	H	L	L

'90A, 'LS90 RESET/COUNT FUNCTION TABLE

N.You	RESET	INPUTS	\$	V	OUT	PUT	
R ₀₍₁₎	R ₀₍₂₎	R ₉₍₁₎	R9(2)	σ_{D}	QC	QB	QA
(H)	Н	A L	X	L	L	L	N.L.
H	Н	X	W L	L	L	L	L
×	X	Н	н	н	L	L	Н
(X)	L	X	L		СО	UNT	
L	X	L	X		СО	UNT	
L.	X	Cx	LV		СО	UNT	
X	700	. do	X	κŤ	СО	UNT	

'93A, 'LS93 **COUNT SEQUENCE**

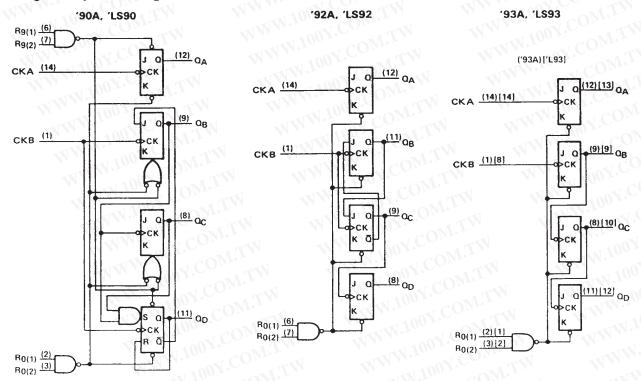
(See Note C)

COUNT		OUT	PUT	
COONT	QD	ac	QB	QA
0	W.	L.	Ļ	L
N.10	Ĺ	L	L	Н
2	06	L	Н	L
3	L	Y L	Н	Н
4	L	Н		L
5	LLO	H	L	H
6	L	H	Н	L
7	L	н	H	H
8	H	L	L	L
9	Н	L	L	Н
10	н	L	Н	L
11	н	Ł	Н	Н
12	Н	н	L	L
13	н	н	L	Н
14	н	Н	Н	L
15	н	н	н	Н



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logic diagrams (positive logic)



The J and K inputs shown without connection are for reference only and are functionally at a high level. Pin numbers shown in () are for the 'LS93 and '93A and pin numbers shown in () are for the 54L93.

schematics of inputs and outputs

'90A, '92A, '93A TYPICAL OF ALL OUTPUTS **EQUIVALENT OF EACH INPUT** V_{CC} Vсс 100 Ω NOM INPUT INPUT Req NOM 2.5 kΩ CKA $1.25\;k\Omega$ CKB ('90A, '92A) 2.5 kΩ CKB ('93A) 6 kΩ All resets

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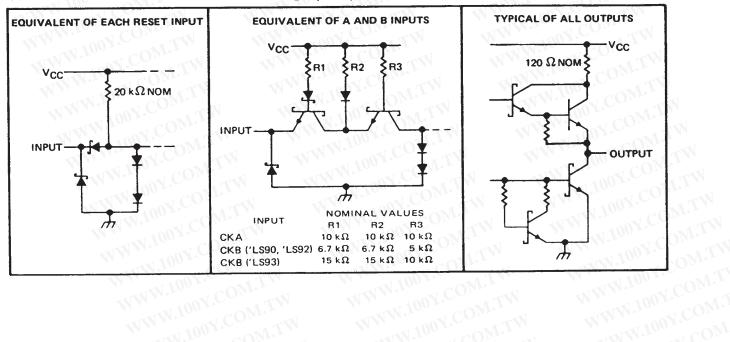
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schematics of inputs and outputs (continued)

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'LS90, 'LS92, 'LS93



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC (see Note 1)	1007	J	 7V
Input voltage		TW	 5.5 V
Interemitter voltage (see Note 2)			5.5 V
Operating free-air temperature range:	SN5490A, SN5492A, SN5493A	M	 -55°C to 125°C
ALM M. A. COM	SN7490A, SN7492A, SN7493A	·	 . 0°C to 70°C
Storage temperature range			-65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.

2. This is the voltage between two emitters of a multiple-emitter transistor. For these circuits, this rating applies between the two R₀ inputs, and for the '90A circuit, it also applies between the two Rg inputs.

recommended operating conditions

MANNION CONTIN	M.M.100		0A, SN SN5493		SN749	0A, SN N7493		UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	UV
Supply voltage, VCC	W 1 21 10	4.5	5	5.5	4.75	5	5.25	V
High-level output current, IOH		NY.	COL	-800			-800	μА
Low-level output current, IOI	.W.V.	-7	COD	16	κŢ		16	mA
WY 2,007 2(IV)	A input	0		32	0		32	MHz
Count frequency, f _{count} (see Figure 1)	8 input	0	V.CO	16	0		16	1411.12
TIN TOW CONT.	A input	15	- 0	OM.	15		1	W.
Pulse width, tw	B input	30	07.	100	30			ns
TAMAN'TO COMP.	Reset inputs	15	ov.	JO _P	15		11	
Reset inactive-state setup time, t _{SII}		25	00	COL	25	«1		ns
Operating free-air temperature, T _A		-55	100X	125	0	N	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

			11/11			'90A		M.	'92A	M.C.	_ 10 7	'93A		UNIT
	PARAMETE	ER [¶]	TEST CONDITI	ONST	MIN	TYP	MAX	MIN	TYP#	MAX	MIN	TYP [‡]	MAX	OIVII
th H	ligh-level inpu	ıt voltage	100	13.	2			2	11. IV	10 7.	_ 2			V
	ow-level inpu		WW V	W.C.	- K 1	TW	0.8	WV	V 1	0.8		TT	0.8	V
10-	nput clamp vo		VCC = MIN, 11 = -	12 mA	Ohr.	-XXI	-1.5	-11	W.	-1.5	CO	Nr.	-1.5	V
	ligh-level out	out voltage	V _{CC} = MIN, V _{IH} = V _{IL} = 0.8 V, I _{OH} =	2 V,	2.4	3.4	Ī	2.4	3.4	100	2.4	3.4		٧
OL L	ow-level outp	out voltage	V _{CC} = MIN, V _{IH} = V _{IL} = 0.8 V, I _{OL} =	2 V,	CO	0.2	0.4		0.2	0.4	OY.C	0.2	0.4	V
	nput current		V _{CC} = MAX, V ₁ = 5	.5 V	YO		1		WV	1	001	<u>.co</u> 1	M.T.V	mA
		Any reset		- 110	DAG		40			40	1003		40	N
H .	ligh-level	CKA	V _{CC} = MAX, V ₁ = 2	.4 V	N.	$C_{O_{2}}$	80		V	80	100	1.C	80	μА
' i	nput current	СКВ			00	- CO	120	cT.		120	1.70.	7.0	80	
		Any reset		N W	100		-1.6	N		-1.6	×11(0x.	-1.6	1.7.
	_ow-level	CKA	VCC = MAX, VI = 0	.4 V	0.0	V.CL	-3.2	W		-3.2	1	ooV.	-3.2	- ' \ \
i	nput current	СКВ	1		To	-7 (-4.8	1		-4.8	WW.	Ing	-3.2	110
	Short-circuit			SN54'	-20	101.	-57	-20		-57	-20	100.	-57	mA
20	output curren	t §	VCC = MAX	SN74'	-18	. NO.	-57	-18		-57	-18		-57	
	Supply curren		VCC = MAX, See N	ote 3	aN.	29	42	1.	26	39		26	39	mA

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTE 3: I_{CC} is measured with all outputs open, both R₀ inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.



 $[\]ddagger$ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

Not more than one output should be shorted at a time.

QA outputs are tested at IOL = 16 mA plus the limit value for IIL for the CKB input. This permits driving the CKB input while maintaining

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switching characteristics, VCC = 5 V, TA = 25°C

~ 100 x.	FROM	то	TEST COMPLETIONS	M.	'90A			'92A	$\times 1.10^{\circ}$	J »	'93A	7.7.	UNI
PARAMETER	(INPUT)	(OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	3.4
W.100	CKA	QA	TANN TO	32	42	ĸI.	32	42	M.r.	32	42	Mr.	мн:
f _{max}	СКВ	QB	M. 100 1.	16		IN .	16	44	74X	16		$\Delta M_{\rm c}$	
tPLH .	CKA	TW o.	MANA		10	16		10	16	400	10	16	ns
tPHL 1	COM	QA	MW.To	CO	12	18		12	18		12	18	
†PLH	СКА	α _D	W 1 100		32	48		32	48	$\sqrt{10}$	46	70	ns
t _{PHL}	CAAO	αБ	WWW	V.C	34	50		34	50		46	70	100
tPLH	скв	Mr.	CL = 15 pF,	-7 (10	16	i T	10	16	11/15	10	16	ns
tPHL.		α _B	R _L = 400 Ω,	03.	14	21		14	21	-31	14	21	ΔM
tPLH .	СКВ	QC	See Figure 1	OOV	21	32	W	10	16	M. J.	21	32	ns
^t PHL	CKB	OMGE	WW.	00	23	35		14	21	50IN	23	35	40)
tPLH	СКВ	TOTAL	WW	100	21	32	17.11	21	32		34	51	ns
tPHL .	The state of the s	COJOD	MMM		23	35		23	35	MW	34	51	
tPHL	Set-to-0	Any		1.70	26	40		26	40		26	40	ns
tPLH	Santa 0	Q _A , Q _D	N Min	411	20	30	AT	AA.		100	1 1	<u> 1104</u>	ns
tPHL -	Set-to-9	QB, QC	W. W.	177.	26	40						V .	N.

[†]f_{max} = maximum count frequency

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tpLH = propagation delay time, low-to-high-level output

tpHL = propagation delay time, high-to-low-level output

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	144			. 0		0	1	-	CALE	cor				-	241.6	00	012	
mmended operating conditions	×XI	W	37	UV			O	M	. 1	J					M	Too	J	CO
1: Voltage values are with respect to network ground termina	ı.																	
Storage temperature range			01	1	. C	Y	•		1	•		V	N.		-6	5°C 1	o 1	50°C
SN74LS' Circui																		
Operating free-air temperature range: SN54LS' Circui																		
A and B inputs																		
Input voltage: R inputs																		
Supply voltage, VCC (see Note 1)																		

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

WWW.100X.COM.TW	MMM.100X	COA	SN54LS90 SN54LS92 SN54LS93			SN74LS90 SN74LS92 SN74LS93		
MM, took of the	100	MIN	NOM	MAX	MIN	NOM	MAX	00x.
Supply voltage, V _{CC}	MMM	4.5	5	5.5	4.75	5	5.25	V
High-level output current, IOH	111/10		OM.	-400		-7	-400	μА
Low-level output current, IOL		101.		4			8	mA
Construction of the Constr	A input	0	CO_{2}	32	0		32	1411-0
Count frequency, f _{count} (see Figure 1)	B input	0	_c01	16	0		16	MHz
WWW ONLOW IN	A input	15		TIL	15		11/11	-311
Pulse width, tw	B input			DIA.	30		431	ns
	Reset inputs	30	0 -	OM.	30			TW
Reset inactive-state setup time, t _{su}	M MN	25	W.	,	25			ns
Operating free-air temperature, TA	-1	-55		125	0	KÍ	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS [†]			SN54LS90 SN54LS92			SN74LS90 SN74LS92			UNIT										
			COM.				TYP‡	MAX	MIN	TYP‡	MAX										
VIH	High-level inpu	t voltage	VI - VI 10	OM.	11.	2	JVV.	00	2	1. 1		V									
VIL	Low-level inpu	t voltage		on V.Co	TITE .			0.7		TI	0.8	V									
VIK	Input clamp vo	ltage	VCC = MIN,	I _I = -18 mA		-31	WW	-1.5	7 CU	N.	-1.5	V									
VOH High-level output voltage		V _{CC} = MIN, V _{IL} = V _{IL} max,	V _{IH} = 2 V,	ıA A	2.5	3.4	1.100	2.7	3.4	TW	٧										
VOL Low-level output voltage			VCC = MIN,	V _{IH} = 2 V,	IOL = 4 mA¶		0.25	0.4	×1 (0.25	0.4										
		ut voltage	VIL = VIL max,		10L = 8 mA¶		N. T.	-xx11	On r.	0.35	0.5	V									
	Input current	Any reset	VCC = MAX,	V ₁ = 7 V				0.1			0.1	N									
11	at maximum	CKA	V _{CC} = MAX, V _I = 5.5 V		COM			0.2	10	st C.O	0,2	mA									
	input voltage	CKB					1/1	0.4	100	3.0	0.4										
	High lavel	Any reset	TIMM: OF COR		V.CO			20	. 0		20										
Ιн	High-level	CKA	VCC = MAX,	V1 = 2.7 V	V1 = 2.7 V	$V_1 = 2.7 \text{ V}$	V1 = 2.7 V	V1 = 2.7 V	$V_1 = 2.7 V$	V1 = 2.7 V	$V_1 = 2.7 V$	V1 = 2.7 V	$V_1 = 2.7 \text{ V}$		-1		40	11.10	-7	40	μА
	input current	СКВ				1/1		80	-311	00 1.	80	TI									
	1 1 1	Any reset			of Con	MX		-0.4	144.	V	-0.4	-1									
11L	Low-level	CKA	V _{CC} = MAX, V _I = 0.4 V			F 4		-2.4	TIN	Ino_	-2.4	mA									
input current		СКВ		MAN AL. OUN.CO.				-3.2	44	- 100	-3.2										
los	Short-circuit or	utput current§	VCC = MAX	TWW.	To COM	-20	(I	-100	-20	1.10	-100	mA									
	C			'LS90	9 15 9 15			1	9	15	0										
ICC Supply current			V _{CC} = MAX, See Note 3					'LS92		9 15		mA									

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTE 3: ICC is measured with all outputs open, both RO inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.



 $[\]ddagger$ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

[§]Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

 $[\]P$ QA outputs are tested at specified IOL plus the limit value of IIL for the CKB input. This permits driving the CKB input while maintaining full fan-out capability.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			S	N54LS9	3	S	UNIT			
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	UNI	
VIH	High-level inpu	t voltage	-1	MIN.To	CON	2			2	AT C	DAr.	V
VIL	Low-level inpu		W W	100	TIME			0.7	x1 10	n r.	0.8	V
VIK	Input clamp vo	oltage	VCC = MIN,	1 ₁ = -18 mA	V.Co.	N		-1.5	1,10	OOX.	-1.5	V
Vон	High-level outp	out voltage	V _{CC} = MIN, V _{IL} = V _{IL} max,	V _{IH} = 2 V, 1 _{OH} = -400 μ.	AOY.CONI.	2.5	3.4	WV	2.7	3,4	COD	٧
		VI CON	VCC = MIN,	V _{IH} = 2 V,	IOL = 4 mA¶	TW	0.25	0.4	W.A.	0.25	0.4	V
VOL Low-level o	Low-level outp	out voltage	VIL = VIL max	W.	IOL = 8 mA¶		d .		a(1)	0.35	0.5	7.
	Input current	Any reset	V _{CC} = MAX,	V1 = 7 V	1007.	T.T.		0.1	-755	W.101	0.1	mA
Ч	at maximum input voltage	CKA or CKB	VCC = MAX,	V ₁ = 5.5 V	N.100 X.	T.M	N	0.2	M. A.	JN.1	0.2	0
	High-level	Any reset		V _{CC} = MAX, V _I = 2.7 V		TIM		20	11/1	1	20	J.,
чн	input current	CKA or CKB	VCC = MAX,			One	TW	40		11/1/4	80	μА
		Any reset	TOM.		100.100			-0.4			-0.4	-7
IIL.	Low-level	$V_{CC} = MAX$, $V_{I} = 0.4$	V ₁ = 0.4 V	4 V		TI	-2.4			-2.4	mA	
inpu	input current	СКВ	COM	N	INW.		N. P.	-1.6			-1.6	W
los	Short-circuit o	utput current §	VCC = MAX		TXV.100	-20	$M_{i,j}$	-100	-20		-100	mA
Icc	Supply current		VCC = MAX,	See Note 3	1100	N.C.	9	15		9	15	mA

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions

switching characteristics, VCC = 5 V, TA = 25°C

	FROM	ТО	- 1177		'LS90	-1	100,	'LS92	· Mr	r.A.	'LS93	- 1	UNI					
PARAMETER#	(INPUT)	(OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	Oldi					
	CKA	QA	COMP	32	42		32	42	OM	32	42		MHz					
f _{max}	CKB	QB	OY. COMITW	16			16	0 7.		16			191112					
†PLH	011		OV.COM		10	16	MA.	10	16		10	16	ns					
tPHL	CKA	QA	on COM'I		12	18	W.	12	18	Mr.	12	18	113					
tPLH .	CKA	WW	1007.C		32	48	4.1	32	48		46	70	ns					
^t PHL	CKA	UD	UD	αD	A COM	XX	34	50		34	50	Or	46	70				
tPLH .		0	CL = 15 pF,	1	10	16	- 1	10	16	ON	10	16	ns					
tPHL	CKB	QB	R _L = 2 kΩ	TW	14	21		14	21		14	21	,,,,					
¹PLH		a XIXI	O _C See Figure 1		21	32	ovV	10	16	CO	21	32	ns					
tPHL .	CKB	a _C		W.100 1. CON	I. F.	23	35		14	21		23	35	113				
tPLH			- N					M. OOX.CO.		21	32	11	21	32	N.C.	34	51	ns
†PHL	CKB	σD	MN.100	MM. TO	MM. TO	MM. To CO	NY.	23 35 23 35	V (34	51	1 "						
tPHL	Set-to-0	Any	1001.	M.	26	40		26	40	0 -	26	40	ns					
tPLH .		QA, QD	MAN ALL TOTAL CA	J - 1	20	30	1	MAN	1	001			ns					
tPHL	Set-to-9 QB, QC		WW.In	OM	26	40		- XTV	1111				113					

[#]fmax = maximum count frequency

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[‡]All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

S Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

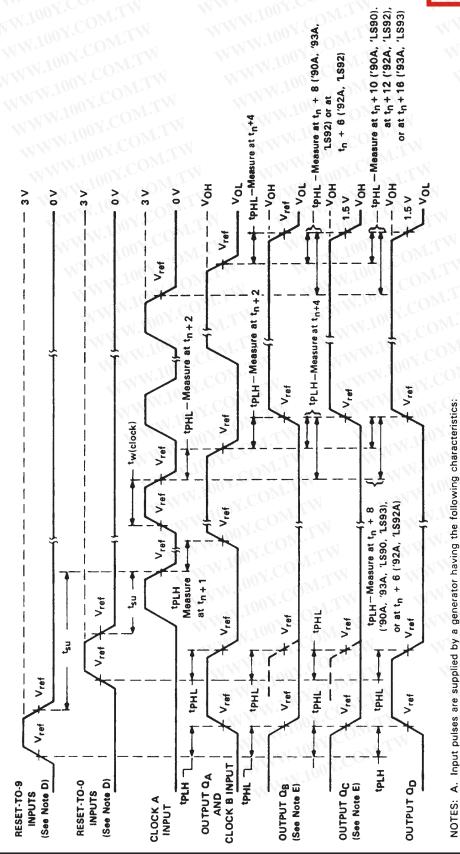
[¶] Q_A outputs are tested at specified I_{OL} plus the limit value for I_{IL} for the CKB input. This permits driving the CKB input while maintaining full famous capability

NOTE 3: ICC is measured with all outputs open, both R₀ inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.

tpLH = propagation delay time, low-to-high-level output

tpHL = propagation delay time, high-to-low-level output

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for '90A, '92A, '93A, $t_1 \le 5$ ns, $t_1 \le 5$ ns, PRR = 1 MHz, duty cycle = 50%, $Z_{out} \approx 50$ ohms;

for 'LS90, 'LS92, 'LS93, $t_f \le 15$ ns, $t_f \le 5$ ns, PRR = 1 MHz, duty cycle = 50%, $Z_{out} \approx 50$ ohms.

- includes probe and jig capacitance. CL includes probe and jig capacitance All diodes are 1N3064 or equivalent.
- Each reset input is tested separately with the other reset at 4.5 V. BB CJ CJ UJ UL
 - Reference waveforms are shown with dashed lines.
- For '90A, '92A, and '93A; $V_{ref} = 1.5 \text{ V}$. For 'LS90, 'LS92, and 'LS93; $V_{ref} = 1.3 \text{ V}$.

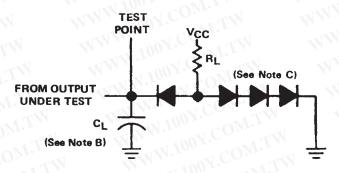
FIGURE 1A



PARAMETER MEASUREMENT INFORMATION

SDLS940A - MARCH 1974 - REVISED MARCH 1988

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

- NOTES: A. Input pulses are supplied by a generator having the following characteristics: for '90A, '92A, '93A, $t_r \le 5$ ns, $t_f \le 5$ ns, PRR = 1 MHz, duty cycle = 50%, $t_{out} \approx 50$ ohms; for 'LS90, 'LS92, 'LS93, $t_r \le 15$ ns, $t_f \le 5$ ns, PRR = 1 MHz, duty cycle = 50%, $t_{out} \approx 50$ ohms.
 - B. C_L includes probe and jig capacitance.
 - C. All diodes are 1N3064 or equivalent.
 - D. Each reset input is tested separately with the other reset at 4.5 V.
 - E. Reference waveforms are shown with dashed lines.
 - F. For '90A, '92A, and '93A; $V_{ref} = 1.5 \text{ V}$. For 'LS90, 'LS92, and 'LS93; $V_{ref} = 1.3 \text{ V}$.

FIGURE 1B

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PACKAGE OPTION ADDENDUM

28-Feb-2005

PACKAGING INFORMATION

Orderable Device	Status (1)	Package	Package	Pins	Package	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
WWW.	TW	Туре	Drawing	OY.C	Qty	V	1/1/1/100	Y. TW
7603201CA	ACTIVE	CDIP	J	14	01	None	Call TI	Level-NC-NC-NC
7603201DA	ACTIVE	CFP	W	14	(1)	None	Call TI	Level-NC-NC-NC
7700101CA	ACTIVE	CDIP	W J	14	1	None	Call TI	Level-NC-NC-NC
7700101DA	ACTIVE	CFP	W	14	1.1	None	Call TI	Level-NC-NC-NC
M38510/31501BCA	ACTIVE	CDIP	J	14	100	None	Call TI	Level-NC-NC-NC
M38510/31501BDA	ACTIVE	CFP	W	14	1	None	Call TI	Level-NC-NC-NC
M38510/31502BCA	ACTIVE	CDIP	J	14	1	None	Call TI	Level-NC-NC-NC
M38510/31502BDA	ACTIVE	CFP	W	14	1V.C	None	Call TI	Level-NC-NC-NC
SN5490AJ	LIFEBUY	CDIP	J	14	1	None	Call TI	Level-NC-NC-NC
SN5492AJ	OBSOLETE	CDIP	J	14	1.100 1.	None	Call TI	Call TI
SN54LS90J	ACTIVE	CDIP	J	14	100	None	Call TI	Level-NC-NC-NC
SN54LS93J	ACTIVE	CDIP	N J	14	1	None	Call TI	Level-NC-NC-NC
SN7490AN	OBSOLETE	PDIP	N	14	^{0}M ^{1}n	None	Call TI	Call TI
SN7492AN	OBSOLETE	PDIP	N	14	-xx 1	None	Call TI	Call TI
SN7493AN	OBSOLETE	PDIP	T N	14	MAN	None	Call TI	Call TI
SN74LS90D	ACTIVE	SOIC	D	14	50	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR Level-1-235C-UNLIM
SN74LS90DR	ACTIVE	SOIC	D	14	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR Level-1-235C-UNLIM
SN74LS90N	ACTIVE	PDIP	N N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74LS92D	ACTIVE	SOIC	OND	14	50	Pb-Free (RoHS)		Level-2-260C-1 YEAR Level-1-235C-UNLIM
SN74LS92DR	ACTIVE	SOIC	COD	14	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR Level-1-235C-UNLIM
SN74LS92N	ACTIVE	PDIP	I.VN	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74LS92N3	OBSOLETE	PDIP	N	14		None	Call TI	Call TI
SN74LS92NSR	ACTIVE	SO	NS	14	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR Level-1-235C-UNLIM
SN74LS93D	ACTIVE	SOIC	100 P.	14	50	Pb-Free (RoHS)		Level-2-260C-1 YEAR Level-1-235C-UNLIM
SN74LS93DR	ACTIVE	SOIC	.10 D	14	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR Level-1-235C-UNLIM
SN74LS93N	ACTIVE	PDIP	NOV	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74LS93N3	OBSOLETE	PDIP	N ₁	14	VIII	None	Call TI	Call TI
SN74LS93NSR	ACTIVE	so	NS	14	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR Level-1-235C-UNLIM
SNJ5490AJ	LIFEBUY	CDIP <	1117	14	1,1	None	Call TI	Level-NC-NC-NC
SNJ5490AW	LIFEBUY	CFP	W	14	CCI	None	Call TI	Level-NC-NC-NC
SNJ5492AJ	OBSOLETE	CDIP	J.V.	14	MOD	None	Call TI	Call TI
SNJ5492AW	OBSOLETE	CFP	W	14		None	Call TI	Call TI
SNJ54LS90J	ACTIVE	CDIP	Ú	14	1	None	Call TI	Level-NC-NC-NC
SNJ54LS90W	ACTIVE	CFP	W	14	1	None	Call TI	Level-NC-NC-NC



PACKAGE OPTION ADDENDUM

28-Feb-2005

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins I	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp (3)
SNJ54LS93J	ACTIVE	CDIP	J.100	14	1	None	Call TI	Level-NC-NC-NC
SNJ54LS93W	ACTIVE	CFP	W	14	11.7	None	Call TI	Level-NC-NC-NC

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in

a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - May not be currently available - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

None: Not yet available Lead (Pb-Free).

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDECindustry standard classifications, and peak solder temperature.

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