

勝 特 力 材 料 886-3-5753170 胜特力电子(上海) 86-21-54151736 胜特力电子(深圳) 86-755-83298787

Http://www.100y.com.tw

CMOS Dual Precision Monostable Multivibrator

High-Voltage Types (20-Volt Rating)

Features:

- Retriggerable/resettable capability
- Trigger and reset propagation delays independent of R_x, C_x
- Triggering from leading or trailing edge
- Q and Q buffered outputs available
- Separate resets
- Replaces CD4538B Type

CX1 RX1

VDD

TR 4

TR 5

MONO1 7 G1

TRESET 3

MONO2 9 G2

VDO*16

VSS*8

CX2 RXCX(1)

VDD

S2CS*24255RI

FUNCTIONAL DIAGRAM

■ CD14538B dual precision monostable multivibrator provides stable retriggerable/resettable one-shot operation for any fixed-voltage timing application.

An external resistor (R_x) and an external capacitor (C_x) control the timing and accuracy for the circuit. Adjustment of R_x and C_x provides a wide range of output pulse widths from the Q and \overline{Q} terminals. The time delay from trigger input to output transition (trigger propagation delay) and the time delay from reset input to output transition (reset propagation delay) are independent of R_x and C_x . Precision control of output pulse widths is achieved through linear CMOS techniques.

Leading-edge-triggering (+TR) and trailing-edge-triggering (-TR) inputs are provided for triggering from either edge of an input pulse. An unused +TR input should be tied to V_{SS} . An unused -TR input should be tied to V_{DD} . A RESET (on low level) is provided for immediate termination of the output pulse or to prevent output pulses when power is turned on. An unused RESET input should be tied to V_{DD} . However, if an entire section of the CD14538B is not used, its inputs must be tied to either V_{DD} or V_{SS} . See Table I.

In normal operation the circuit retriggers (extends the output pulse one period) on the application of each new trigger pulse. For operation in the non-retriggerable mode, \overline{Q} is connected to -TR when leading-edge triggering (+TR) is used or \overline{Q} is connected to +TR when trailing-edge triggering (-TR) is used. The time period (T) for this multivibrator can be calculated by: $T = R_X C_X$.

The minimum value of external resistance, R_X , is 4 K Ω . The minimum and maximum values of external capacitance, C_X , are 0 pF and 100 μ F, respectively.

The CD14538B is interchangeable with type MC14538 and is similar to and pin-compatible with the CD4098B* and CD4538B. It can replace the CD4538B which type is not recommended for new designs.

The CD14538B types are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix), 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (M, M96, MT, and NSR suffixes), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).

*T = 0.5 R_xC_x for $C_x \ge 1000 pF$ #T = R_xC_x ; $C_xmin = 5000 pF$

- Wide range of output-pulse widths
- Schmitt-trigger input allows unlimited rise and fall times on +TR and -TR inputs
- 100% tested for maximum quiescent current at 20 V
- Maximum input current of 1 µA at 18 V over full package-temperature range; 100 nA at 18 V and 25° C
- Noise margin (full package-temperature range):

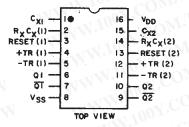
1 V at
$$V_{DD} = 5 V$$

2 V at $V_{DD} = 10 V$

- 2.5 V at VDD = 15 V
- 5-V, 10-V, and 15-V parametric ratings
- Standardized, symmetrical output characteristics
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices."

Applications:

- Pulse delay and timing
- Pulse shaping



TERMINALS 1,8,15 ARE ELECTRICALLY CONNECTED INTERNALLY

92CS-24848RI
Terminal Assignment

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MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (VDD)	
Voltages referenced to VSS Terminal)	0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS	+0.5V to Vpp +0.5V
DC INPUT CURRENT, ANY ONE INPUT	±10mA
DOMED DISCIPATION DED DACKAGE (D.).	
For T _A = +100°C to +125°C	500mW
For TA = +100°C to +125°C	Derate Linearity at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	COm.
FOR TA = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100mW
OPERATING-TEMPERATURE RANGE (TA)	55°C to +125°C
STORAGE TEMPERATURE RANGE (Tstg)	65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 \pm 1/32 inch (1.59 \pm 0.79mm) from case for 10s max	+265°C

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operating is always within the following ranges:

	CHARACTERISTIC		V _{DO}	CONTIN			
	CHARACTERISTIC		(V)	Min.	Max.	UNITS	
Supply-Voltage Range	(For T _A =Full Package-Temperature Range)	- 11	N 1	3	18	y	
Input Pulse Width	twn, tw.	1	5	140	M.TV	N N	
+TR, -TR, or RESET	WW.TOOY.COM.TW		10 15	80 60	JW IW	ns	

TABLE I CD4538B FUNCTIONAL TERMINAL CONNECTIONS

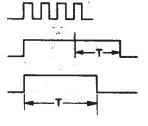
FUNCTIION	V _{DD}	TO M. NO.		TO VI. NO.	INPUT PULSE TO TERM. NO.		OTHER CONNECTIONS	
	MONO1	MONO ₂	MONO:	MONO ₂	MONO1	MONO ₂	MONO:	MONO ₂
Leading-Edge Trigger/ Retriggerable	3, 5	11,.13	N.100X	$co_{M,U}$	4	12	1003	$O_{M,I,\Lambda}$
Leading-Edge Trigger/ Non-Retriggerable	3	13	M.100	(CO_{M})	4	12	5-7	11-9
Trailing-Edge Trigger/ Retriggerable	3	. 13	4	12	5	11	West	
Trailing-Edge Trigger/ Non-Retriggerable	3	13	TN. Y	DOY.CO	5	11	4-6	12-10

NOTES:

- 1. A RETRIGGERABLE ONE-SHOT MULTIVIBRATOR HAS AN OUTPUT PULSE WIDTH WHICH IS EXTENDED ONE FULL TIME PERIOD (T) AFTER APPLICATION OF THE LAST TRIGGER PULSE.
- 2. A NON—RETRIGGERABLE ONE-SHOT MULTIVIBRATOR HAS A TIME PERIOD (T) REFERENCED FROM THE APPLICATION OF THE FIRST TRIGGER PULSE.

INPUT PULSE TRAIN

RETRIGGERABLE MODE PULSE WIDTH (+TR MODE) NON-RETRIGGERABLE MODE PULSE WIDTH (+TR MODE)



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STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CO	NDITIO	NS	LIMITS AT INDICATED TEMPERATURES (°C)							UNITS	
	V _o (V)	V _{IN} (V)	V ₀₀ (V)	-55	-40	+85	+125	Min.	+25 Typ.	Max.	DW.	
	$Q_{\overline{A}\overline{A}}$.	0,5	5	5	5	150	150	- 0	0.04	5		
uiescent Device	·	0,10	10	10	10	300	300	_	0.04	10	$CO_{N_{1}}$	
Current, I _{DD} Max.	(0,15	15	20	20	600	600	_	0.04	20	μΑ	
	COM	0,20	20	100	100	3000	3000	_	0.08	100	4 CO	
utput Low (Sink)	0.4	0,5	5 .	0.64	0.61	0.42	0.36	0.51	1	$a_{1p_{\mu}}$	- 00	
Current, IoL Min.	0.5	0,10	10	1.6	1.5	31.1	0.9	1.3	2.6	-1 40	DY.C	
COTTENIC, TOL WITH.	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	114.	W.C	
	4.6	0,5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	-1 5 1.	mA	
output High (Source)	2.5	0,5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	А. Т.	1 100X	
urrent, I _{OH} Min.	9.5	0,10	_10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	W N		
WW.	13.5	0,15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8			
Output Voltage:	11.	0,5	5		0.05				0	0.05	1001	
ow-Level, Vol. Max.	14 HOU?	0,10	10		0.	05	- 60	11.7	0	0.05	10,100	
JW ECYCI, VOE WIEX.	V - 400	0,15	15		0.	05	M.	A.V	0	0.05		
utput Voltage:	1/1/10	0,5	5	dKI	4.	95	N.C.	4.95	√ 5	- N	v	
ligh-Level, Von Min.	_ \si 10	0,10	10		9.	95	UV ×	9.95	10			
ngir Eovol, von Min.	$a_{M,m}$.	0,15	15		14	.95	on y.	14.95	15		1	
put Low Voltage,	0.5,4.5	0.0	5	-<1	1	.5	~ <1	$CO_{Z_{k,k}}$	-XN	1.5	MAN	
il Max.	1,9	10 0 7	10	111		3	1700 1.		77.77	3		
IF INITIAL	1.5,13.5	Toy	15	TIN		4	- 001	,CY	<u>~</u> \	4		
nput High Voltage,	0.5,4.5	$17m_{o}$.	5	1.1	3	.5	W.In.	3.5	- X	_		
mput riigii voitage, V⊪ Min.	1,9	$\sqrt{\pi}$ 00	10			7	_ < 100	7	$\sqrt{\pi}$	_] \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	
	1.5,13.5	117	15		N .	1	144.	11		V — .		
nput Current, _{IN} Max.		0,18	18	±0.1	±0.1	±1	±1	00₹.C	±10 ⁻⁵	(±0.1	μΑ	

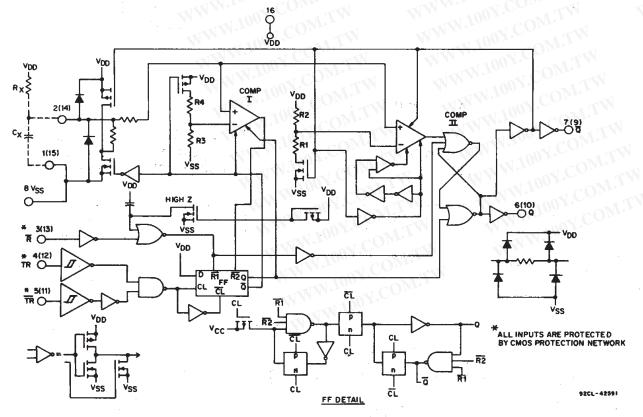


Fig. 1 - Logic diagram (1/2 of device shown).

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DYNAMIC ELECTRICAL CHARACTERISTICS, At TA=25° C; Input tr,tr=20 ns, CL=50 pF

CHARACTERISTIC		TEST CONDITIONS					
CHARACTERIST	JC .	V _{DD} (V)	Min.	Typ.	Max.	UNITS	
Transition Time	ttin, tthi	105	<i>I</i> —	100	200	Mon	
MW. To COM	TXN.	10	TIT	50	100	V.Co	
	$V_{i,I_{i,I_{i,I_{i}}}}$	15	- · ·	40	80	LI CON	
Propagation Delay Time:	telh, tehl	5,0	TIM	300	600		
+TR or -TR to Q or Q		10 CO	- W	150	300	NY.CU	
W 100 x.	M_{II}	15	1/1-	100	220	ns	
Reset to Q or Q		5	-TW	250	500	1007.0	
		10	ONF	125	250	Tow.C	
MM. 100X.	TIME	15		95	190	1700	
Minimum Input Pulse Width:	C twn, twn	5	UU- 11	80	140	100X	
+TR, -TR or Reset		10	CONT.	40	80	11.10	
	Y.C. TIN	15		30	60	X 100	
Output Pulse Width - Q or Q:	COMP. T.	5	198	210	230	100	
$C_X = 0.002 \mu F$, $R_X = 100 K\Omega$	0 $^{\circ}OM_{II}$	10	200	212	232	μs	
	ON TO	15	202	214	234	1	
$C_{x}=0.1 \mu F$, $R_{x}=100 K\Omega$	COM	5	9.4	9.97	10.5	M. M.	
	-100 A. TOW.	10	9.4	9.95	10.6	ms	
WWW.	CON. CO	15	9.5	10	10.6	M. A.	
C _x =10 μF, R _x =100 KΩ	1.100 CON	5	0.95	Obt	1.06		
		10	0.95	11.11	1.06	s	
Www	M. CO	15 WW	0.96	1.01	1.07	MM	
Pulse Width Match between	100 (T ₁ -T ₂)	5	11.10	(±1)	-XXI	- NIV	
circuits in same package: 🤍	1400	10	-400	±1	17.A.	%	
$C_x=0.1 \mu F$, $R_x=100 K\Omega$	WWI	15	MAIN.	±1	T 1 1	W	
Minimum Retrigger Time	t _{rr}	5	0	T-0N			
		10	0	1017	V 771	ns	
·	TWW.IO	15	0	L _A CO	-W		
Input Capacitance	Cin	Any Input	-XX	5	7.5	pF	

^{*}Note: Minimum R_x value=4 KΩ, minimum C_x value=5000 pF.

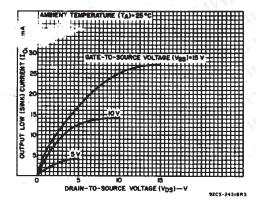


Fig. 2 - Typical output low (sink) current characteristics.

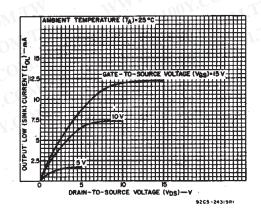


Fig. 3 - Minimum output low (sink) current characteristics.

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CD14538B Types

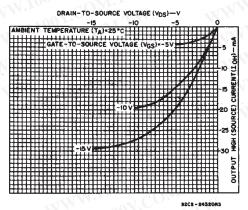


Fig. 4 - Typical output high (source) current characteristics.

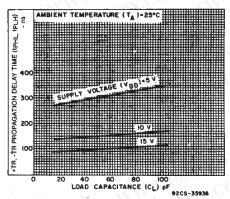


Fig. 6 - Typical propagation delay time as a function of load capacitance (+TR or −TR to Q or Q).

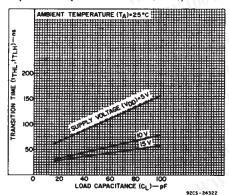


Fig. 8 - Typical transition time as a function of load capacitance.

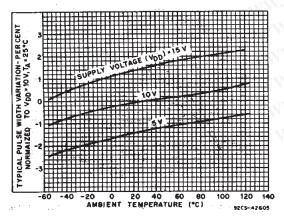


Fig. 10 - Typical pulse-width variation as a function of temperature ($R_X=100 \text{ K}\Omega$, $C_X=0.1 \mu\text{F}$).

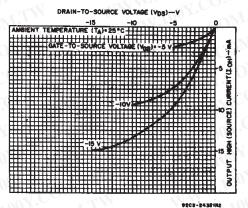


Fig. 5 - Minimum output high (source) current characteristics.

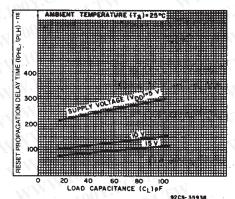


Fig. 7 - Typical propagation delay time as a function of load capacitance (RESET to Q or Q).

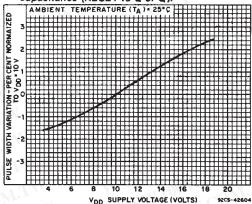


Fig. 9 - Typical pulse-width variation as a function of supply voltage.

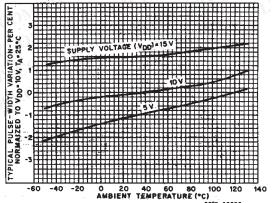


Fig. 11 - Typical pulse-width variation as a function of temperature ($R_X=100 \text{ K}\Omega$, $C_X=2000 \text{ pF}$).

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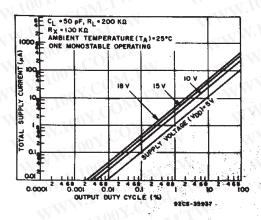


Fig. 12 - Typical total supply current as a function of output duty cycle.

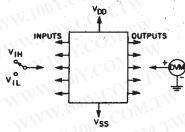
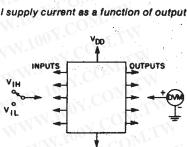


Fig. 14 - Input voltage test circuit.

NOTE:

fied limit.



R_X = 100 KΩ TA = 25 °C SUPPLY VOLTAGE (VDD) = 15 10 V 8 100 K 81 1000 100 10K CX CAPACITANCE (pfs)

Fig. 13 - Typical total supply current as a function of load capacitance.

1. Test any combination of inputs. 2. When measuring VIH or VIL for Schmitt trigger inputs (+TR, -TR), the input must first be brought to VDD or Vss. respectively, then reduced to the speci-

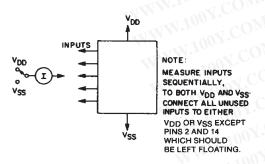


Fig. 15 - Input leakage-current test circuit.

VDD VDD INPUTS o Vss (t_{DD})

Fig. 16 - Quiescent device current test circuit.

Power-Down Mode

During a rapid power-down condition, as would occur with a power-supply short circuit or with a poorly filtered power supply, the energy stored in Cx could discharge into Pin 2 or 14. To avoid possible device damage in this mode, when C_x is ≥ 0.5 microfarad, a protection diode with a 1-ampere or higher rating (1N5395 or equivalent) and a separate ground return for Cx should be provided as shown in Fig. VDD

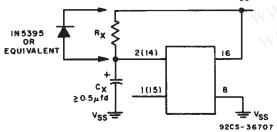


Fig. 17 - Rapid power-down protection circuit.

An alternate protection method is shown in Fig. 18, where a 51-ohm current-limiting resistor is inserted in series with Cx. Note that a small pulse width decrease will occur however, and Rx must be appropriately increased to obtain the originally desired pulse width.

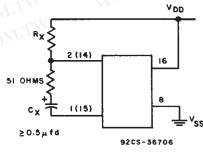
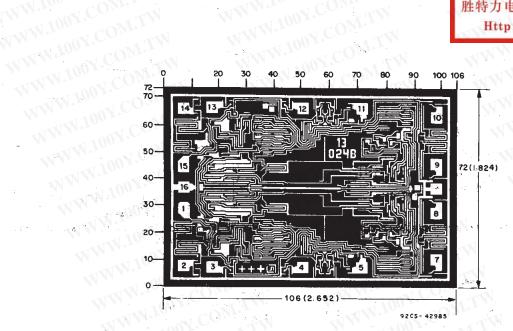


Fig. 18 - Alternate rapid power-down protection circuit.

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Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch) .

Dimensions and pad layout for CD14538BH.

PACKAGE OPTION ADDENDUM





PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finis	n MSL Peak Temp ⁽³⁾
5962-9055701EA	ACTIVE	CDIP	J	16	01	None	Call TI	Level-NC-NC-NC
CD14538BE	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
CD14538BF	ACTIVE	CDIP	J	16	$_{\rm J}$ (10 $^{ m N}$	None	Call TI	Level-NC-NC-NC
CD14538BF3A	ACTIVE	CDIP	J	16	100	None	Call TI	Level-NC-NC-NC
CD14538BM	ACTIVE	SOIC	D	16	40	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR Level-1-235C-UNLIM
CD14538BM96	ACTIVE	SOIC	D	16	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR Level-1-235C-UNLIM
CD14538BMT	ACTIVE	SOIC	D	16	250	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR Level-1-235C-UNLIM
CD14538BNSR	ACTIVE	SO	NS	16	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR Level-1-235C-UNLIM
CD14538BPW	ACTIVE	TSSOP	PW	16	90	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
CD14538BPWR	ACTIVE	TSSOP	PW	16	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - May not be currently available - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

None: Not yet available Lead (Pb-Free).

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

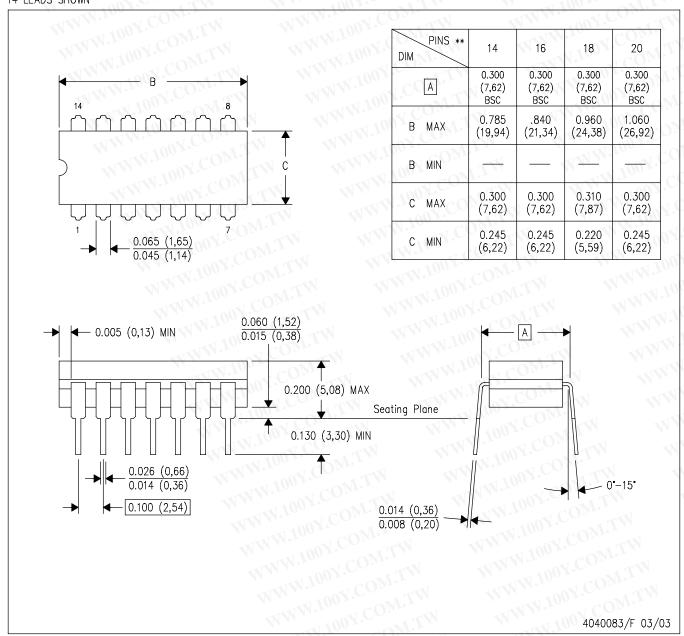
Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDECindustry standard classifications, and peak solder temperature.

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14 LEADS SHOWN



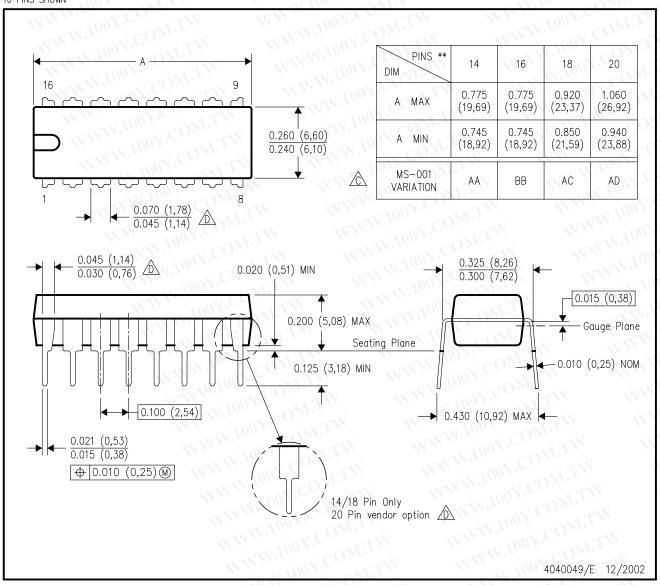
NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

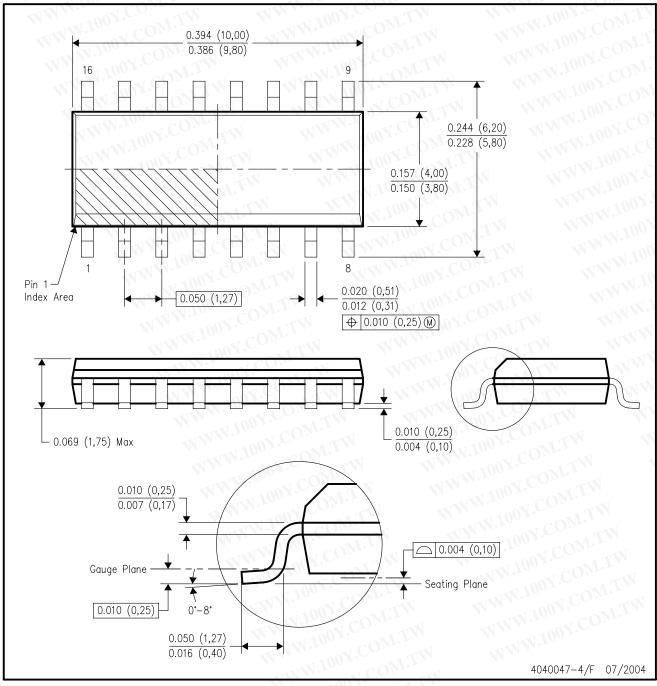
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- ⚠ The 20 pin end lead shoulder width is a vendor option, either half or full width.



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D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

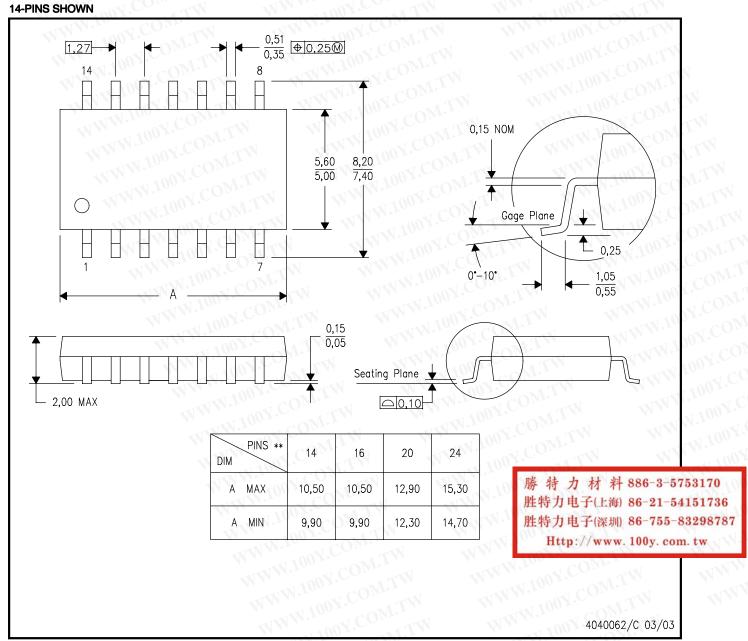
- All linear dimensions are in inches (millimeters).
- В. This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15). C.
- D. Falls within JEDEC MS-012 variation AC.



MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

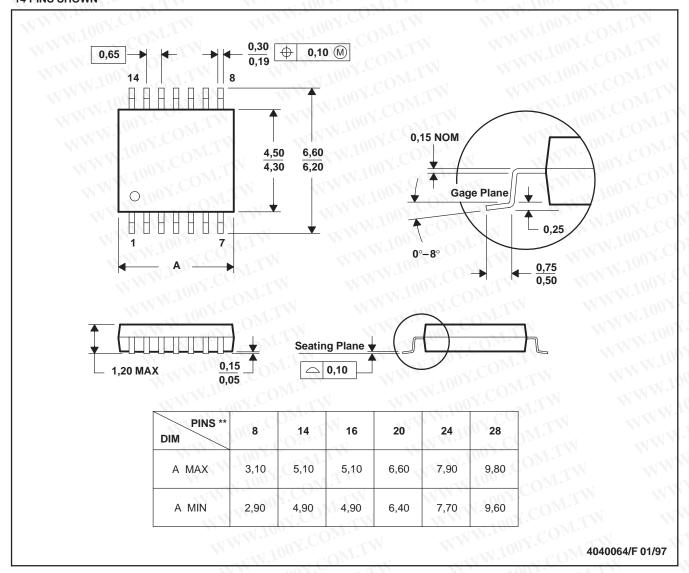
- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



PW (R-PDSO-G**)

14 PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.

D. Falls within JEDEC MO-153



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