

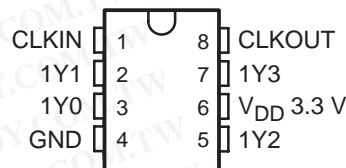
CDCVF2505

3.3-V CLOCK PHASE-LOCK LOOP CLOCK DRIVER

SCAS640E – JULY 2000 – REVISED MARCH 2005

- Phase-Lock Loop Clock Driver for Synchronous DRAM and General-Purpose Applications
- Spread Spectrum Clock Compatible
- Operating Frequency: 24 MHz to 200 MHz
- Low Jitter (Cycle-cycle): $<|150\text{ ps}|$ Over the Range 66 MHz–200 MHz
- Distributes One Clock Input to One Bank of Five Outputs (CLKOUT Is Used to Tune the Input-Output Delay)
- Three-States Outputs When There Is no Input Clock
- Operates From Single 3.3-V Supply
- Available in 8-Pin TSSOP and 8-Pin SOIC Packages
- Consumes Less Than 100 μA (Typically) in Power Down Mode
- Internal Feedback Loop Is Used to Synchronize the Outputs to the Input Clock
- 25- Ω On-Chip Series Damping Resistors
- Integrated RC PLL Loop Filter Eliminates the Need for External Components

D OR PW PACKAGE
(TOP VIEW)



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description

The CDCVF2505 is a high-performance, low-skew, low-jitter, phase-lock loop (PLL) clock driver. It uses a PLL to precisely align, in both frequency and phase, the output clocks (1Y[0–3] and CLKOUT) to the input clock signal (CLKIN). The CDCVF2505 operates at 3.3 V. It also provides integrated series-damping resistors that make it ideal for driving point-to-point loads.

One bank of five outputs provides low-skew, low-jitter copies of CLKIN. Output duty cycles are adjusted to 50 percent, independent of duty cycle at CLKIN. The device automatically goes in power-down mode when no input signal is applied to CLKIN.

Unlike many products containing PLLs, the CDCVF2505 does not require an external RC network. The loop filter for the PLLs is included on-chip, minimizing component count, space, and cost.

Because it is based on the PLL circuitry, the CDCVF2505 requires a stabilization time to achieve phase lock of the feedback signal to the reference signal. This stabilization is required following power up and application of a fixed-frequency, fixed-phase signal at CLKIN, and following any changes to the PLL reference.

The CDCVF2505 is characterized for operation from -40°C to 85°C .



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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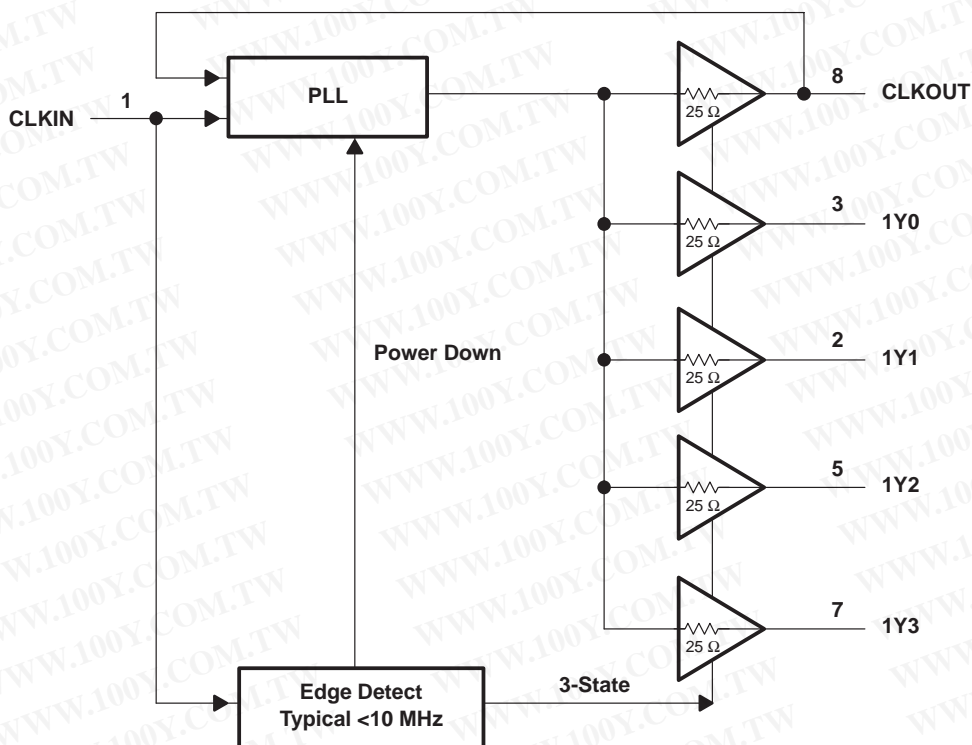
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FUNCTION TABLE

INPUT	OUTPUTS	
	1Y (0:3)	CLKOUT
L	L	L
H	H	H
<10 MHz†	Z	Z

† Typically, below 2 MHz the device goes in power-down mode in which the PLL is turned off and the outputs enter into Hi-Z mode. If a >10-MHz signal is applied at CLKIN the PLL turns on, reacquires lock, and stabilizes after approximately 100 μs. The outputs will then be enabled.

functional block diagram



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Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
1Y[0–3]	2, 3, 5, 7	O	Clock outputs. These outputs are low-skew copies of CLKIN. Each output has an integrated 25- Ω series damping resistor.
CLKIN	1	I	Clock input. CLKIN provides the clock signal to be distributed by the CDCVF2505 clock driver. CLKIN is used to provide the reference signal to the integrated PLL that generates the clock output signals. CLKIN must have a fixed frequency and fixed phase for the PLL to obtain phase lock. Once the circuit is powered up and a valid signal is applied, a stabilization time (100 μ s) is required for the PLL to phase lock the feedback signal to CLKIN.
CLKOUT	8	O	Feedback output. CLKOUT completes the internal feedback loop of the PLL. This connection is made inside the chip and an external feedback loop should NOT be connected. CLKOUT can be loaded with a capacitor to achieve zero delay between CLKIN and the Y outputs.
GND	4	Power	Ground
V _{DD3.3V}	6	Power	3.3-V Supply

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V _{DD}	–0.5 V to 4.3 V
Input voltage range, V _I (see Notes 1 and 2)	–0.5 V to V _{DD} + 0.5 V
Output voltage range, V _O (see Notes 1 and 2)	–0.5 V to V _{DD} + 0.5 V
Input clamp current, I _{IK} (V _I < 0 or V _I > V _{DD})	±50 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{DD})	±50 mA
Continuous total output current, I _O (V _O = 0 to V _{DD})	±50 mA
Package thermal impedance, θ_{JA} (see Note 3): D package	165.5°C/W
PWR package	230.5°C/W
Storage temperature range, T _{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This value is limited to 4.3 V maximum.
 3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V _{DD}	3	3.3	3.6	V
High-level input voltage, V _{IH}	0.7 V _{DD}			V
Low-level input voltage, V _{IL}	0.3 V _{DD}			V
Input voltage, V _I	0	V _{DD}		V
High-level output current, I _{OH}	–12			mA
Low-level output current, I _{OL}	12			mA
Operating free-air temperature, T _A	–40	85		°C

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timing requirements over recommended ranges of supply voltage and operating free-air temperature

		MIN	NOM	MAX	UNIT
f_{clk}	Clock frequency	24		200	MHz
	Input clock duty cycle	24 MHz – 85 MHz (see Note 4)		30%	85%
		86 MHz – 200 MHz		40%	50% 60%
Stabilization time (see Note 5)				100	μ s

NOTES: 4. Ensured by design but not 100% production tested.

5. Time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal. For phase lock to be obtained, a fixed-frequency, fixed-phase reference signal must be present at CLKIN. Until phase lock is obtained, the specifications for propagation delay, skew, and jitter parameters given in the switching characteristics table are not applicable. This parameter does not apply for input modulation under SSC application.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{DD}	MIN	TYP†	MAX	UNIT
V_{IK}	Input voltage	$I_I = -18$ mA	3 V			-1.2	V
V_{OH}	High-level output voltage	$I_{OH} = -100$ μ A	MIN to MAX	$V_{DD}-0.2$			V
		$I_{OH} = -12$ mA	3 V	2.1			
		$I_{OH} = -6$ mA	3 V	2.4			
V_{OL}	Low-level output voltage	$I_{OL} = 100$ μ A	MIN to MAX			0.2	V
		$I_{OL} = 12$ mA	3 V			0.8	
		$I_{OL} = 6$ mA	3 V			0.55	
I_{OH}	High-level output current	$V_O = 1$ V	3 V			-27	mA
		$V_O = 1.65$ V	3.3 V			-36	
I_{OL}	Low-level output current	$V_O = 2$ V	3 V			27	mA
		$V_O = 1.65$ V	3.3 V			40	
I_I	Input current	$V_I = 0$ V or V_{DD}				± 5	μ A
C_i	Input capacitance	$V_I = 0$ V or V_{DD}	3.3 V			4.2	pF
C_o	Output capacitance	Y_n	3.3 V			2.8	pF
		CLKOUT				5.2	

† All typical values are at respective nominal V_{DD} and 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 25$ pF, $V_{DD} = 3.3$ V \pm 0.3 V (see Note 5)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{pd}	Propagation delay (normalized (see Figure 3))	CLKIN to Y_n , $f = 66$ MHz to 200 MHz	-150		150	ps
$t_{sk(o)}$	Output skew (see Note 6)	Y_n to Y_n			150	ps
$t_{c(jit_cc)}$	Jitter (cycle to cycle) (see Figure 5)	$f = 66$ MHz to 200 MHz		70	150	ps
		$f = 24$ MHz to 50 MHz		200	400	
odc	Output duty cycle (see Figure 4)	$f = 24$ MHz to 200 MHz at 50% V_{DD}	45%		55%	
t_r	Rise time	$V_O = 0.4$ V to 2 V	0.5		2	ns
t_f	Fall time	$V_O = 2$ V to 0.4 V	0.5		2	ns

† All typical values are at respective nominal V_{DD} and 25°C.

NOTE 6: The $t_{sk(o)}$ specification is only valid for equal loading of all outputs.



ESD information

ESD MODELS	LIMIT
Human Body Model (HBM)	2.0 kV
Machine Model (MM)	300 V
Charge Device Model (CDM)	1 kV

thermal information

CDCVF2505 8-PIN SOIC			THERMAL AIR FLOW (CFM)				UNIT
			0	150	250	500	
R _{θJA}	High K		97	87	83	77	°C/W
R _{θJA}	Low K		165	126	113	97	°C/W
R _{θJC}	High K	39					°C/W
R _{θJC}	Low K	42					°C/W

CDCVF2505 8-PIN TSSOP			THERMAL AIR FLOW (CFM)				UNIT
			0	150	250	500	
R _{θJA}	High K		149	142	138	132	°C/W
R _{θJA}	Low K		230	185	170	150	°C/W
R _{θJC}	High K	65					°C/W
R _{θJC}	Low K	69					°C/W

TYPICAL CHARACTERISTICS

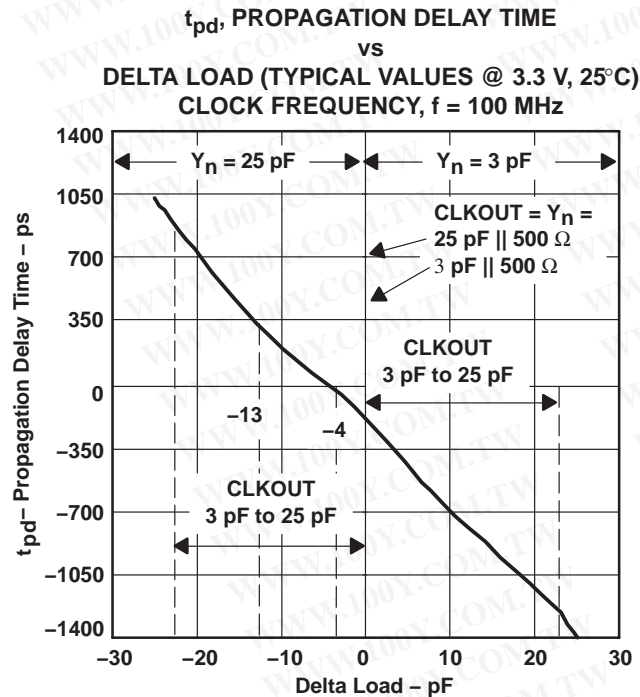


Figure 1

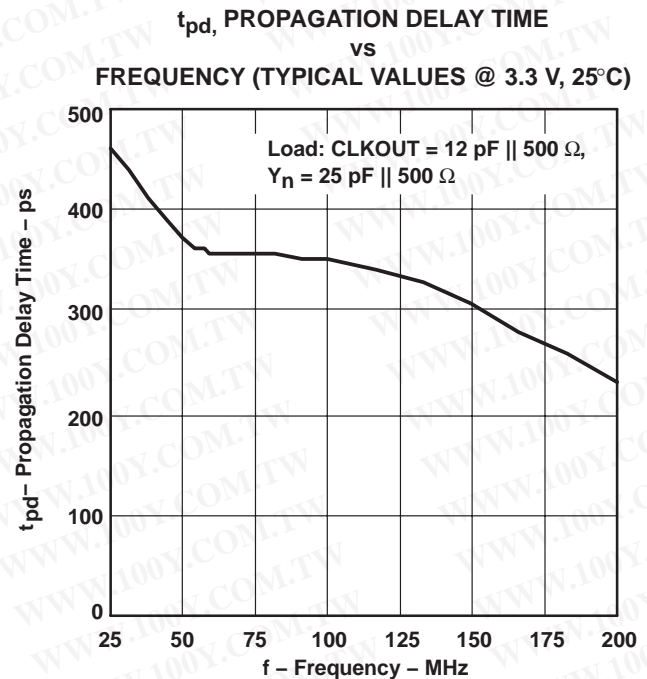


Figure 2

NOTE: Delta Load = CLKOUT Load – Yn Load

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TYPICAL CHARACTERISTICS

t_{pd} , TYPICAL PROPAGATION DELAY TIME
vs
FREQUENCY(TUNED FOR MINIMUM DELAY)

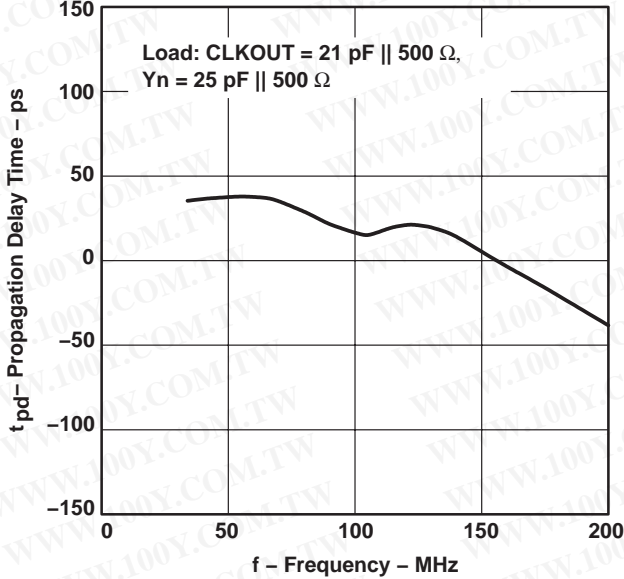


Figure 3

DUTY CYCLE
vs
FREQUENCY

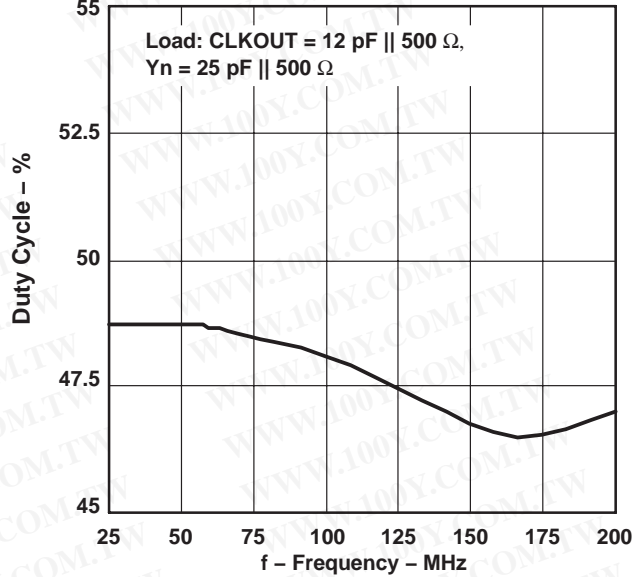


Figure 4

CYCLE-CYCLE JITTER
vs
FREQUENCY

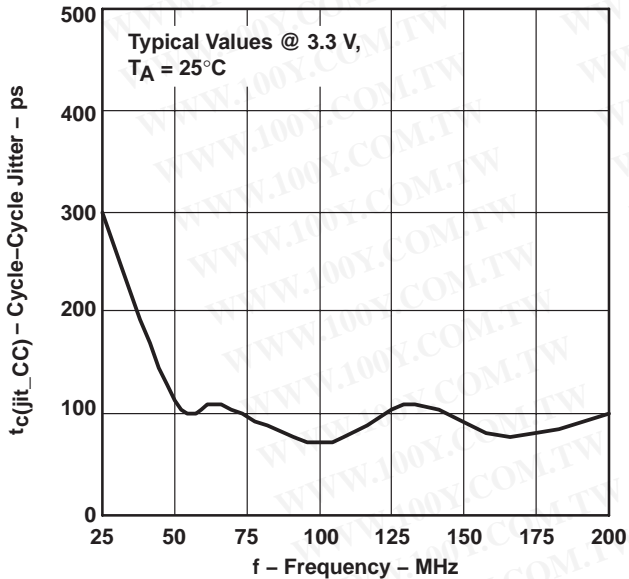


Figure 5

I_{CC} , SUPPLY CURRENT
vs
FREQUENCY

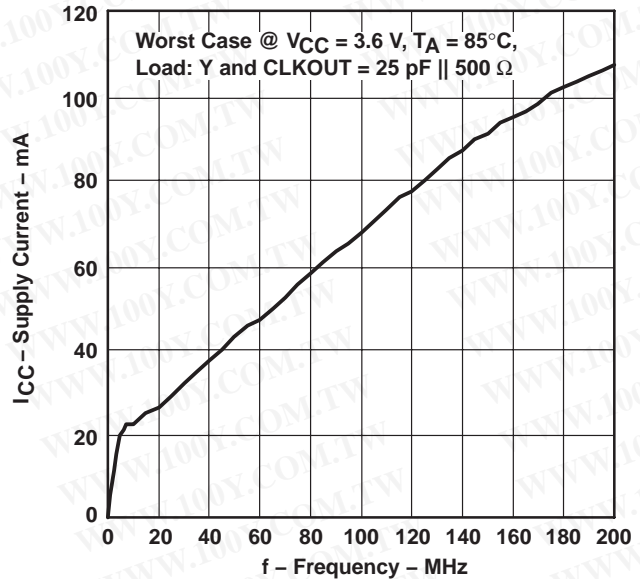


Figure 6



PARAMETER MEASUREMENT INFORMATION

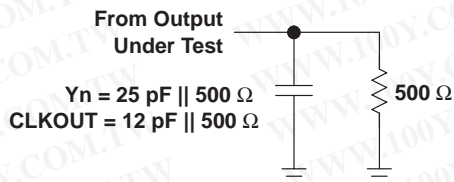


Figure 7. Test Load Circuit

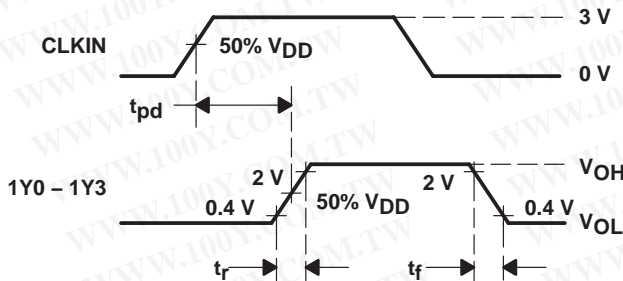


Figure 8. Voltage Threshold for Measurements, Propagation Delay (t_{pd})

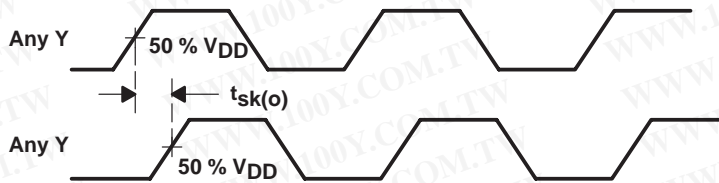


Figure 9. Output Skew

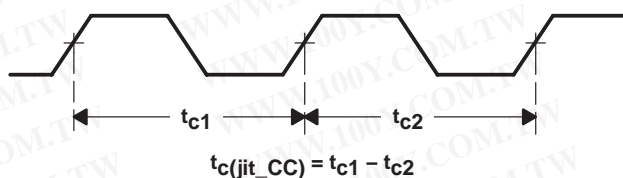
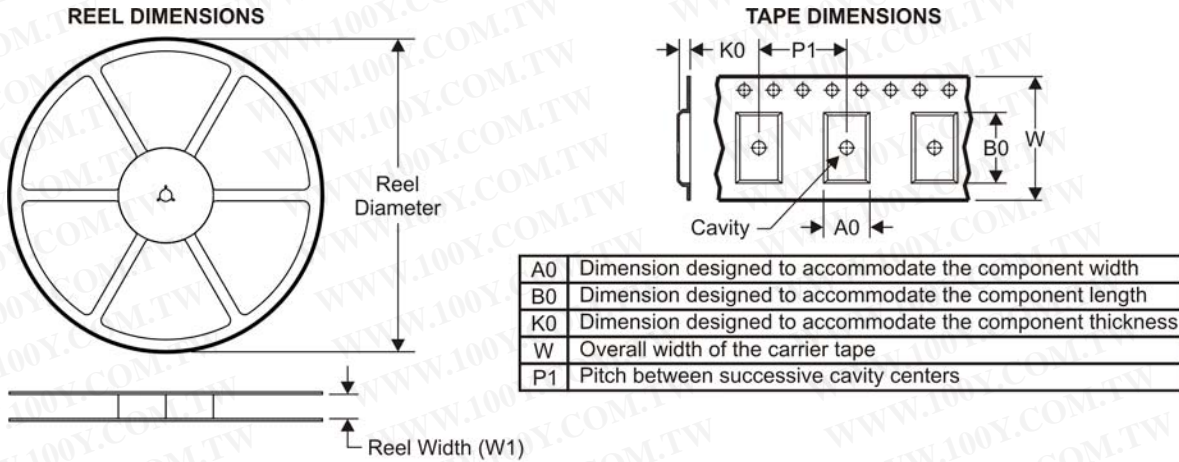


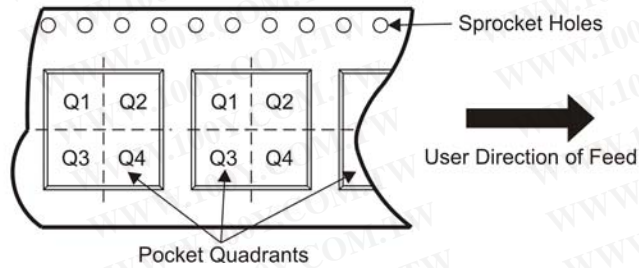
Figure 10. Cycle-to-Cycle Jitter

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

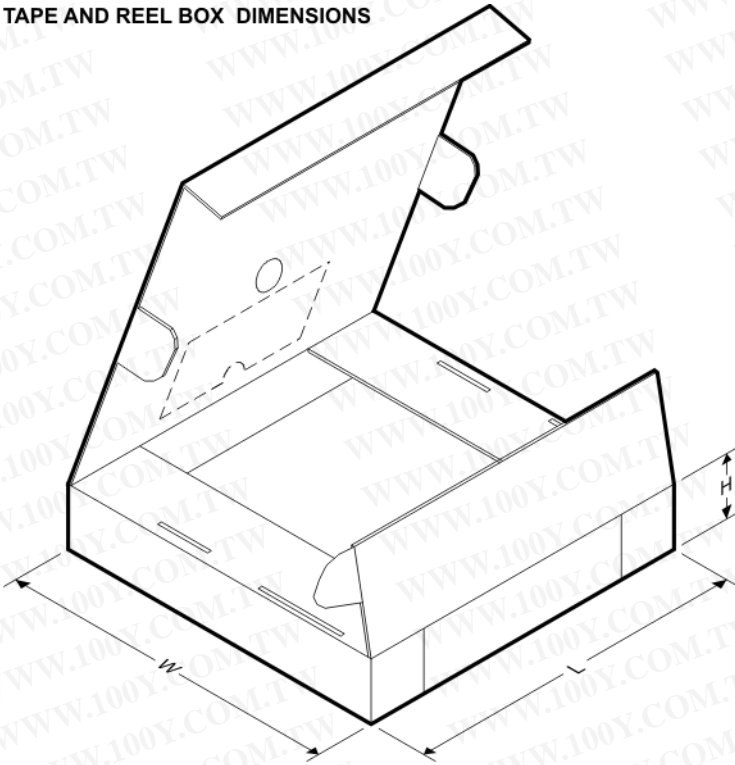


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCVF2505DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
CDCVF2505PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

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TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

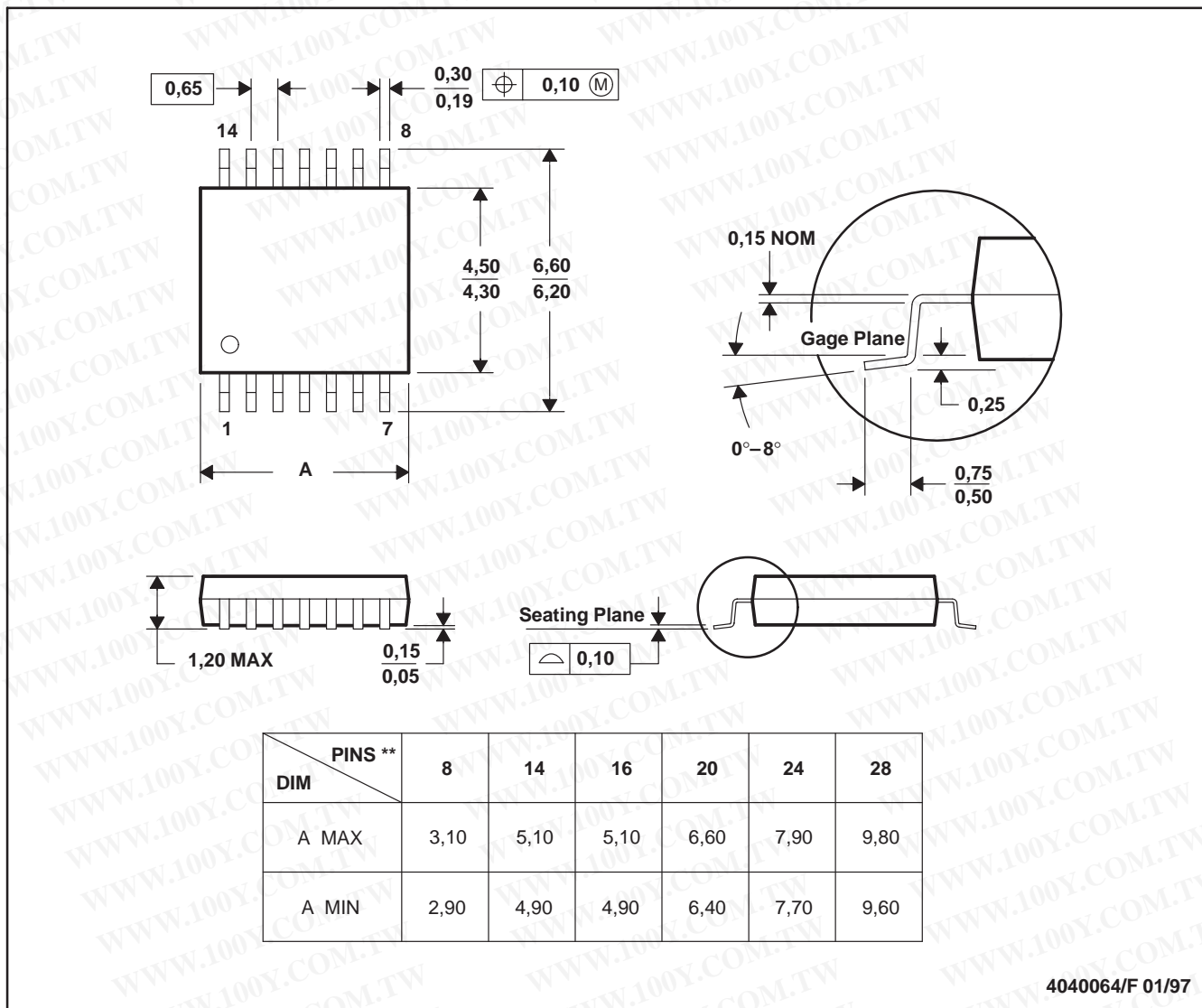
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDCVF2505DR	SOIC	D	8	2500	346.0	346.0	29.0
CDCVF2505PWR	TSSOP	PW	8	2000	346.0	346.0	29.0

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PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



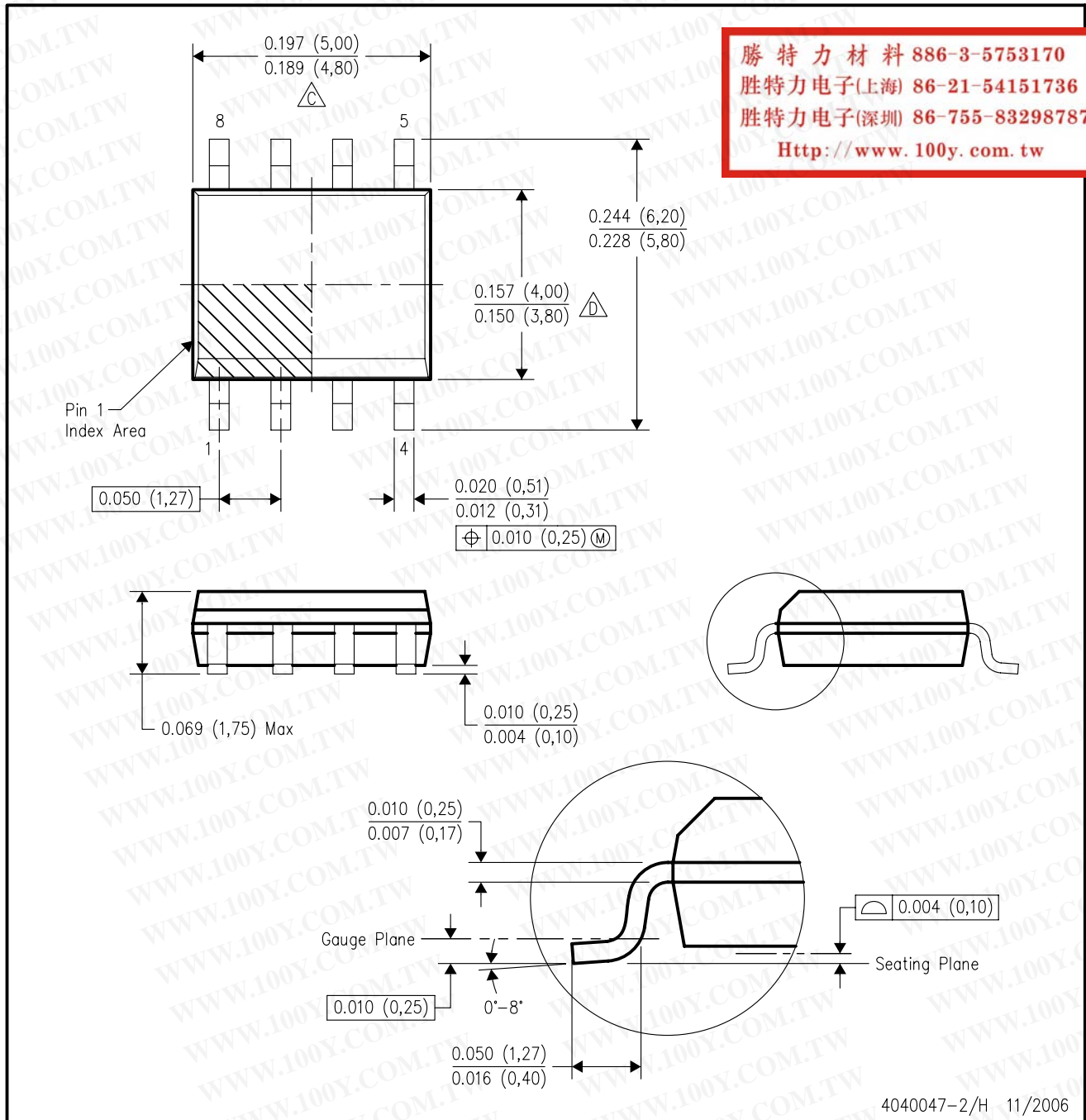
- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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D (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE

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- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
 - E. Reference JEDEC MS-012 variation AA.