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 Http://www.100y.com.tw

# DMOS 250mA Low-Dropout Regulator

## FEATURES

- **NEW DMOS TOPOLOGY:**  
 Ultra Low Dropout Voltage:  
 150mV typ at 250mA  
 Output Capacitor *not* Required for Stability
- **FAST TRANSIENT RESPONSE**
- **VERY LOW NOISE:** 28µVrms
- **HIGH ACCURACY:** ±1.5% max
- **HIGH EFFICIENCY:**  
 $I_{GND} = 600\mu A$  at  $I_{OUT} = 250mA$   
 Not Enabled:  $I_{GND} = 0.01\mu A$
- **2.5V, 2.8V, 2.85V, 3.0V, 3.3V, AND 5.0V  
 ADJUSTABLE OUTPUT VERSIONS**
- **OTHER OUTPUT VOLTAGES AVAILABLE UPON  
 REQUEST**
- **FOLDBACK CURRENT LIMIT**
- **THERMAL PROTECTION**
- **SMALL SURFACE-MOUNT PACKAGES:**  
 SOT23-5, SOT223-5, and SO-8

## APPLICATIONS

- **PORTABLE COMMUNICATION DEVICES**
- **BATTERY-POWERED EQUIPMENT**
- **PERSONAL DIGITAL ASSISTANTS**
- **MODEMS**
- **BAR-CODE SCANNERS**
- **BACKUP POWER SUPPLIES**

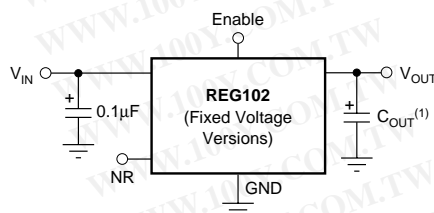
## DESCRIPTION

The REG102 is a family of low-noise, low-dropout linear regulators with low ground pin current. The new DMOS topology provides significant improvement over previous designs, including low-dropout voltage (only 150mV typ at full load), and better transient performance. In addition, no output capacitor is required for stability, unlike conventional low-dropout regulators that are difficult to compensate and require expensive low ESR capacitors greater than 1µF.

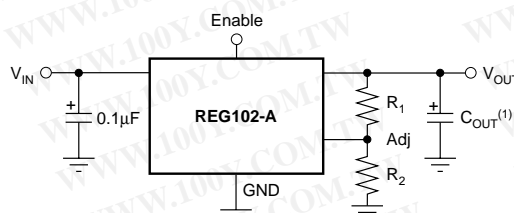
Typical ground pin current is only 600µA (at  $I_{OUT} = 250mA$ ) and drops to 10nA when not enabled. Unlike regulators with PNP pass devices, quiescent current remains relatively constant over load variations and under dropout conditions.

The REG102 has very low output noise (typically 28µVrms for  $V_{OUT} = 3.3V$  with  $C_{NR} = 0.01\mu F$ ), making it ideal for use in portable communications equipment. On-chip trimming results in high output voltage accuracy. Accuracy is maintained over temperature, line, and load variations. Key parameters are tested over the specified temperature range (–40°C to +85°C).

The REG102 is well protected—internal circuitry provides a current limit that protects the load from damage; furthermore, thermal protection circuitry keeps the chip from being damaged by excessive temperature. The REG102 is available in SOT23-5, SOT223-5, and SO-8 packages.



NR = Noise Reduction



NOTE: (1) Optional.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Supply Input Voltage, $V_{IN}$ .....	-0.3V to 12V
Enable Input Voltage, $V_{EN}$ .....	-0.3V to $V_{IN}$
Feedback Voltage, $V_{FB}$ .....	-0.3V to 6.0V
NR Pin Voltage, $V_{NR}$ .....	-0.3V to 6.0V
Output Short-Circuit Duration .....	Indefinite
Operating Temperature Range ( $T_J$ ) .....	-55°C to +125°C
Storage Temperature Range ( $T_A$ ) .....	-65°C to +150°C
Lead Temperature (soldering, 3s) .....	+240°C

NOTE: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability.



## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## PACKAGE/ORDERING INFORMATION<sup>(1)</sup>

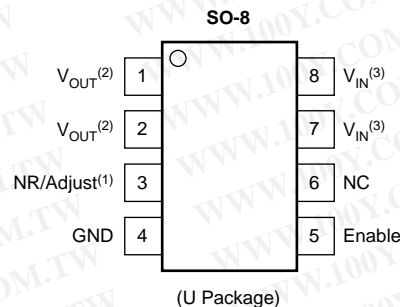
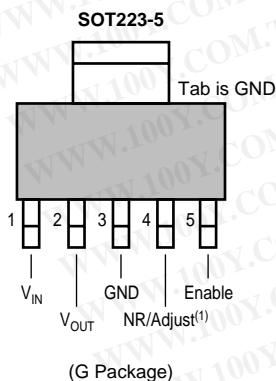
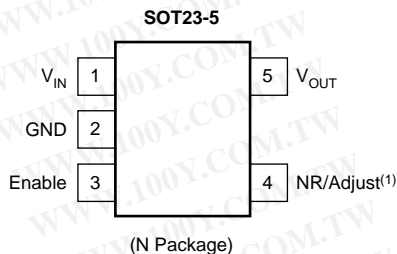
PRODUCT	$V_{OUT}$ <sup>(2)</sup>
REG102xx-yyy/zzz	<p>XX is package designator.</p> <p>YYYY is typical output voltage (5 = 5.0V, 2.85 = 2.85V, A = Adjustable).</p> <p>ZZZ is package quantity.</p>

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).

(2) Output voltages from 2.5V to 5.1V in 50mV increments are available; minimum order quantities apply. Contact factory for details and availability.

## PIN CONFIGURATIONS

Top View



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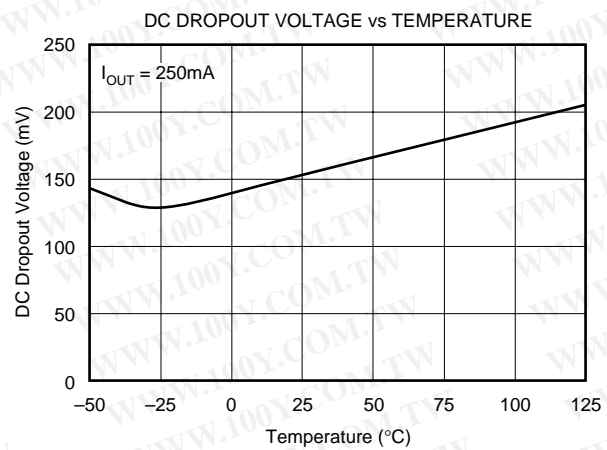
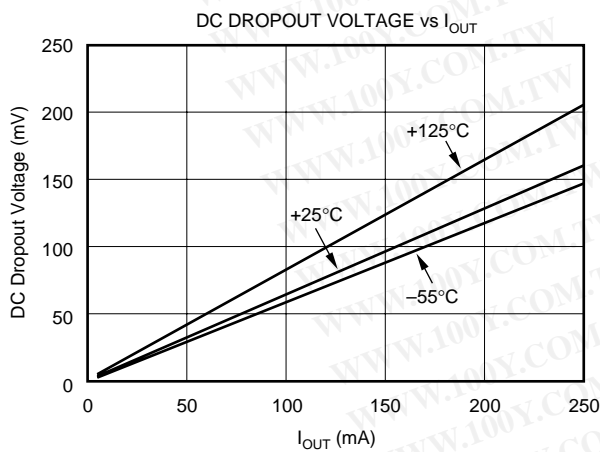
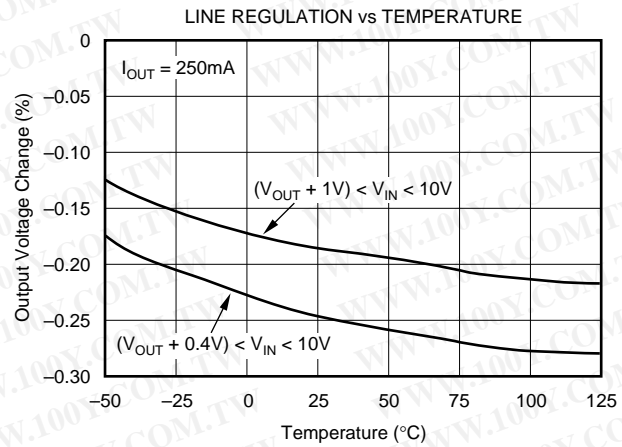
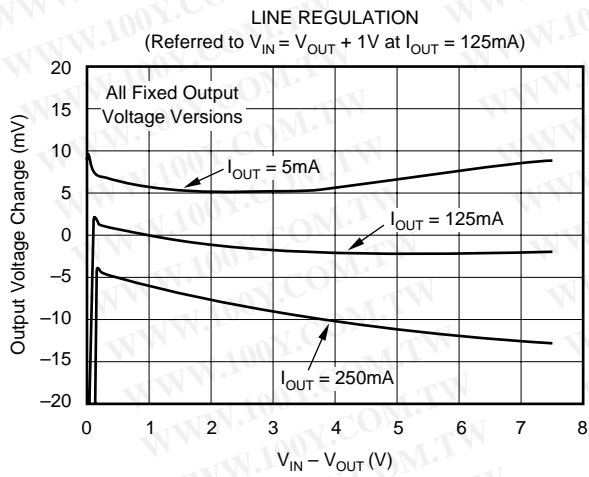
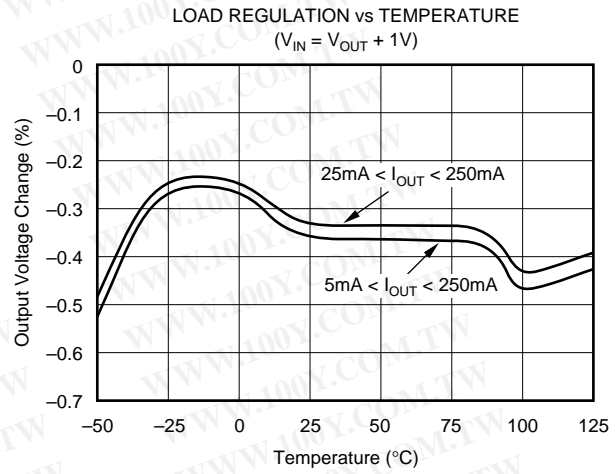
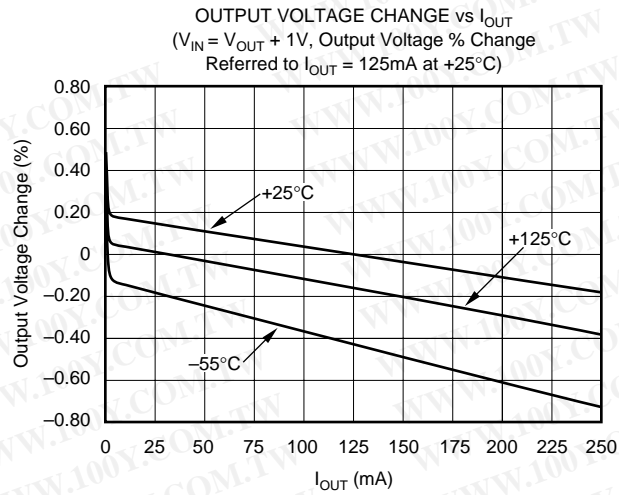
NOTES: (1) For REG102A-A: voltage setting resistor pin.  
 All other models: noise reduction capacitor pin.  
 (2) Both pin 1 and pin 2 must be connected.  
 (3) Both pin 7 and pin 8 must be connected.





# TYPICAL CHARACTERISTICS

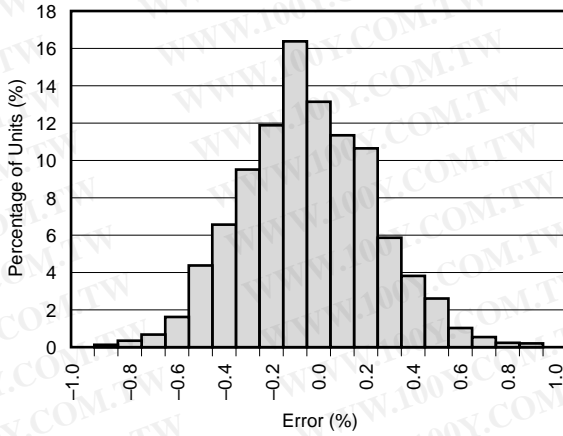
For all models, at  $T_J = +25^\circ\text{C}$  and  $V_{\text{ENABLE}} = 1.8\text{V}$ , unless otherwise noted.



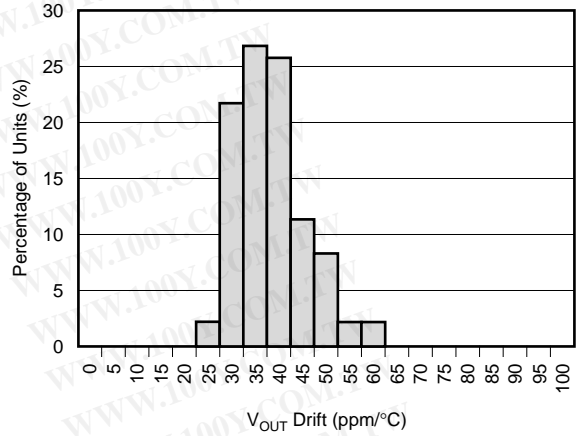
# TYPICAL CHARACTERISTICS (Cont.)

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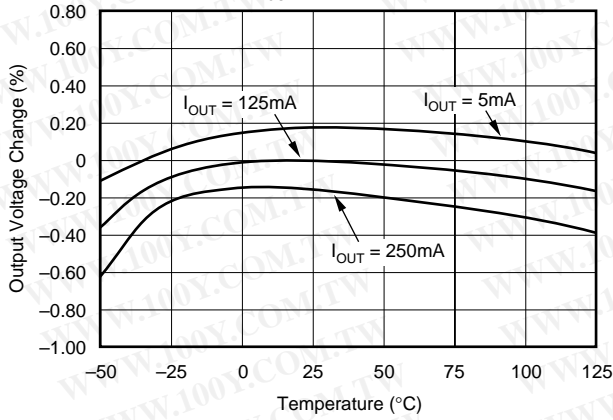
OUTPUT VOLTAGE ACCURACY HISTOGRAM



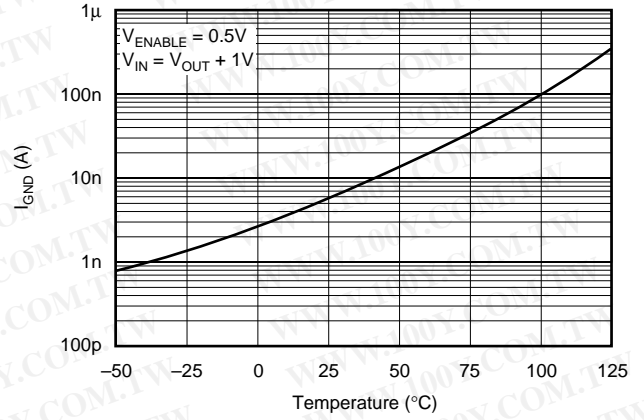
OUTPUT VOLTAGE DRIFT HISTOGRAM



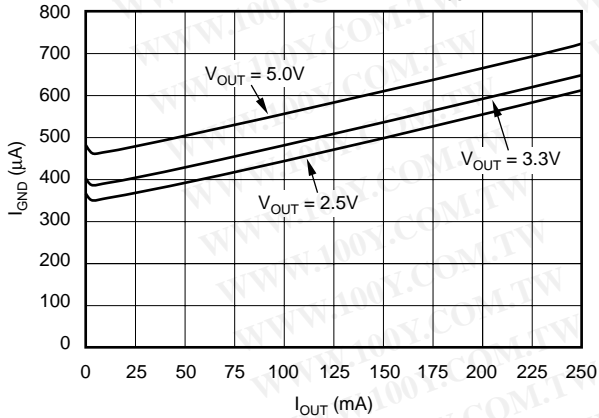
OUTPUT VOLTAGE vs TEMPERATURE  
(Output Voltage % Change Referred  
to  $I_{\text{OUT}} = 125\text{mA}$  at  $+25^\circ\text{C}$ )



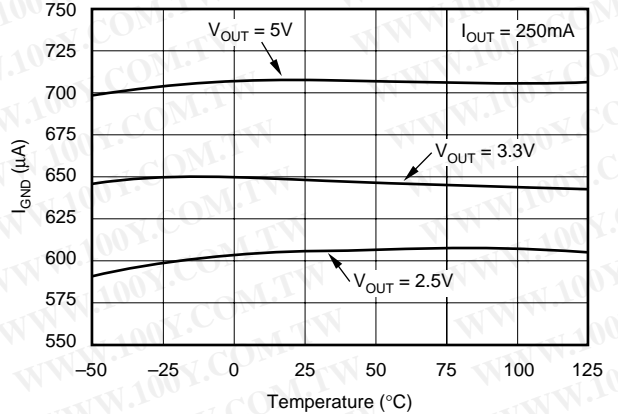
GROUND PIN CURRENT, NOT ENABLED  
vs TEMPERATURE



GROUND PIN CURRENT vs  $I_{\text{OUT}}$

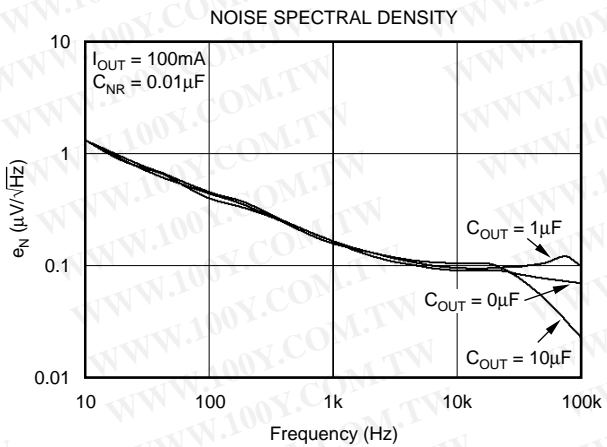
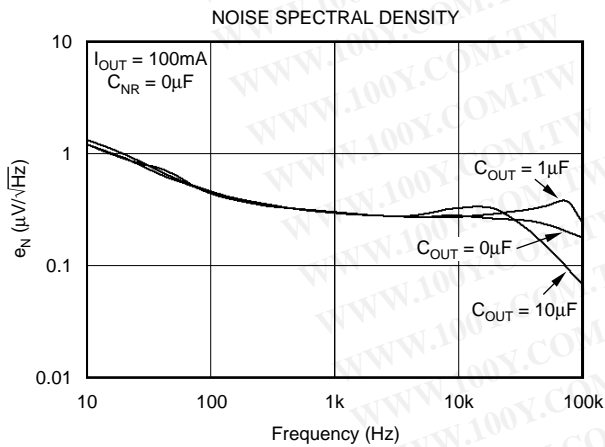
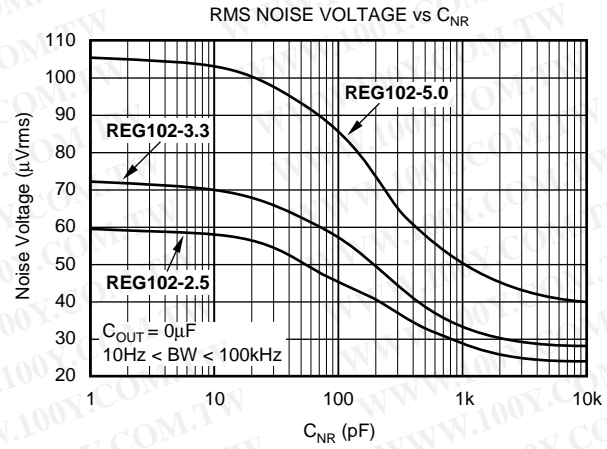
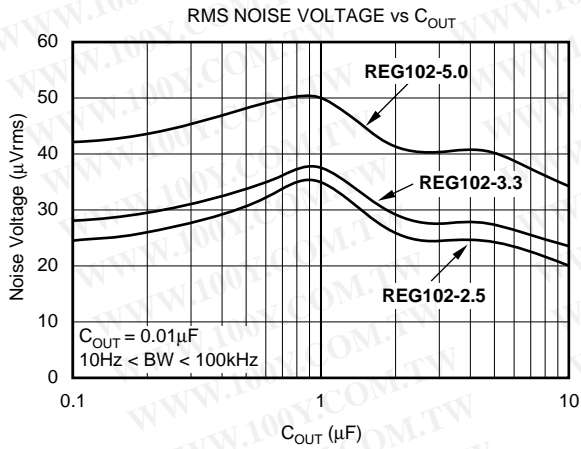
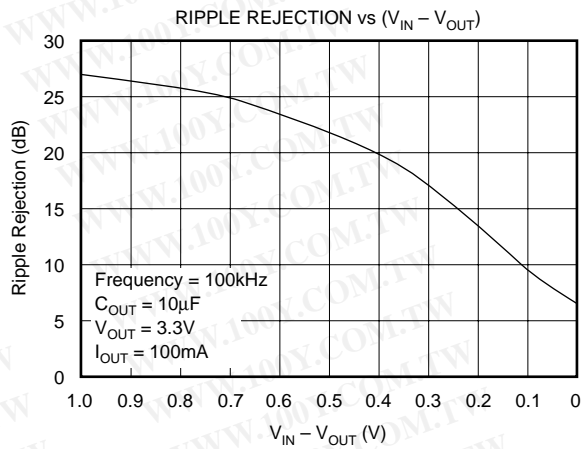
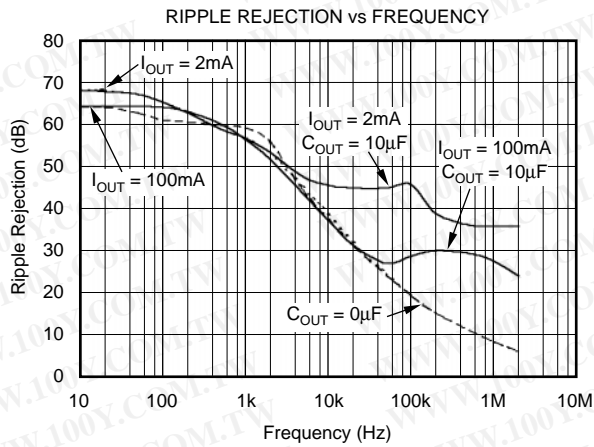


GROUND PIN CURRENT vs TEMPERATURE



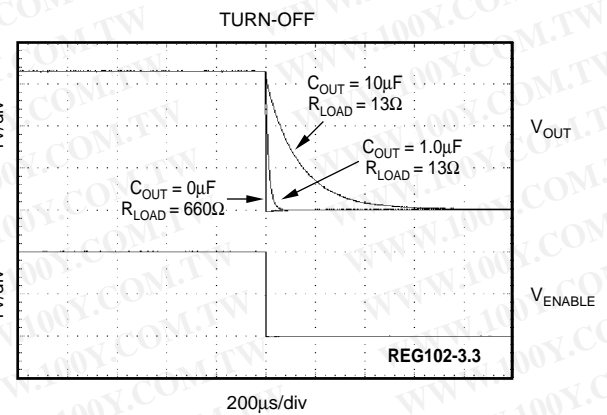
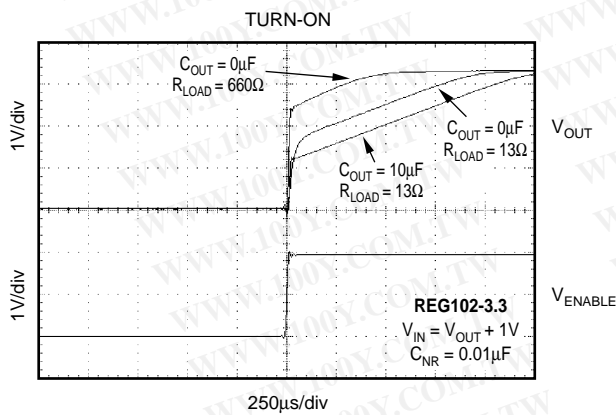
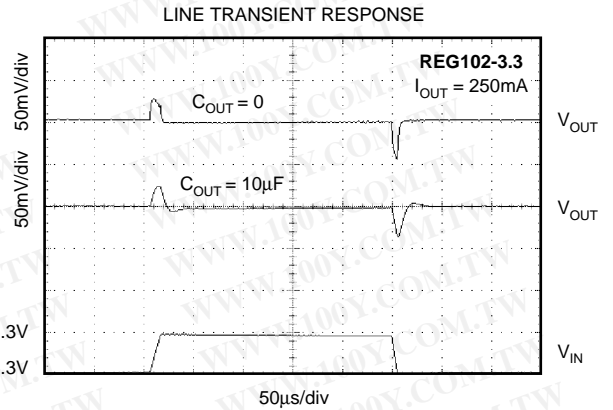
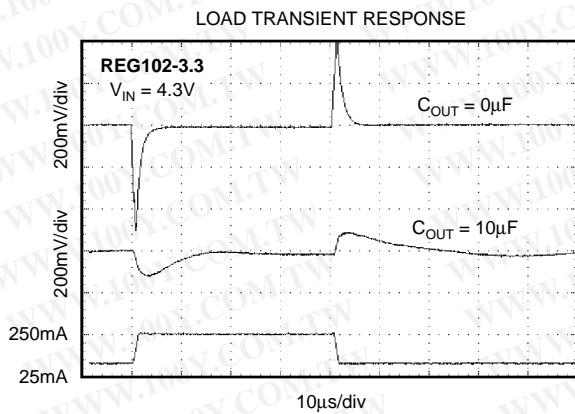
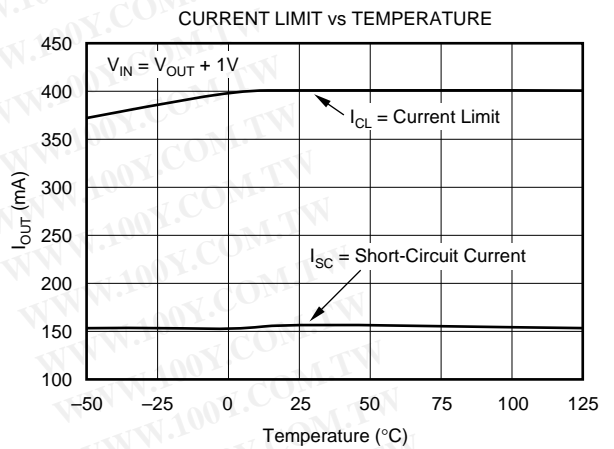
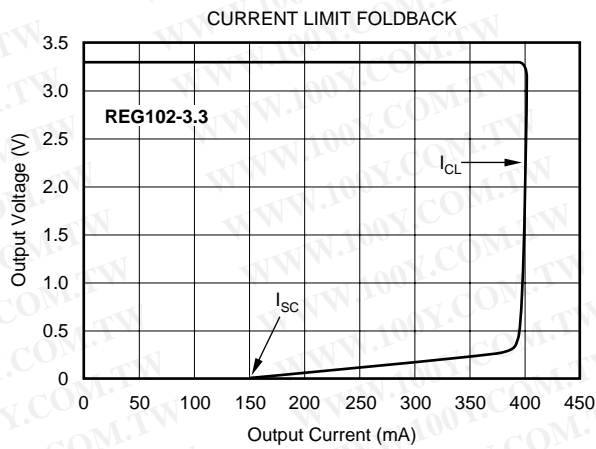
# TYPICAL CHARACTERISTICS (Cont.)

For all models, at  $T_J = +25^\circ\text{C}$  and  $V_{\text{ENABLE}} = 1.8\text{V}$ , unless otherwise noted.



# TYPICAL CHARACTERISTICS (Cont.)

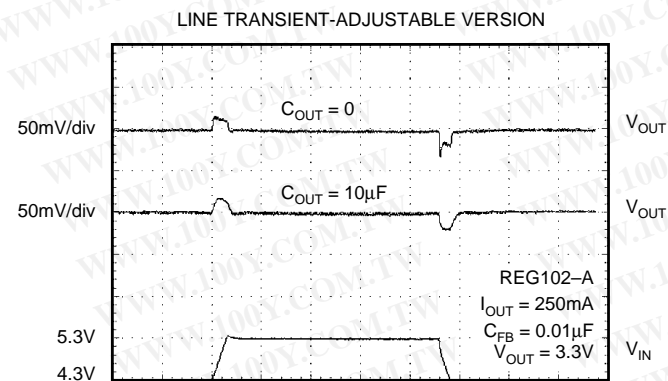
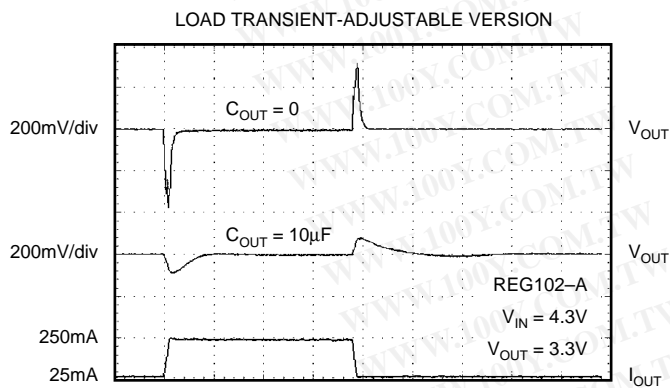
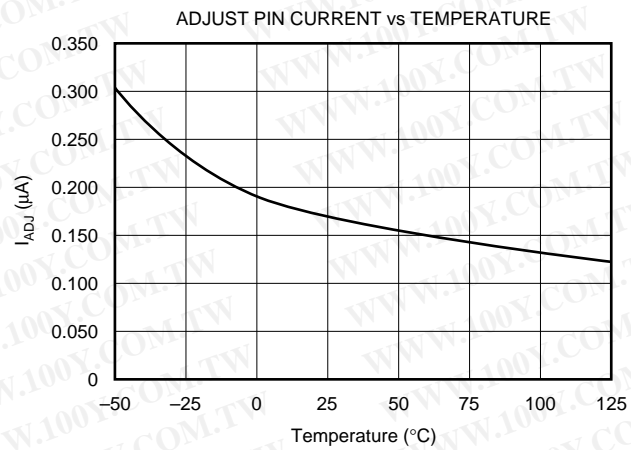
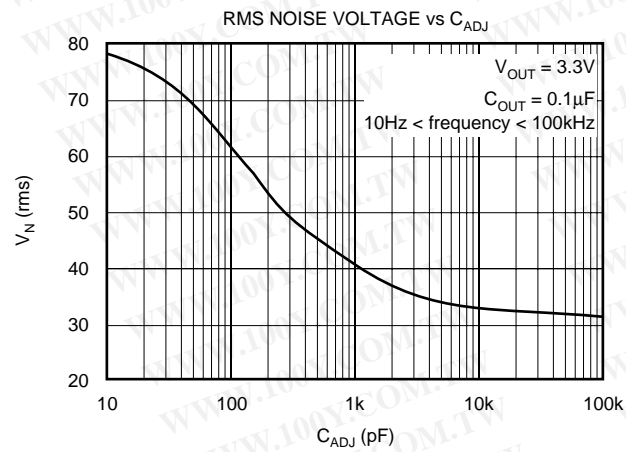
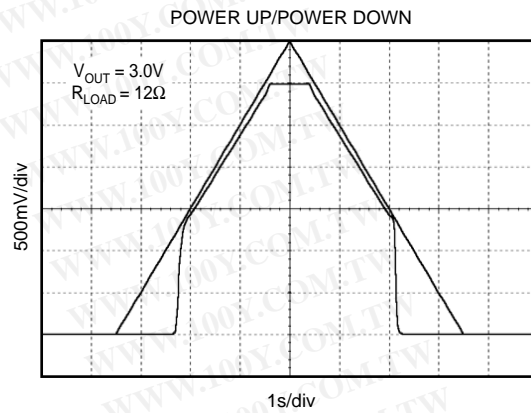
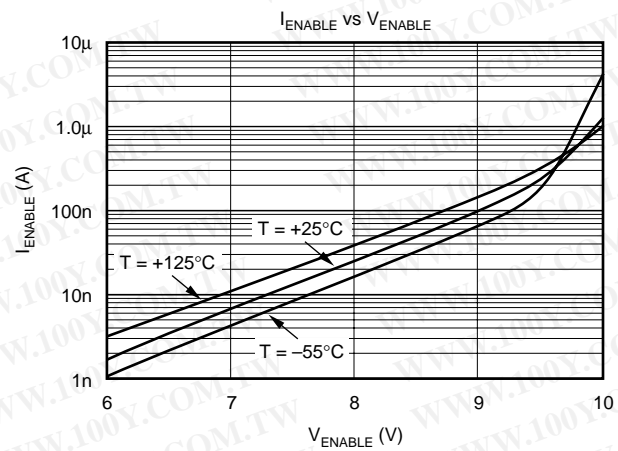
For all models, at  $T_J = +25^\circ\text{C}$  and  $V_{\text{ENABLE}} = 1.8\text{V}$ , unless otherwise noted.





# TYPICAL CHARACTERISTICS (Cont.)

For all models, at  $T_J = +25^\circ\text{C}$  and  $V_{\text{ENABLE}} = 1.8\text{V}$ , unless otherwise noted.





# BASIC OPERATION

The REG102 series of LDO (low dropout) linear regulators offers a wide selection of fixed output voltage versions and an adjustable output version as well. The REG102 belongs to a family of new generation LDO regulators that use a DMOS pass transistor to achieve ultra low-dropout performance and freedom from output capacitor constraints. Ground pin current remains under 1mA over all line, load, and temperature conditions. All versions have thermal and over-current protection, including foldback current limit.

The REG102 does not require an output capacitor for regulator stability and is stable over most output currents and with almost any value and type of output capacitor up to 10µF or more. For applications where the regulator output current drops below several milliamps, stability can be enhanced by adding a 1kΩ to 2kΩ load resistor, using capacitance values smaller than 10µF, or keeping the effective series resistance greater than 0.05Ω including the capacitor ESR and parasitic resistance in printed circuit board traces, solder joints, and sockets.

Although an input capacitor is not required, it is a good standard analog design practice to connect a 0.1µF low ESR capacitor across the input supply voltage. This is recommended to counteract reactive input sources and improve ripple rejection by reducing input voltage ripple.

Figure 1 shows the basic circuit connections for the fixed voltage models. Figure 2 gives the connections for the adjustable output version (REG102A) and example resistor values for some commonly used output voltages. Values for other voltages can be calculated from the equation shown in Figure 2.

## INTERNAL CURRENT LIMIT

The REG102 internal current limit has a typical value of 400mA. A foldback feature limits the short-circuit current to a typical short-circuit value of 150mA, which helps to protect

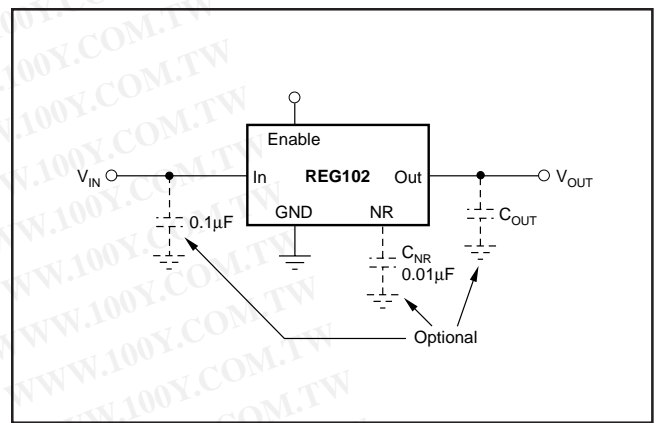


FIGURE 1. Fixed Voltage Nominal Circuit for the REG102.

the regulator from damage under all load conditions. A characteristic of  $V_{OUT}$  versus  $I_{OUT}$  is given in Figure 3 and in the Typical Characteristics section.

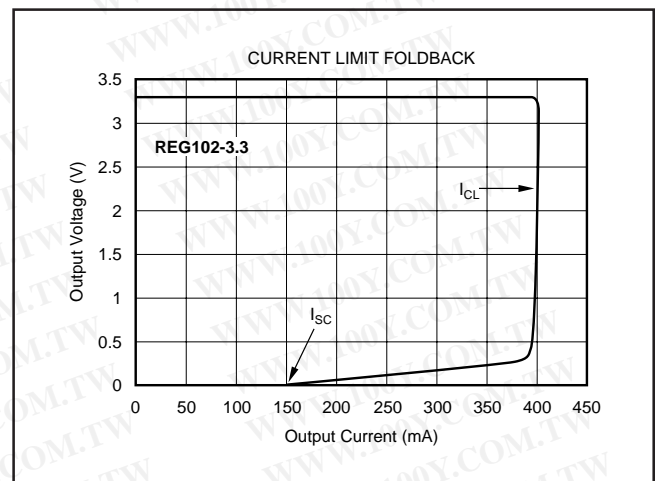


FIGURE 3. Foldback Current Limit of the REG102-3.3 at 25°C.

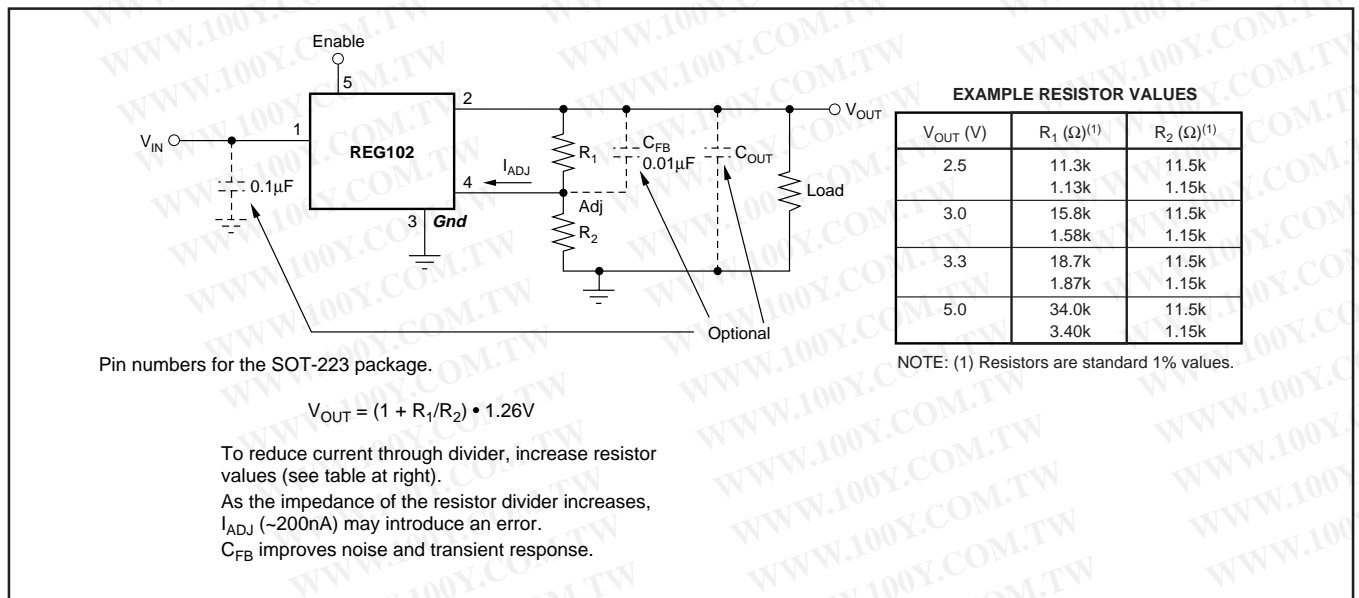


FIGURE 2. Adjustable Voltage Circuit for the REG102A.

## ENABLE

The Enable pin is active high and compatible with standard TTL-CMOS levels. Inputs below 0.5V (max) turn the regulator off and all circuitry is disabled. Under this condition, ground pin current drops to approximately 10nA. When not used, the Enable pin can be connected to  $V_{IN}$ . When a pull-up resistor is used, and operation below 1.8V is required, use pull-up resistor values below 50k $\Omega$ .

## OUTPUT NOISE

A precision bandgap reference is used to generate the internal reference voltage,  $V_{REF}$ . This reference is the dominant noise source within the REG102 and generates approximately 29 $\mu$ Vrms in the 10Hz to 100kHz bandwidth at the reference output. The regulator control loop gains up the reference noise, so that the noise voltage of the regulator is approximately given by:

$$V_N = 29\mu\text{Vrms} \frac{R_1 + R_2}{R_2} = 29\mu\text{Vrms} \cdot \frac{V_{OUT}}{V_{REF}} \quad (1)$$

As the value of  $V_{REF}$  is 1.26V, this relationship reduces to:

$$V_N = 23 \frac{\mu\text{Vrms}}{\text{V}} \cdot V_{OUT} \quad (2)$$

Connecting a capacitor,  $C_{NR}$ , from the Noise Reduction (NR) pin to ground forms a low-pass filter for the voltage reference. Adding  $C_{NR}$  (as shown in Figure 4) forms a low-pass filter for the voltage reference. For  $C_{NR} = 10\text{nF}$ , the total noise in the 10Hz to 100kHz bandwidth is reduced by approximately a factor of 2.8 for  $V_{OUT} = 3.3\text{V}$ . This noise reduction effect is shown in Figure 5 and as *RMS Noise Voltage vs  $C_{NR}$*  in the Typical Characteristics section.

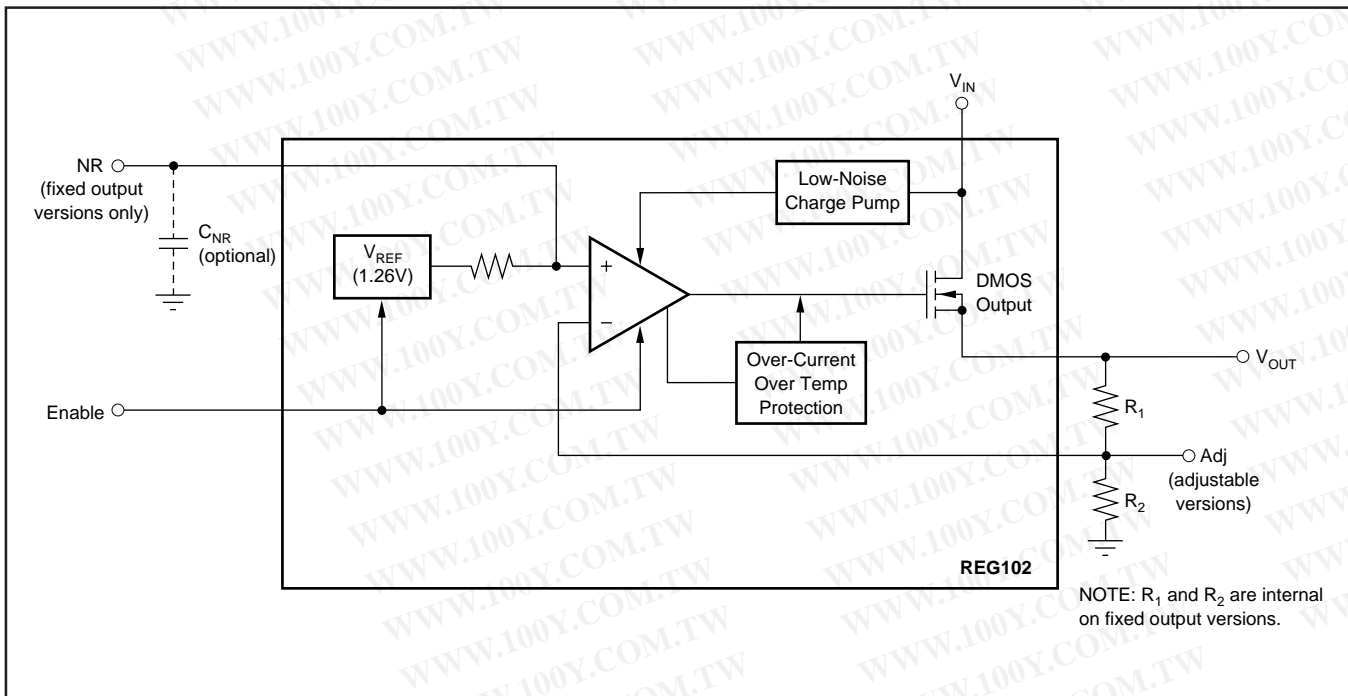


FIGURE 4. Block Diagram.

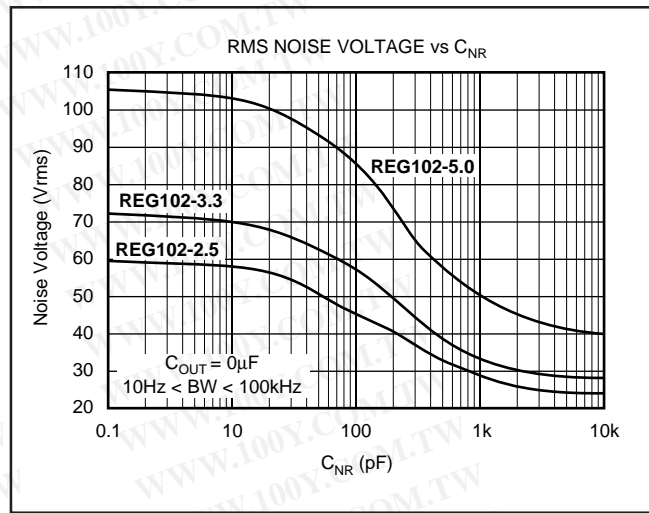


FIGURE 5. Output Noise versus Noise Reduction Capacitor.

Noise can be further reduced by carefully choosing an output capacitor,  $C_{OUT}$ . Best overall noise performance is achieved with very low ( $< 0.22\mu\text{F}$ ) or very high ( $> 2.2\mu\text{F}$ ) values of  $C_{OUT}$  (see the *RMS Noise Voltage vs  $C_{OUT}$*  typical characteristic).

The REG102 uses an internal charge pump to develop an internal supply voltage sufficient to drive the gate of the DMOS pass element above  $V_{IN}$ . The charge-pump switching noise (nominal switching frequency = 2MHz) is not measurable at the output of the regulator over most values of  $I_{OUT}$  and  $C_{OUT}$ .

The REG102 adjustable version does not have the noise-reduction pin available; however, the adjust pin is the summing junction of the error amplifier. A capacitor,  $C_{FB}$ , connected from the output to the adjust pin can reduce both the output noise and the peak error from a load transient (see the typical characteristics for output noise performance).

## DROPOUT VOLTAGE

The REG102 uses an N-channel DMOS as the pass element. When  $(V_{IN} - V_{OUT})$  is less than the drop-out voltage ( $V_{DROP}$ ), the DMOS pass device behaves like a resistor; therefore, for low values of  $(V_{IN} - V_{OUT})$ , the regulator input-to-output resistance is the  $R_{DS(ON)}$  of the DMOS pass element (typically  $600m\Omega$ ). For static (DC) loads, the REG102 typically maintains regulation down to a  $(V_{IN} - V_{OUT})$  voltage drop of 150mV at full rated output current. In Figure 6, the bottom line (DC dropout) shows the minimum  $V_{IN}$  to  $V_{OUT}$  voltage drop required to prevent dropout under DC load conditions.

For large step changes in load current, the REG102 requires a larger voltage drop across it to avoid degraded transient response. The boundary of this transient drop-out region is shown as the top line in Figure 6 and values of  $V_{IN}$  to  $V_{OUT}$  voltage drop above this line insure normal transient response.

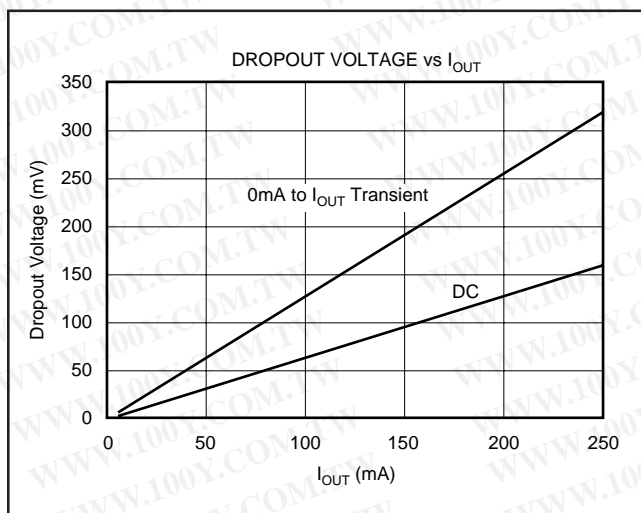


FIGURE 6. Transient and DC Dropout.

In the transient dropout region between DC and Transient, transient response recovery time increases. The time required to recover from a load transient is a function of both the magnitude and rate of the step change in load current and the available headroom  $V_{IN}$  to  $V_{OUT}$  voltage drop. Under worst-

case conditions (full-scale load change with  $(V_{IN} - V_{OUT})$  voltage drop close to DC dropout levels), the REG102 can take several hundred microseconds to re-enter the specified window of regulation.

## TRANSIENT RESPONSE

The REG102 response to transient line and load conditions improves at lower output voltages. The addition of a capacitor (nominal value  $0.47\mu F$ ) from the output pin to ground can improve the transient response. In the adjustable version, the addition of a capacitor,  $C_{FB}$  (nominal value  $10nF$ ), from the output to the adjust pin can also improve the transient response.

## THERMAL PROTECTION

Power dissipated within the REG102 can cause the junction temperature to rise. The REG102 has thermal shutdown circuitry that protects the regulator from damage which disables the output when the junction temperature reaches approximately  $160^{\circ}C$ , allowing the device to cool. When the junction temperature cools to approximately  $140^{\circ}C$ , the output circuitry is again enabled. Depending on various conditions, the thermal protection circuit can cycle on and off. This limits the dissipation of the regulator, but can have an undesirable effect on the load.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heat sink. For reliable operation, junction temperature must be limited to  $125^{\circ}C$ , maximum. To estimate the margin of safety in a complete design (including heat sink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger more than  $35^{\circ}C$  above the maximum expected ambient condition of the application. This produces a worst-case junction temperature of  $125^{\circ}C$  at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the REG102 is designed to protect against overload conditions and is not intended to replace proper heat sinking. Continuously running the REG102 into thermal shutdown will degrade reliability.



## POWER DISSIPATION

The REG102 is available in three different package configurations. The ability to remove heat from the die is different for each package type and, therefore, presents different considerations in the printed circuit board (PCB) layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Although it is difficult to impossible to quantify all of the variables in a thermal design of this type, performance data for several simplified configurations are shown in Figure 7. In all cases, the PCB copper area is bare copper (free of solder resist mask), not solder plated, and are for 1-ounce copper. Using heavier copper will increase the effectiveness in moving the heat from the device. In those examples where there is copper on both sides of the PCB, no connection has been provided between the two sides. The addition of plated through holes will improve the heat sink effectiveness.

Power dissipation depends on input voltage, load conditions, and duty cycle and is equal to the product of the average output current times the voltage across the output element,  $V_{IN}$  to  $V_{OUT}$  voltage drop.

$$P_D = (V_{IN} - V_{OUT}) \cdot I_{OUT} \quad (3)$$

Power dissipation can be minimized by using the lowest possible input voltage necessary to assure the required output voltage.

## REGULATOR MOUNTING

The tab of the SOT-223 package is electrically connected to ground. For best thermal performance, this tab must be soldered directly to a circuit-board copper area. Increasing the copper area improves heat dissipation, as shown in Figure 8.

Although the tab of the SOT-223 is electrical ground, it is not intended to carry current. The copper pad that acts as a heat sink should be isolated from the rest of the circuit to prevent current flow through the device from the tab to the ground pin. Solder pad footprint recommendations for the various REG102 devices are presented in Application Bulletin *Solder Pad Recommendations for Surface-Mount Devices* (SBFA015), available from the Texas Instruments web site ([www.ti.com](http://www.ti.com)).

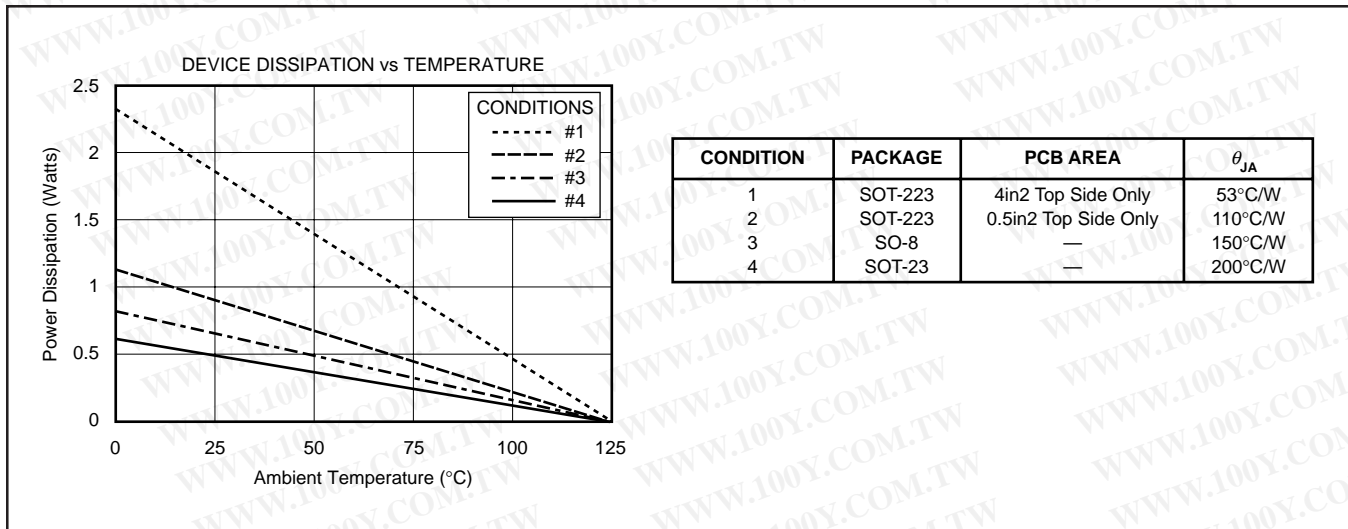


FIGURE 7. Maximum Power Dissipation versus Ambient Temperature for the Various Packages and PCB Heat Sink Configurations.

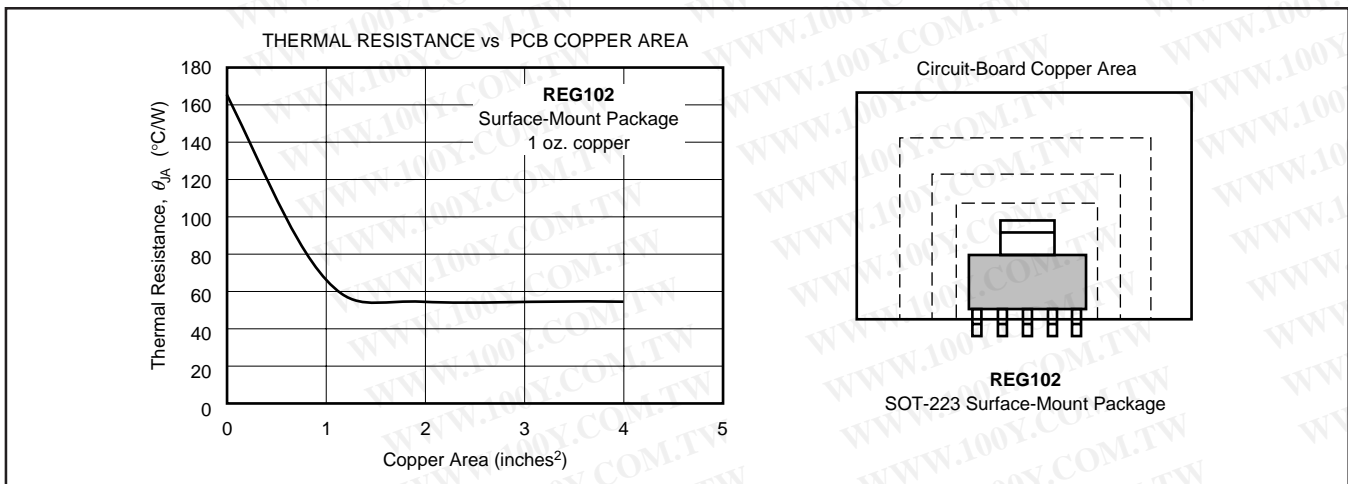


FIGURE 8. Thermal Resistance versus PCB Area for the Five-Lead SOT-223.



**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
REG102GA-2.5	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REG102GA-2.5/2K5	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REG102GA-2.5/2K5G4	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REG102GA-2.5G4	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REG102GA-2.8	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REG102GA-2.8/2K5	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REG102GA-2.8/2K5G4	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REG102GA-2.85	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REG102GA-2.85/2K5	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REG102GA-2.85G4	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REG102GA-2.8G4	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REG102GA-3	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REG102GA-3.3	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REG102GA-3.3/2K5	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REG102GA-3.3/2K5G4	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REG102GA-3.3G4	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REG102GA-3/2K5	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REG102GA-3/2K5G4	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REG102GA-3G4	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REG102GA-5	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REG102GA-5/2K5	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REG102GA-5/2K5G4	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REG102GA-5G4	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REG102GA-A	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REG102GA-A/2K5	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
REG102GA-A/2K5G4	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REG102GA-AG4	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REG102GA2.85/2K5G4	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REG102NA-2.5/250	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
REG102NA-2.5/250G4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
REG102NA-2.5/3K	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
REG102NA-2.5/3KG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
REG102NA-2.8/250	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
REG102NA-2.8/250G4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
REG102NA-2.8/3K	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
REG102NA-2.8/3KG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
REG102NA-2.85/250	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
REG102NA-2.85/3K	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
REG102NA-2.85/3KG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
REG102NA-285/250G4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
REG102NA-3.3/250	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
REG102NA-3.3/250G4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
REG102NA-3.3/3K	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
REG102NA-3.3/3KG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
REG102NA-3/250	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
REG102NA-3/250G4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
REG102NA-3/3K	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
REG102NA-3/3KG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
REG102NA-5/250	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
REG102NA-5/250G4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
REG102NA-5/3K	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
REG102NA-5/3KG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
REG102NA-A/250	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
REG102NA-A/250G4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
REG102NA-A/3K	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
REG102NA-A/3KG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
REG102UA-2.5	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REG102UA-2.5/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REG102UA-2.5/2K5G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REG102UA-2.5G4	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REG102UA-2.8	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REG102UA-2.8/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REG102UA-2.8/2K5G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REG102UA-2.85	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REG102UA-2.85/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REG102UA-2.85G4	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REG102UA-2.8G4	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REG102UA-3	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REG102UA-3.3	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REG102UA-3.3/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REG102UA-3.3/2K5G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REG102UA-3.3G4	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REG102UA-3/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REG102UA-3/2K5G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REG102UA-3G4	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REG102UA-5	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REG102UA-5/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR



Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
REG102UA-5/2K5G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REG102UA-5G4	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REG102UA-A	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REG102UA-A/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REG102UA-A/2K5G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REG102UA-AG4	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REG102UA2.85/2K5G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

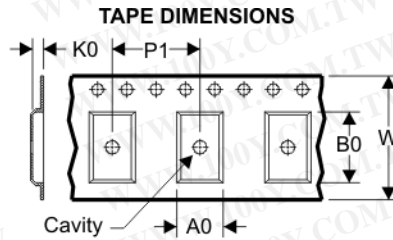
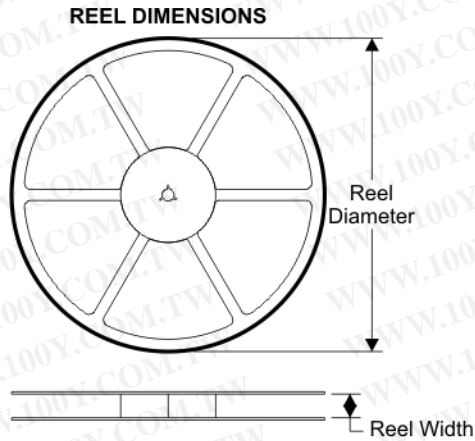
<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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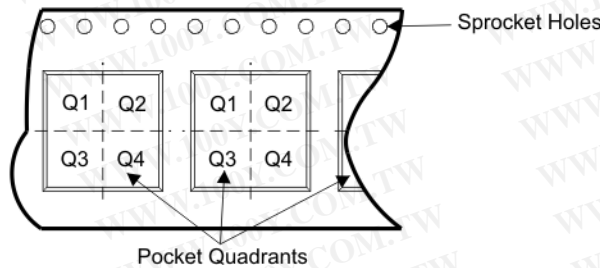


**TAPE AND REEL BOX INFORMATION**



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

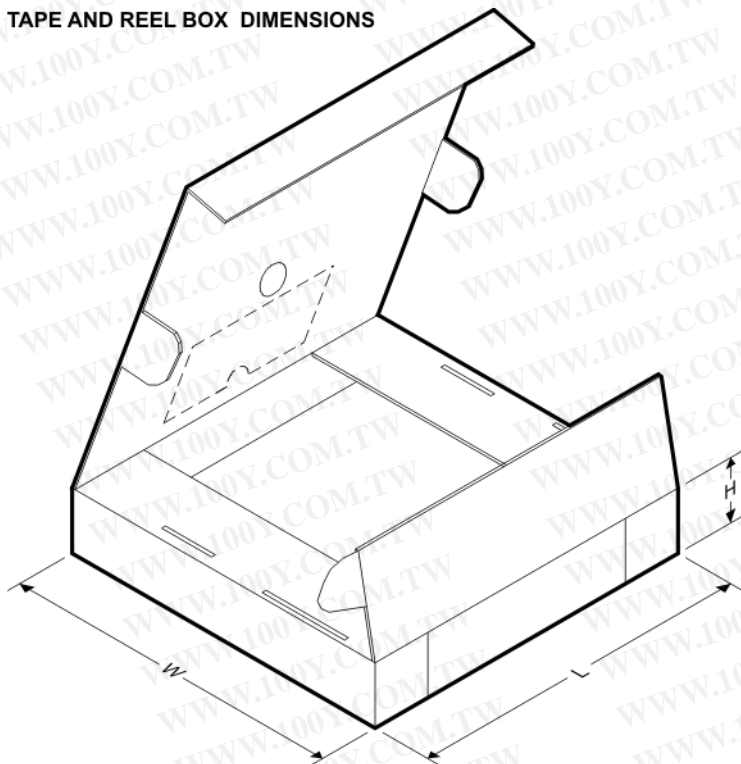
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
REG102GA-2.5/2K5	DCQ	6	SITE 67	330	12	6.83	7.42	1.88	8	12	Q3
REG102GA-2.8/2K5	DCQ	6	SITE 67	330	12	6.83	7.42	1.88	8	12	Q3
REG102GA-2.85/2K5	DCQ	6	SITE 67	330	12	6.83	7.42	1.88	8	12	Q3
REG102GA-3.3/2K5	DCQ	6	SITE 67	330	12	6.83	7.42	1.88	8	12	Q3
REG102GA-3/2K5	DCQ	6	SITE 67	330	12	6.83	7.42	1.88	8	12	Q3
REG102GA-5/2K5	DCQ	6	SITE 67	330	12	6.83	7.42	1.88	8	12	Q3
REG102GA-A/2K5	DCQ	6	SITE 67	330	12	6.83	7.42	1.88	8	12	Q3
REG102NA-2.5/250	DBV	5	SITE 48	179	8	3.2	3.2	1.4	4	8	Q3
REG102NA-2.5/3K	DBV	5	SITE 48	179	8	3.2	3.2	1.4	4	8	Q3
REG102NA-2.8/250	DBV	5	SITE 48	179	8	3.2	3.2	1.4	4	8	Q3
REG102NA-2.8/3K	DBV	5	SITE 48	179	8	3.2	3.2	1.4	4	8	Q3
REG102NA-2.85/250	DBV	5	SITE 48	179	8	3.2	3.2	1.4	4	8	Q3
REG102NA-2.85/3K	DBV	5	SITE 48	179	8	3.2	3.2	1.4	4	8	Q3
REG102NA-3.3/250	DBV	5	SITE 48	179	8	3.2	3.2	1.4	4	8	Q3
REG102NA-3.3/3K	DBV	5	SITE 48	179	8	3.2	3.2	1.4	4	8	Q3
REG102NA-3/250	DBV	5	SITE 48	179	8	3.2	3.2	1.4	4	8	Q3
REG102NA-3/3K	DBV	5	SITE 48	179	8	3.2	3.2	1.4	4	8	Q3
REG102NA-5/250	DBV	5	SITE 48	179	8	3.2	3.2	1.4	4	8	Q3
REG102NA-5/3K	DBV	5	SITE 48	179	8	3.2	3.2	1.4	4	8	Q3

Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
REG102NA-A/250	DBV	5	SITE 48	179	8	3.2	3.2	1.4	4	8	Q3
REG102NA-A/3K	DBV	5	SITE 48	179	8	3.2	3.2	1.4	4	8	Q3
REG102UA-2.5/2K5	D	8	SITE 41	330	12	6.9	5.4	2.0	8	12	Q1
REG102UA-2.8/2K5	D	8	SITE 41	330	12	6.9	5.4	2.0	8	12	Q1
REG102UA-2.85/2K5	D	8	SITE 41	330	12	6.9	5.4	2.0	8	12	Q1
REG102UA-3.3/2K5	D	8	SITE 41	330	12	6.9	5.4	2.0	8	12	Q1
REG102UA-3/2K5	D	8	SITE 41	330	12	6.9	5.4	2.0	8	12	Q1
REG102UA-5/2K5	D	8	SITE 41	330	12	6.9	5.4	2.0	8	12	Q1
REG102UA-A/2K5	D	8	SITE 41	330	12	6.9	5.4	2.0	8	12	Q1

**TAPE AND REEL BOX DIMENSIONS**

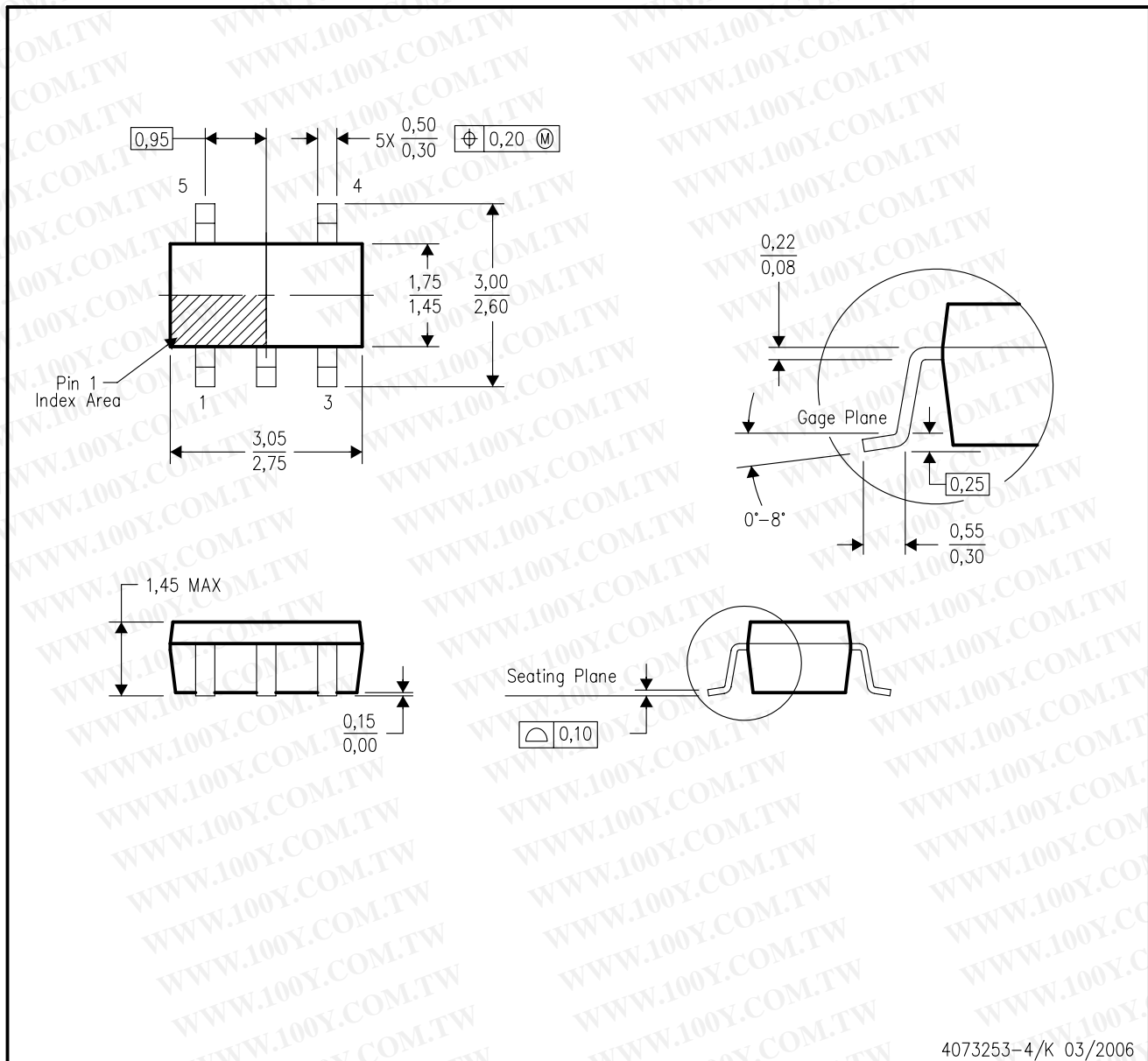


Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
REG102GA-2.5/2K5	DCQ	6	SITE 67	375.0	340.0	57.0
REG102GA-2.8/2K5	DCQ	6	SITE 67	375.0	340.0	57.0
REG102GA-2.85/2K5	DCQ	6	SITE 67	375.0	340.0	57.0
REG102GA-3.3/2K5	DCQ	6	SITE 67	375.0	340.0	57.0
REG102GA-3/2K5	DCQ	6	SITE 67	375.0	340.0	57.0
REG102GA-5/2K5	DCQ	6	SITE 67	375.0	340.0	57.0
REG102GA-A/2K5	DCQ	6	SITE 67	375.0	340.0	57.0
REG102NA-2.5/250	DBV	5	SITE 48	195.0	200.0	45.0

Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
REG102NA-2.5/3K	DBV	5	SITE 48	195.0	200.0	45.0
REG102NA-2.8/250	DBV	5	SITE 48	195.0	200.0	45.0
REG102NA-2.8/3K	DBV	5	SITE 48	195.0	200.0	45.0
REG102NA-2.85/250	DBV	5	SITE 48	195.0	200.0	45.0
REG102NA-2.85/3K	DBV	5	SITE 48	195.0	200.0	45.0
REG102NA-3.3/250	DBV	5	SITE 48	195.0	200.0	45.0
REG102NA-3.3/3K	DBV	5	SITE 48	195.0	200.0	45.0
REG102NA-3/250	DBV	5	SITE 48	195.0	200.0	45.0
REG102NA-3/3K	DBV	5	SITE 48	195.0	200.0	45.0
REG102NA-5/250	DBV	5	SITE 48	195.0	200.0	45.0
REG102NA-5/3K	DBV	5	SITE 48	195.0	200.0	45.0
REG102NA-A/250	DBV	5	SITE 48	195.0	200.0	45.0
REG102NA-A/3K	DBV	5	SITE 48	195.0	200.0	45.0
REG102UA-2.5/2K5	D	8	SITE 41	346.0	346.0	29.0
REG102UA-2.8/2K5	D	8	SITE 41	346.0	346.0	29.0
REG102UA-2.85/2K5	D	8	SITE 41	346.0	346.0	29.0
REG102UA-3.3/2K5	D	8	SITE 41	346.0	346.0	29.0
REG102UA-3/2K5	D	8	SITE 41	346.0	346.0	29.0
REG102UA-5/2K5	D	8	SITE 41	346.0	346.0	29.0
REG102UA-A/2K5	D	8	SITE 41	346.0	346.0	29.0

DBV (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE

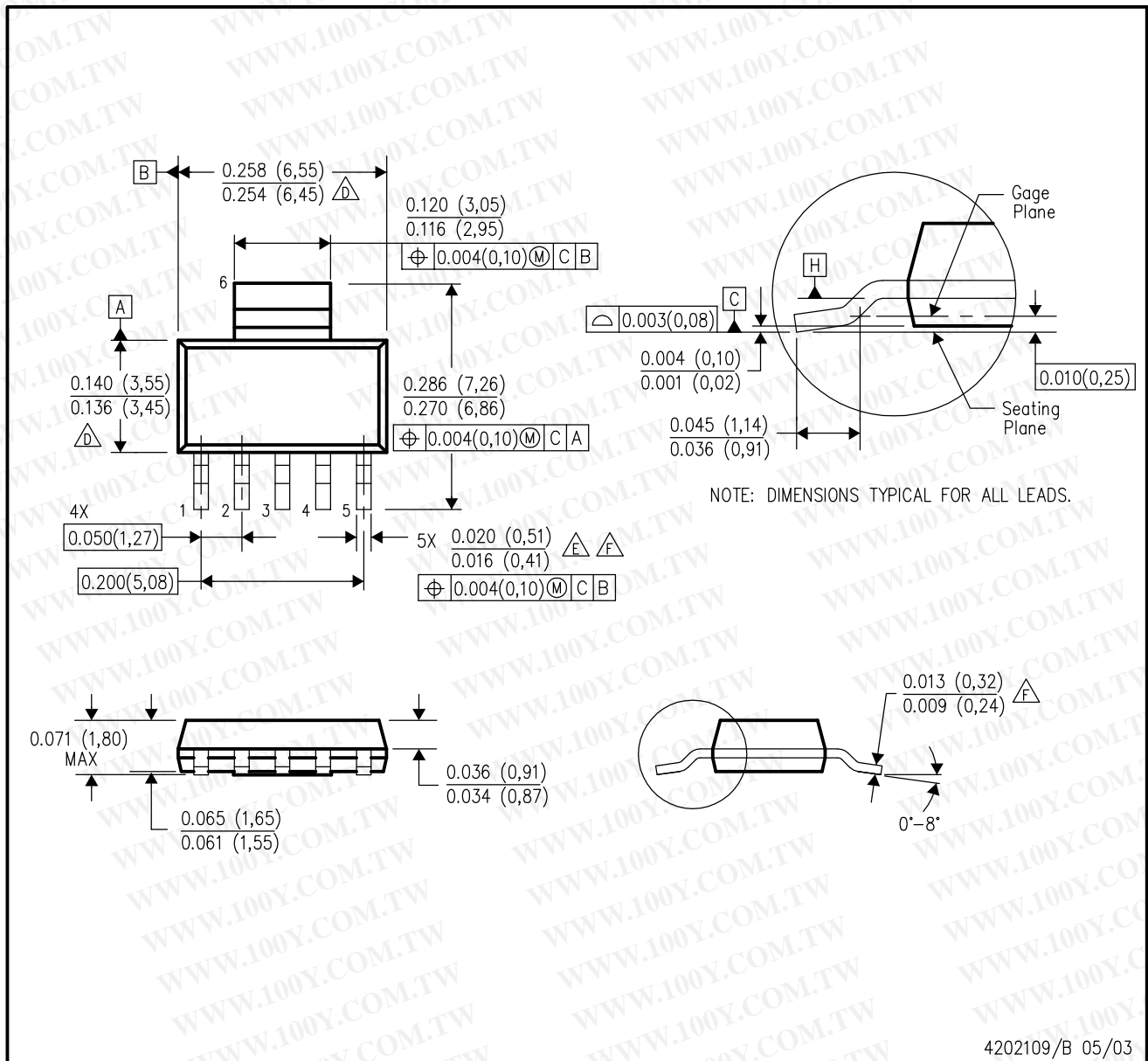


- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
  - Falls within JEDEC MO-178 Variation AA.



DCQ (R-PDSO-G6)

PLASTIC SMALL-OUTLINE

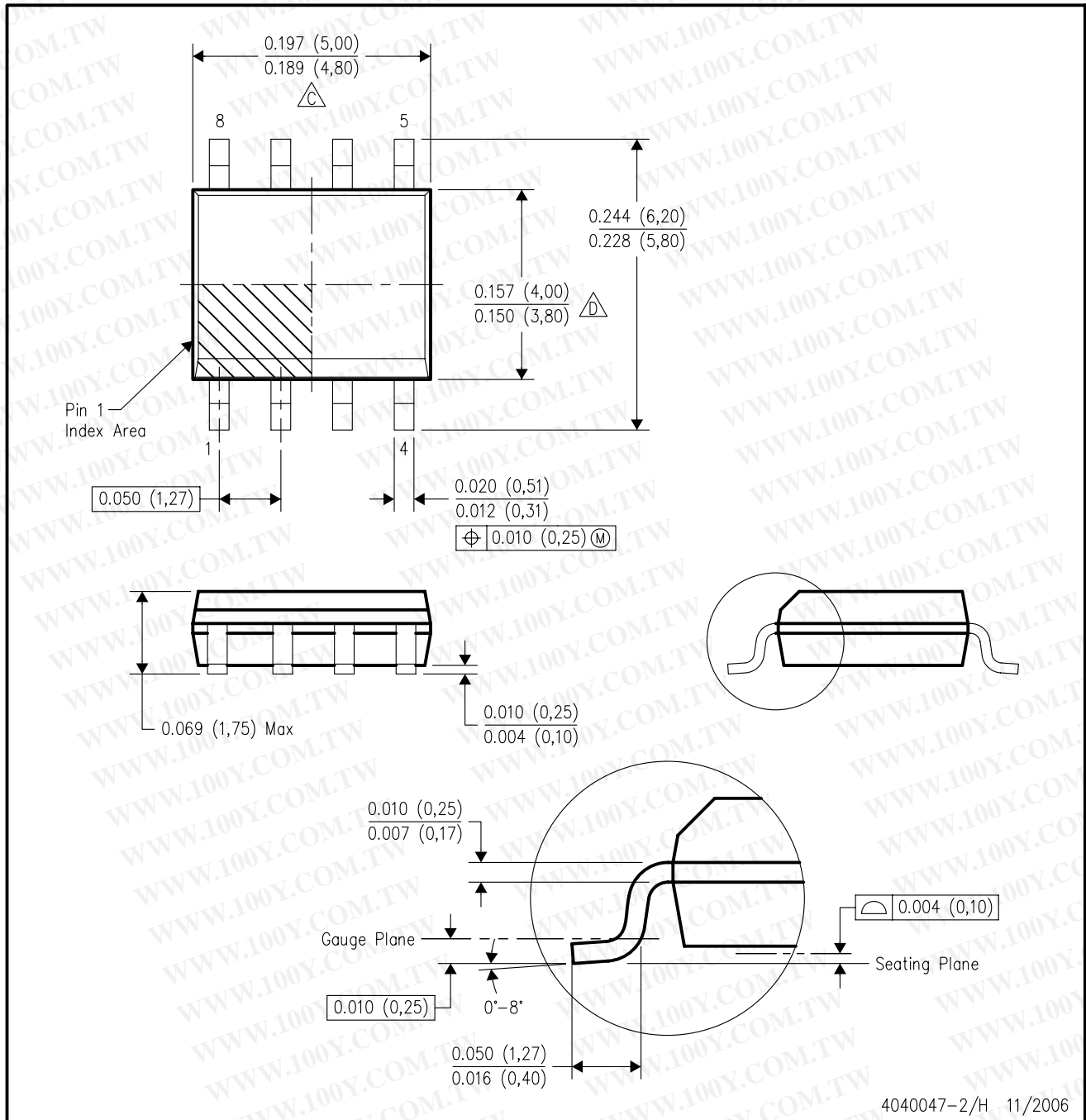


- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Controlling dimension in inches.
  - Body length and width dimensions are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and interlead flash, but including any mismatch between the top and the bottom of the plastic body.
  - Lead width dimension does not include dambar protrusion.

- Lead width and thickness dimensions apply to solder plated leads.
- G. Interlead flash allow 0.008 inch max.
- H. Gate burr/protrusion max. 0.006 inch.
- I. Datums A and B are to be determined at Datum H.
- J. Package dimensions per JEDEC outline drawing T0-261, issue B, dated Feb. 1999. This variation is not yet included.

D (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



4040047-2/H 11/2006

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
  - $\triangle D$  Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
  - E. Reference JEDEC MS-012 variation AA.

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