SN75C1167, SN65C1168, SN75C1168 DUAL DIFFERENTIAL DRIVERS AND RECEIVERS

SLLS159D - MARCH 1993 - REVISED AUGUST 2002

- Meet or Exceed Standards TIA/EIA-422-B and ITU Recommendation V.11
- BiCMOS Process Technology
- Low Supply-Current Requirements:
 9 mA Max
- Low Pulse Skew
- Receiver Input Impedance . . . 17 kΩ Typ
- Receiver Input Sensitivity . . . ±200 mV
- Receiver Common-Mode Input Voltage Range of -7 V to 7 V
- Operate From Single 5-V Power Supply
- Glitch-Free Power-Up/Power-Down Protection
- Receiver 3-State Outputs Active-Low Enable for SN75C1167 Only
- Improved Replacements for the MC34050 and MC34051

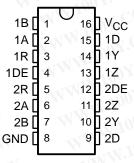
description/ordering information

The SN75C1167, SN65C1168, and SN75C1168 dual drivers and receivers are integrated circuits designed for balanced transmission lines. The devices meet TIA/EIA-422-B and ITU recommendation V.11.

SN75C1167 . . . DB, N, OR NS PACKAGE (TOP VIEW)



SN65C1168 . . . N, NS, OR PW PACKAGE SN75C1168 . . . DB, N, NS, OR PW PACKAGE (TOP VIEW)



The SN75C1167 combines dual 3-state differential line drivers and 3-state differential line receivers, both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, which can be connected together externally to function as direction control. The SN65C1168 and SN75C1168 drivers have individual active-high enables.

ORDERING INFORMATION

TA	PACK	AGE [†]	ORDERABLE PART NUMBER	TOP-SIDE MARKING
M.	PDIP (N)	Tube	SN75C1167N	SN75C1167N
	SOP (NS)	Tape and reel	SN75C1167NSR	75C1167
	SSOP (DB)	Tape and reel	SN75C1167DBR	CA1167
0°C to 70°C	PDIP (N)	Tube	SN75C1168N	SN75C1168N
	SOP (NS)	Tape and reel	SN75C1168NSR	75C1168
	SSOP (DB)	Tape and reel	SN75C1168DBR	CA1168
	TSSOP (PW)	Tape and reel	SN75C1168PWR	CA1168
	PDIP (N)	Tube	SN65C1168N	SN65C1168N
–40°C to 85°C	SOP (NS)	Tape and reel	SN65C1168NSR	65C1168
	TSSOP (PW)	Tape and reel	SN65C1168PWR	CB1168

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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Function Tables

EACH DRIVER

	INPUT	ENABLE	OUTPUTS			
	D	DE	Υ	Z		
	Н	COH	ΝН	L		
l.	L.10	Н	Ļ	н		
	X	O. FOW.	Z	Z		

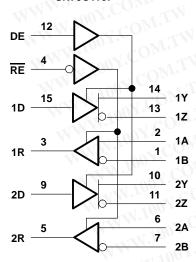
SN75C1167, EACH RECEIVER

N	X	L L	L Z	H Z	
D	SN/5C1 DIFFERENTIAL A – B	INPUTS	ENABLI RE		UT
	V _{ID} ≥ 0.2	V V.C	PLA	Н	
	-0.2 V < V _{ID} <	< 0.2 V	CONT.	?	
	V _{ID} ≤ -0.2	2 V 1003	COM	L	
	X		Н	Z	
	Open		A.CL.	TYH	

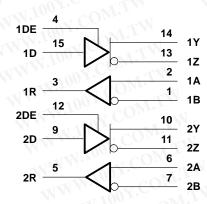
= high level, L = low level, indeterminate, X = irrelevant, Z = high impedance (off)

logic diagram (positive logic)

SN75C1167



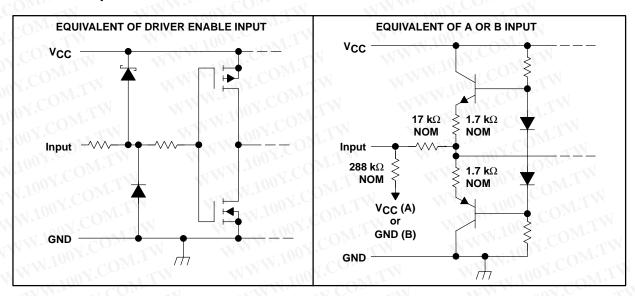
SN65C1168, SN75C1168



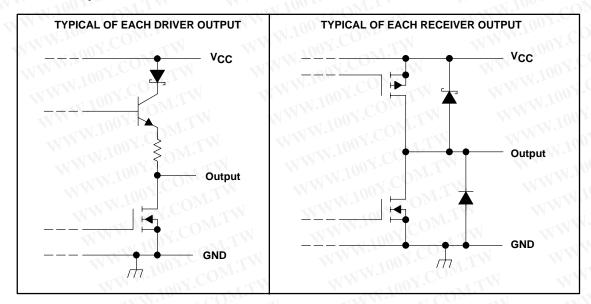
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schematics of inputs



schematics of outputs



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC} (see Note 1)		–0.5 V to 7 V
Input voltage range, V ₁		
Input voltage range, V _I (A or B, Receiver)		
Differential input voltage range, VID, Receiver (see No		
Output voltage range, V _O , Driver		
Clamp current range, I _{IK} or I _{OK} , Driver		
Output current range, I _O , Driver	Marian - Mar	±150 mA
Supply current, I _{CC}	20 p. j	200 mA
GND current		
Output current range, I _O , Receiver		±25 mA
Operating virtual junction temperature		150°C
Package thermal impedance, θ_{JA} (see Notes 3 and 4):	: DB package	82°C/W
	N package	67°C/W
	NS package	64°C/W
	PW package	
Storage temperature range, T _{stq}	oM:::	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10	seconds	260°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values except differential input voltage are with respect to the network GND.
 - 2. Differential input voltage is measured at the noninverting terminal with respect to the inverting terminal.
 - Maximum power dissipation is a function of T_J(max), θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is P_D = (T_J(max) T_A)/θ_{JA}. Selecting the maximum of 150°C can affect reliability.
 - 4. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

	1100	M.TV	M.1001.	MIN	NOM	MAX	UNIT
Vcc	Supply voltage	I.Co. IN W	W. 100Y. COM. T	4.5	5	5.5	V
VIC	Common-mode input voltage (see Note 5)	Receiver	AMM. TOOX. COM.	W	1	±7	N.VOO
VID	Differential input voltage	Receiver	WW. 1007.0M	IM		±7	VIO
۷ıн	High-level input voltage	Except A, B	MM TOWN.CO.	2		M	V
V_{IL}	Low-level input voltage	Except A, B	M.M. COL	TV.	N .	0.8	V
1	High lavel autout august	Receiver			W.		
ЮН	High-level output current	Driver			//	-20	mA
	WW	Receiver		WTI		6	MAN.
IOL Low-level output current		Driver		Ohr	TW	20	mA
<u> </u>	On another form a sintense and the	M.1001.	SN75C1167, SN75C1168	00	. 1	70	-00
TA	Operating free-air temperature		SN65C1168	-40	1.1.11	85	°C

NOTE 5: Refer to TIA/EIA-422-B for exact conditions.



DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

001.	PARAMETER		TEST CONDITIONS			TYP†	MAX	UNIT
VIK	Input clamp voltage	$I_{I} = -18 \text{ mA}$		W 1001		I'I A	-1.5	V
VoH	High-level output voltage	V _{IH} = 2 V,	$V_{IL} = 0.8 V$,	$I_{OH} = -20 \text{ mA}$	2.4	3.4		V
VOL	Low-level output voltage	V _{IH} = 2 V,	$V_{IL} = 0.8 V$,	I _{OL} = 20 mA	N.CU	0.2	0.4	V
VOD1	Differential output voltage	$I_O = 0 \text{ mA}$	1.1	TANN TO	2	0_{Mr}	6	V
VOD2	Differential output voltage	1001.	MIII	W.11	2	3.1	1	V
Δ V _{OD}	Change in magnitude of differential output voltage	$R_L = 100 \Omega$, See Figure 1 and Note 5		001.	COM	±0.4	V	
Voc	Common-mode output voltage			100.	- c01	±3	V	
Δ V _{OC}	Change in magnitude of common-mode output voltage	W.100X.COM.TW WWY			N.100	V.CC	±0.4	V
Al Al		100	V _O = 6 V	-1	M.In.	-1 C	100	μΑ
O(OFF)	Output current with power off (see Note 3)	ACC = 0 A	$V_0 = -0.25 \text{ V}$	4	-1XX 1	00 2.	-100	μΑ
3N V	The second Court of Manager of Ma	V _O = 2.5 V	Y.Co.	M M	1	1007.	20	TW
loz	High-impedance-state output current	V _O = 5 V	COM	TV V	MM.	· nov	-20	μΑ
liH	High-level input current	$V_I = V_{CC}$ or	VIH.		at VIV	Too	< 0	μΑ
I _{IL}	Low-level input current	V _I = GND o	r V _{IL}	1.7.4		0.100	-1	μΑ
los	Short-circuit output current	$V_{O} = V_{CC} \circ$	r GND,	See Note 6	-30	` sī 10	-150	mA
loo	Supply current (total package)	No load,	$V_I = V_{CC}$ or Q	GND	WV	4	6	m A 4
ICC	Supply current (total package)	Enabled $V_I = 2.4 \text{ or } 0.5 \text{ V}$, See Note 7		V, See Note 7	1	5	9	mA
C _i	Input capacitance		1007.	OMIT	14	6	100 -	pF

† All typical values are at $V_{CC} = 5 \text{ V}$ and $T_A = 25^{\circ}\text{C}$. NOTES: 5. Refer to TIA/EIA-422-B for exact conditions.

- 6. Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
- 7. This parameter is measured per input, while the other inputs are at V_{CC} or GND.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	PARAMETER	TEST CONDIT	MIN	TYP [†]	MAX	UNIT	
tPHL	Propagation delay time, high- to low-level output	$R_1 = R_2 = 50 \Omega$	$R_3 = 500 \Omega$		7	12	ns
^t PLH	Propagation delay time, low- to high-level output	$C_1 = C_2 = C_3 = 40 \text{ pF},$	S1 is open,	IM	7	12	ns
tsk(p)	Pulse skew	See Figure 2	100 Y. COL	WT	0.5	4	ns
t _r	Rise time	$R_1 = R_2 = 50 \Omega$	$R_3 = 500 \Omega$	VTT	5	10	ns
tf	Fall time	tiput $C_1 = K_2 = 0.3 = 40 \text{ pF}$, $C_1 = C_2 = C_3 = 40 \text{ pF}$, $C_1 = C_2 = C_3 = 40 \text{ pF}$, $C_1 = C_2 = C_3 = 40 \text{ pF}$, $C_1 = C_2 = C_3 = 40 \text{ pF}$, $C_1 = C_2 = C_3 = 40 \text{ pF}$, $C_1 = C_2 = C_3 = 40 \text{ pF}$, $C_1 = C_2 = C_3 = 40 \text{ pF}$, $C_1 = C_2 = C_3 = 40 \text{ pF}$, $C_1 = C_2 = C_3 = 40 \text{ pF}$, $C_1 = C_2 = C_3 = 40 \text{ pF}$, $C_1 = C_2 = C_3 = 40 \text{ pF}$, $C_1 = C_2 = C_3 = 40 \text{ pF}$, $C_1 = C_2 = C_3 = 40 \text{ pF}$, $C_1 = C_2 = C_3 = 40 \text{ pF}$, $C_1 = C_2 = C_3 = 40 \text{ pF}$, $C_1 = C_2 = C_3 = 40 \text{ pF}$, $C_1 = C_2 = C_3 = 40 \text{ pF}$, $C_1 = C_2 = C_3 = 40 \text{ pF}$, $C_2 = C_3 = 40 \text{ pF}$, $C_3 = C_3 = C_$	S1 is open,	MI.	5	10	ns
^t PZH	Output enable time to high level		$R_3 = 500 \Omega$	\mathcal{I}_{Mr}	10	19	ns
tPZL	Output enable time to low level		S1 is closed,		10	19	ns
^t PHZ	Output disable time from low level		$R_3 = 500 \Omega$, S1 is closed,		7	16	ns
tPLZ	Output disable time from high level	See Figure 4	ST IS CIOSEU,		7	16	ns

 $[\]dagger$ All typical values are at V_{CC} = 5 V and T_A = 25°C.



RECEIVER SECTION

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

vi 10	PARAMETER	TEST CONDITIONS		MIN	TYP [†]	MAX	UNIT	
V _{IT+}	Positive-going input threshold voltage, differential input		DOX.COM.TV	N WWW.1	00.X.C	OM.	0.2	V
VIT-	Negative-going input threshold differential input	voltage,	Too COM	100X.COM.ITW WWW.		CO_{M_2}	V.T.V	V
V _{hys}	Input hysteresis (V _{IT+} – V _{IT-})	WW	M. CO.	TW WWW	- 100	60	TI	mV
VIK	Input clamp voltage, RE	SN75C1167	I _I = -18 mA	Www.W	W. 2	V.CC	-1.5	V
Vон	High-level output voltage		V _{ID} = 200 mV,	I _{OH} = -6 mA	3.8	4.2	O_{Mr}	V
VOL	Low-level output voltage	W.	$V_{ID} = -200 \text{ mV},$	I _{OL} = 6 mA	-TN 1	0.1	0.3	V
loz	High-impedance-state output current	SN75C1167	$V_O = V_{CC}$ or GND	OM.TW W		±0.5	±5	μА
	MM. 1001.	11	Others Salvet at O.V.	V _I = 10 V	- 111	100	1.5 -2.5	M.r.
†į	Line input current		Other input at 0 V	V _I = -10 V	MAL	×1 100		mA
lį	Enable input current, RE	SN75C1167	V _I = V _{CC} or GND	COM	WW	44.	±1	μА
rį	Input resistance	1.1	$V_{IC} = -7 V \text{ to } 7 V,$	Other input at 0 V	4	17		kΩ
	Supply current (total package)		100	V _I = V _{CC} or GND		4	6	CON
ICC			No load, Enabled	V _{IH} = 2.4 V or 0.5 V, See Note 5	N	5	9	mA

[†] All typical values are at $V_{CC} = 5 \text{ V}$ and $T_A = 25^{\circ}\text{C}$.

NOTE 5: Refer to TIA/EIA-422-B for exact conditions.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 8)

	PARAMETER	TEST CONDITIONS	MIN	TYP [†]	MAX	UNIT
tPLH	Propagation delay time, low- to high-level output	Coa Figuro E		17	27	ns
tPHL	Propagation delay time, high- to low-level output	See Figure 5)	17	27	ns
^t TLH	Transition time, low- to high-level output	Via OV See Figure	$G_{I,I,I}$	4	9	ns
tTHL	Transition time, high- to low-level output	VIC = 0 v, See Figure	3	4	9	ns
^t PZH	Output enable time to high level	WWW.	Colp.	13	22	ns
tPZL	Output enable time to low level	D. 4 kW. Soo Figure	C_{OM}	13	22	ns
t _{PHZ}	Output disable time from high level	See Figure 5 VIC = 0 V, See Figure 5 RL = 1 kW, See Figure 6	MON	13	22	ns
tPLZ	Output disable time from low level		Y.	13	22	ns

[†] All typical values are at $V_{CC} = 5 \text{ V}$ and $T_A = 25^{\circ}\text{C}$.

NOTE 8: Measured per input while the other inputs are at $V_{\hbox{CC}}$ or GND



[‡] The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.

PARAMETER MEASUREMENT INFORMATION

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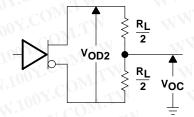
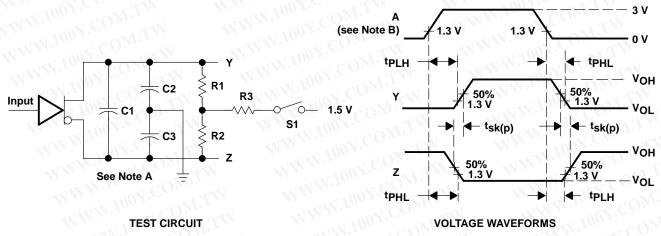


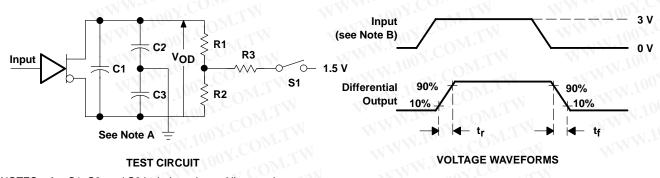
Figure 1. Driver Test Circuit, VOD and VOC



NOTES: A. C1, C2, and C3 include probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_r = t_f \le 6$ ns

Figure 2. Driver Test Circuit and Voltage Waveforms

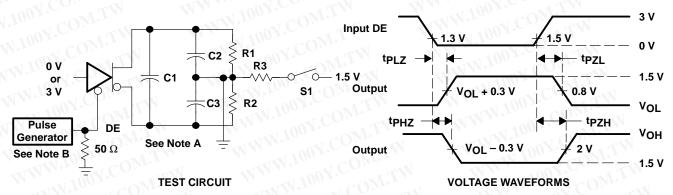


NOTES: A. C1, C2, and C3 include probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_{\Gamma} = t_{\tilde{f}} \le 6$ ns.

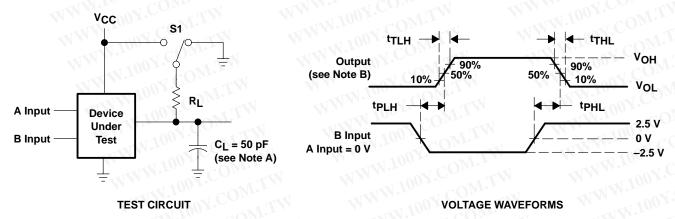
Figure 3. Driver Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C1, C2, and C3 include probe and jig capacitance.
 - B. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_f = t_f \le 6$ ns.

Figure 4. Driver Test Circuit and Voltage Waveforms



NOTES: A. C_L includes probe and jig capacitance.

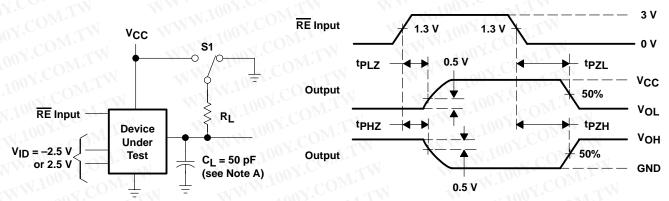
B. The pulse generator has the following characteristics: PRR \leq 1 MHz, duty cycle = 50%, t_Γ = $t_f \leq$ 6 ns.

Figure 5. Receiver Test Circuit and Voltage Waveforms

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PARAMETER MEASUREMENT INFORMATION



 t_{PZL}, t_{PLZ} Measurement: S1 to V_{CC} t_{PZH}, t_{PHZ} Measurement: S1 to GND

TEST CIRCUIT

VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.

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B. The pulse generator has the following characteristics: PRR \leq 1 MHz, duty cycle = 50%, t_Γ = $t_f \leq$ 6 ns.

Figure 6. Receiver Test Circuit and Voltage Waveforms

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Mailing Address:

Texas Instruments Post Office Box 655303 Dallas, Texas 75265