

SN54LS373, SN54LS374, SN54S373, SN54S374, SN74LS373, SN74LS374, SN74S373, SN74S374

OCTAL D-TYPE TRANSPARENT LATCHES AND EDGE-TRIGGERED FLIP-FLOPS

SDLS165B – OCTOBER 1975 – REVISED AUGUST 2002

- Choice of Eight Latches or Eight D-Type Flip-Flops in a Single Package
- 3-State Bus-Driving Outputs
- Full Parallel Access for Loading
- Buffered Control Inputs
- Clock-Enable Input Has Hysteresis to Improve Noise Rejection ('S373 and 'S374)
- P-N-P Inputs Reduce DC Loading on Data Lines ('S373 and 'S374)

description

These 8-bit registers feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. The high-impedance 3-state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pullup components. These devices are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

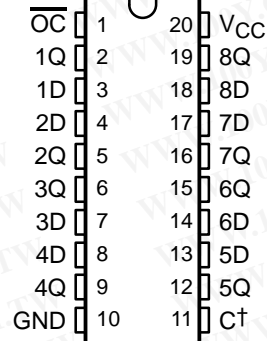
The eight latches of the 'LS373 and 'S373 are transparent D-type latches, meaning that while the enable (C or CLK) input is high, the Q outputs follow the data (D) inputs. When C or CLK is taken low, the output is latched at the level of the data that was set up.

The eight flip-flops of the 'LS374 and 'S374 are edge-triggered D-type flip-flops. On the positive transition of the clock, the Q outputs are set to the logic states that were set up at the D inputs.

Schmitt-trigger buffered inputs at the enable/clock lines of the 'S373 and 'S374 devices simplify system design as ac and dc noise rejection is improved by typically 400 mV due to the input hysteresis. A buffered output-control (\overline{OC}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly.

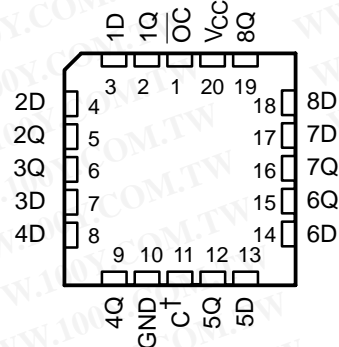
\overline{OC} does not affect the internal operation of the latches or flip-flops. That is, the old data can be retained or new data can be entered, even while the outputs are off.

SN54LS373, SN54LS374, SN54S373,
SN54S374 . . . J OR W PACKAGE
SN74LS373, SN74S374 . . . DW, N, OR NS PACKAGE
SN74LS374 . . . DB, DW, N, OR NS PACKAGE
SN74S373 . . . DW OR N PACKAGE
(TOP VIEW)



† C for 'LS373 and 'S373; CLK for 'LS374 and 'S374.

SN54LS373, SN54LS374, SN54S373,
SN54S374 . . . FK PACKAGE
(TOP VIEW)



† C for 'LS373 and 'S373; CLK for 'LS374 and 'S374.

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SN74LS373, SN74LS374, SN74S373, SN74S374
OCTAL D-TYPE TRANSPARENT LATCHES AND EDGE-TRIGGERED FLIP-FLOPS**

SDLS165B – OCTOBER 1975 – REVISED AUGUST 2002

ORDERING INFORMATION

TA	PACKAGE†	ORDERABLE PART NUMBER	TOP-SIDE MARKING		
0°C to 70°C	PDIP – N	Tube	SN74LS373N	SN74LS373N	
		Tube	SN74LS374N	SN74LS374N	
		Tube	SN74S373N	SN74S373N	
		Tube	SN74S374N	SN74S374N	
	SOIC – DW	Tube	SN74LS373DW	LS373	
		Tape and reel	SN74LS373DWR		
		Tube	SN74LS374DW	LS374	
		Tape and reel	SN74LS374DWR		
		Tube	SN74S373DW	S373	
		Tape and reel	SN74S373DWR		
	SOP – NS	Tape and reel	SN74LS373NSR	74LS373	
		Tape and reel	SN74LS374NSR	74LS374	
	SSOP – DB	Tape and reel	SN74S374NSR	74S374	
		Tape and reel	SN74LS374DBR	LS374A	
	–55°C to 125°C	CDIP – J	Tube	SN54LS373J	SN54LS373J
			Tube	SNJ54LS373J	SNJ54LS373J
Tube			SN54LS374J	SN54LS374J	
Tube			SNJ54LS374J	SNJ54LS374J	
Tube			SN54S373J	SN54S373J	
Tube			SNJ54S373J	SNJ54S373J	
CFP – W		Tube	SN54S374J	SN54S374J	
		Tube	SNJ54S374J	SNJ54S374J	
		Tube	SNJ54LS373W	SNJ54LS373W	
LCCC – FK		Tube	SNJ54LS374W	SNJ54LS374W	
		Tube	SNJ54S374W	SNJ54S374W	
		Tube	SNJ54LS373FK	SNJ54LS373FK	
		Tube	SNJ54LS374FK	SNJ54LS374FK	
			Tube	SNJ54S373FK	SNJ54S373FK
			Tube	SNJ54S374FK	SNJ54S374FK

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† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



**SN54LS373, SN54LS374, SN54S373, SN54S374,
SN74LS373, SN74LS374, SN74S373, SN74S374**
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Function Tables

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'LS373, 'S373
(each latch)

INPUTS			OUTPUT Q
\overline{OC}	C	D	
L	H	H	H
L	H	L	L
L	L	X	Q ₀
H	X	X	Z

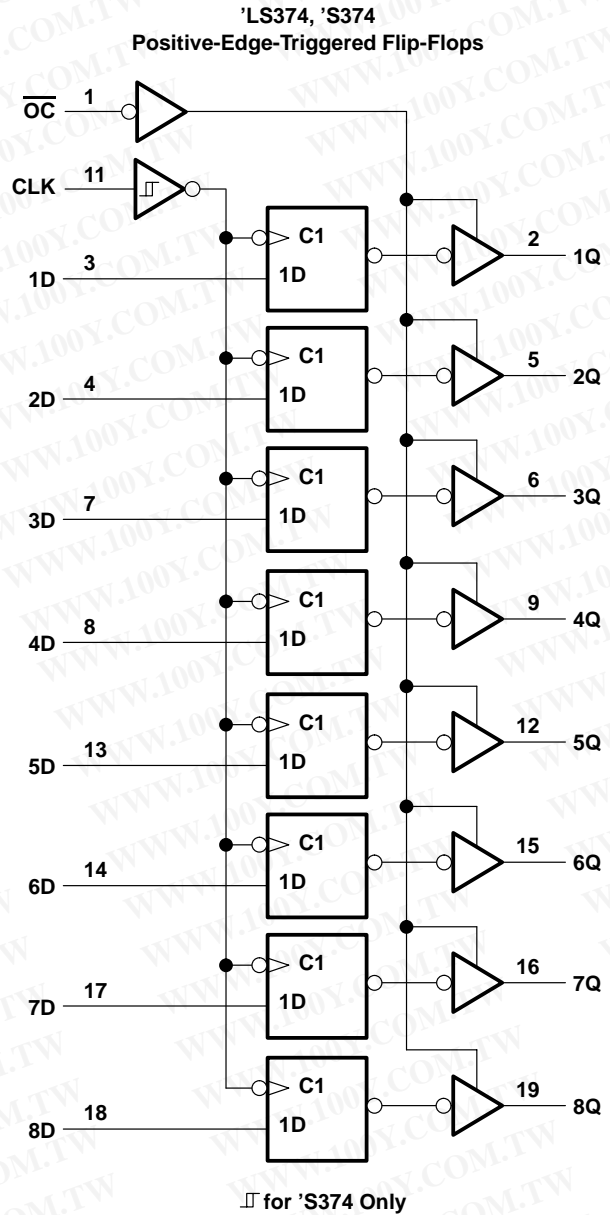
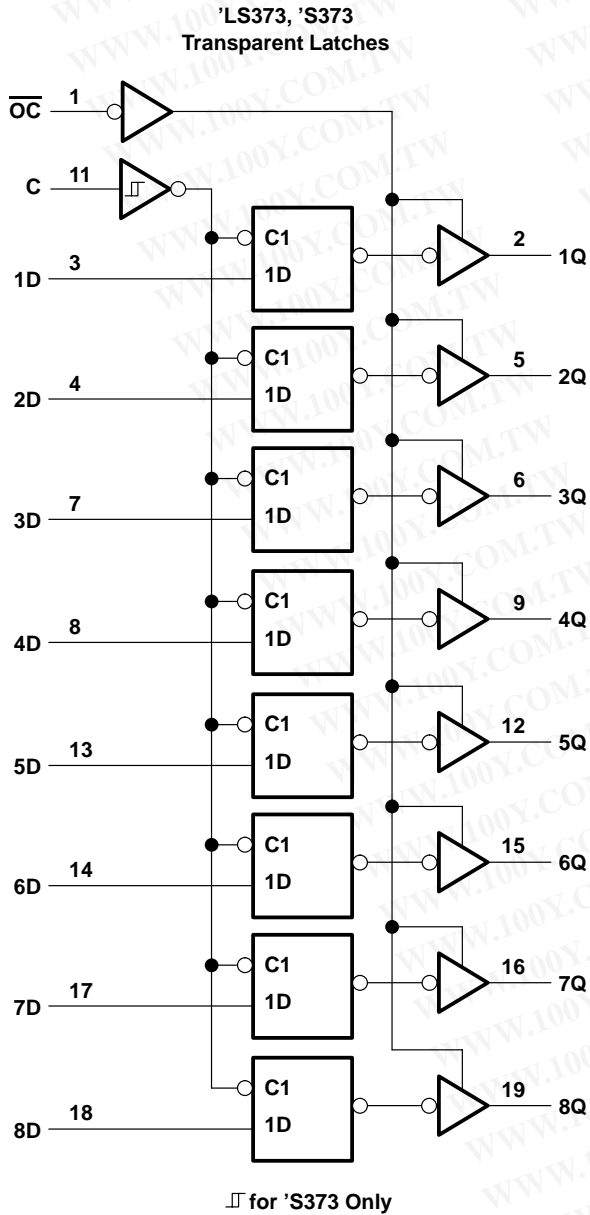
'LS374, 'S374
(each latch)

INPUTS			OUTPUT Q
\overline{OC}	CLK	D	
L	↑	H	H
L	↑	L	L
L	L	X	Q ₀
H	X	X	Z

**SN54LS373, SN54LS374, SN54S373, SN54S374,
SN74LS373, SN74LS374, SN74S373, SN74S374**
OCTAL D-TYPE TRANSPARENT LATCHES AND EDGE-TRIGGERED FLIP-FLOPS

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logic diagrams (positive logic)



Pin numbers shown are for DB, DW, J, N, NS, and W packages.

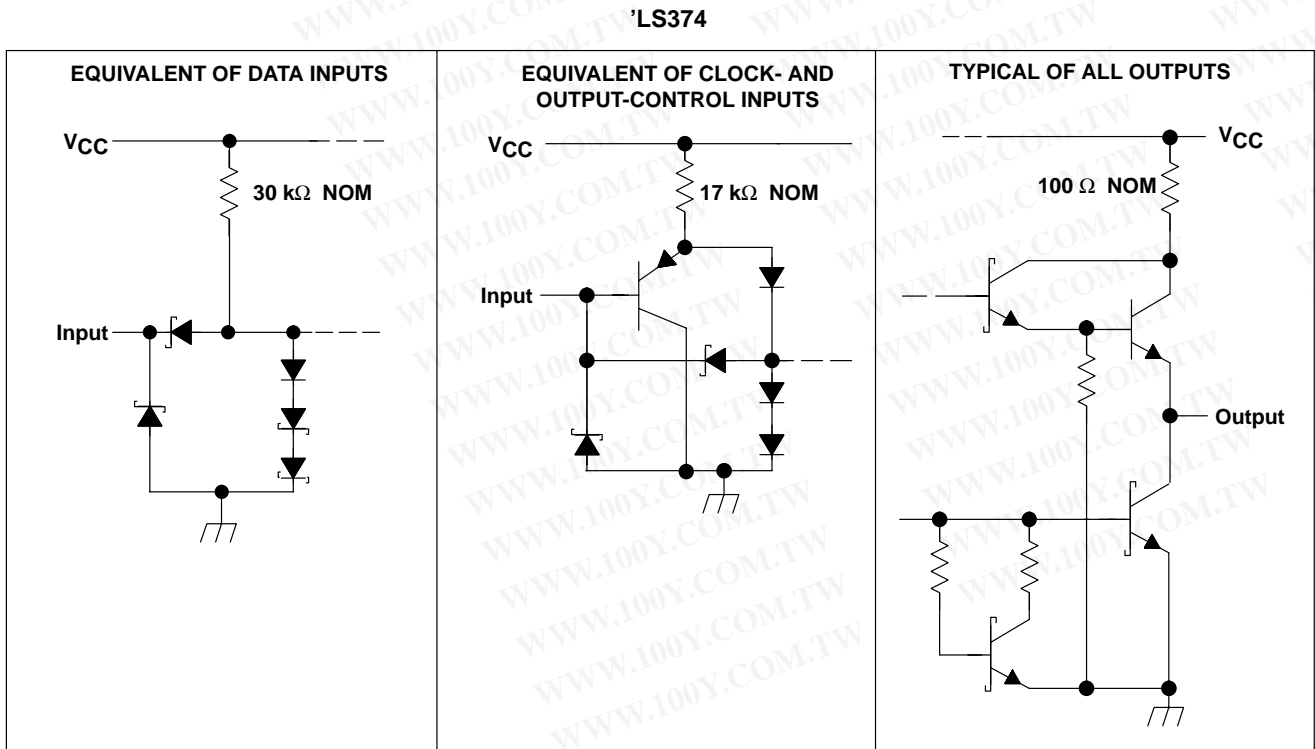
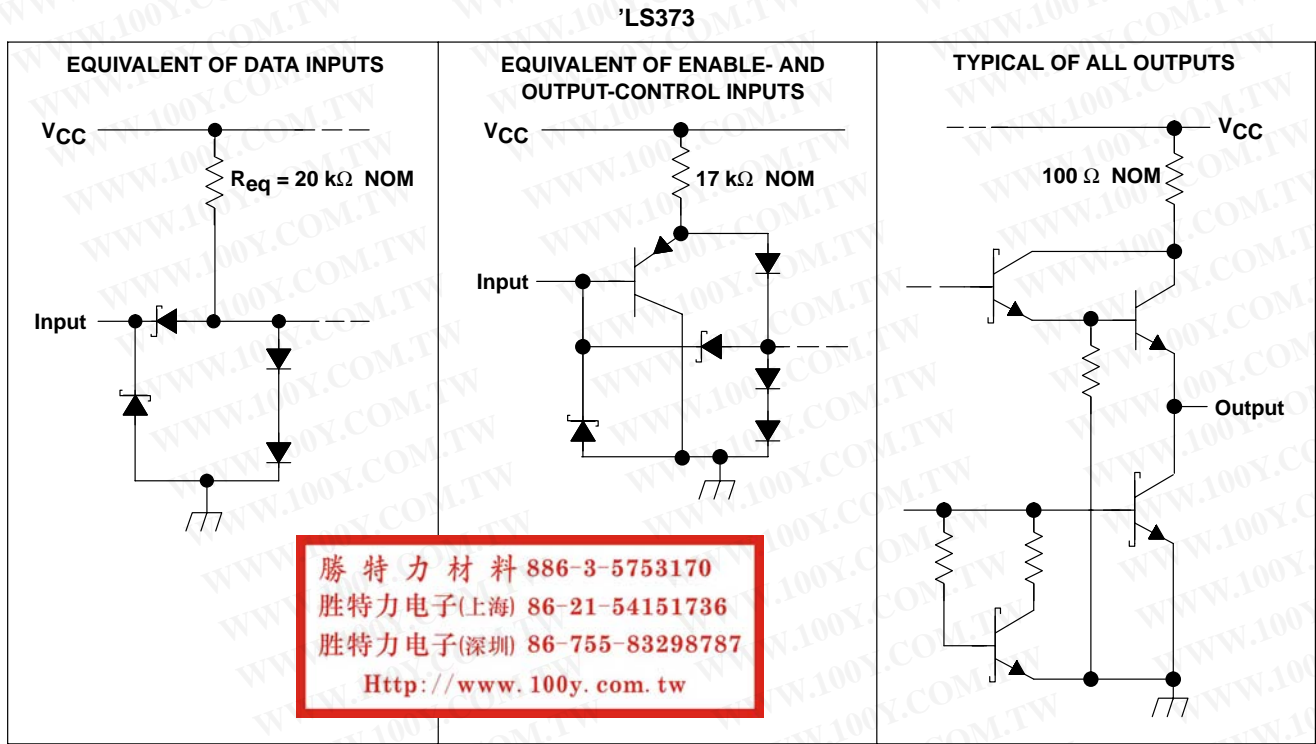
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**SN54LS373, SN54LS374, SN54S373, SN54S374,
SN74LS373, SN74LS374, SN74S373, SN74S374**

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schematic of inputs and outputs



SN54LS373, SN54LS374, SN54S373, SN54S374, SN74LS373, SN74LS374, SN74S373, SN74S374 OCTAL D-TYPE TRANSPARENT LATCHES AND EDGE-TRIGGERED FLIP-FLOPS

SDLS165B – OCTOBER 1975 – REVISED AUGUST 2002

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)† (‘LS devices)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage, V_I	7 V
Off-state output voltage	5.5 V
Package thermal impedance, θ_{JA} (see Note 2): DB package	70°C/W
DW package	58°C/W
N package	69°C/W
NS package	60°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. Voltage values are with respect to network ground terminal.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

		SN54LS'			SN74LS'			UNIT		
		MIN	NOM	MAX	MIN	NOM	MAX			
V_{CC}	Supply voltage	4.5	5	5	4.75	5	5.25	V		
V_{OH}	High-level output voltage			5.5			5.5	V		
I_{OH}	High-level output current			-1			-2.6	mA		
I_{OL}	Low-level output current			12			24	mA		
t_w	Pulse duration	CLK high		15		15		ns		
		CLK low		15		15				
t_{su}	Data setup time	'LS373		5↓		5↓		ns		
		'LS374		20↑		20↑				
t_h	Data hold time	'LS373		20↓		20↓		ns		
		'LS374‡		5↑		0↑				
T_A	Operating free-air temperature			-55		125		0	70	°C

‡ The t_h specification applies only for data frequency below 10 MHz. Designs above 10 MHz should use a minimum of 5 ns (commercial only).

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OCTAL D-TYPE TRANSPARENT LATCHES AND EDGE-TRIGGERED FLIP-FLOPS

SDLS165B – OCTOBER 1975 – REVISED AUGUST 2002

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS'			SN74LS'			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IH} High-level input voltage		2			2			V
V _{IL} Low-level input voltage					0.7			V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = -18 mA				-1.5			V
V _{OH} High-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max, I _{OH} = MAX	2.4	3.4		2.4	3.1		V
V _{OL} Low-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max	I _{OL} = 12 mA			0.25	0.4		V
		I _{OL} = 24 mA				0.35	0.5	
I _{OZH} Off-state output current, high-level voltage applied	V _{CC} = MAX, V _O = 2.7 V, V _{IH} = 2 V				20			μA
I _{OZL} Off-state output current, low-level voltage applied	V _{CC} = MAX, V _O = 0.4 V, V _{IH} = 2 V				-20			μA
I _I Input current at maximum input voltage	V _{CC} = MAX, V _I = 7 V				0.1			mA
I _{IH} High-level input current	V _{CC} = MAX, V _I = 2.7 V				20			μA
I _{IL} Low-level input current	V _{CC} = MAX, V _I = 0.4 V				-0.4			mA
I _{OS} Short-circuit output current§	V _{CC} = MAX	-30		-130	-30		-130	mA
I _{CC} Supply current	V _{CC} = MAX, Output control at 4.5 V	'LS373			24	40		mA
		'LS374			27	40		

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS373			'LS374			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f _{max}			R _L = 667 Ω, C _L = 45 pF, See Note 3				35	50		MHz
t _{PLH}	Data	Any Q	R _L = 667 Ω, C _L = 45 pF, See Note 3	12	18					ns
t _{PHL}				12	18					
t _{PLH}	C or CLK	Any Q	R _L = 667 Ω, C _L = 45 pF, See Note 3	20	30		15	28		ns
t _{PHL}				18	30		19	28		
t _{PZH}	\overline{OC}	Any Q	R _L = 667 Ω, C _L = 45 pF, See Note 3	15	28		20	26		ns
t _{PZL}				25	36		21	28		
t _{PHZ}	\overline{OC}	Any Q	R _L = 667 Ω, C _L = 5 pF	15	25		15	28		ns
t _{PLZ}				12	20		12	20		

NOTE 3: Maximum clock frequency is tested with all outputs loaded.

f_{max} = maximum clock frequency

t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

t_{PZH} = output enable time to high level

t_{PZL} = output enable time to low level

t_{PHZ} = output disable time from high level

t_{PLZ} = output disable time from low level

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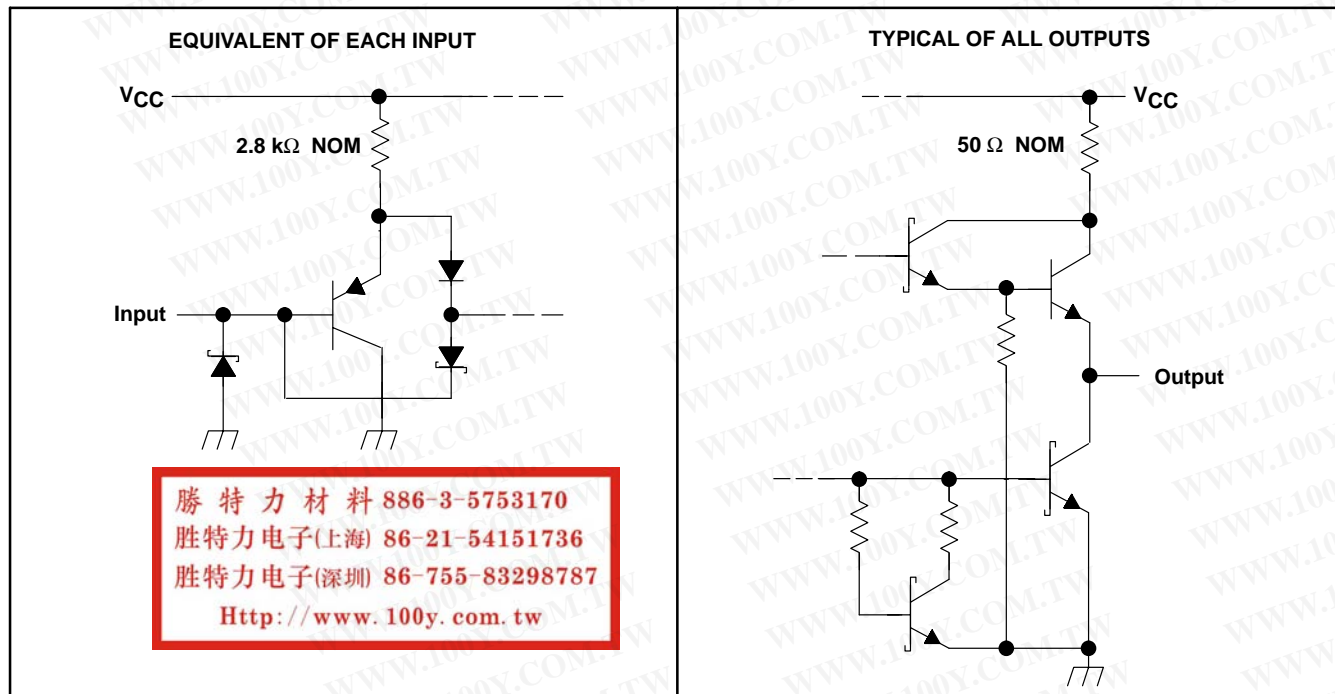
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SN74LS373, SN74LS374, SN74S373, SN74S374
OCTAL D-TYPE TRANSPARENT LATCHES AND EDGE-TRIGGERED FLIP-FLOPS**

SDLS165B – OCTOBER 1975 – REVISED AUGUST 2002

schematic of inputs and outputs

'S373 and 'S374

'S373 and 'S374



**SN54LS373, SN54LS374, SN54S373, SN54S374,
SN74LS373, SN74LS374, SN74S373, SN74S374**
OCTAL D-TYPE TRANSPARENT LATCHES AND EDGE-TRIGGERED FLIP-FLOPS

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**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†
(*S devices)**

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage, V_I	5.5 V
Off-state output voltage	5.5 V
Package thermal impedance, θ_{JA} (see Note 2): DW package	58°C/W
N package	69°C/W
NS package	60°C/W
Storage temperature range, T_{Stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. Voltage values are with respect to network ground terminal.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

		SN54S'			SN74S'			UNIT		
		MIN	NOM	MAX	MIN	NOM	MAX			
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V		
V_{OH}	High-level output voltage			5.5			5.5	V		
I_{OH}	High-level output current			-2			-6.5	mA		
t_w	Pulse duration, clock/enable	High		6		6		ns		
		Low		7.3		7.3				
t_{su}	Data setup time	'S373		0↓		0↓		ns		
		'S374		5↑		5↑				
t_h	Data hold time	'S373		10↓		10↓		ns		
		'S374		2↑		2↑				
T_A	Operating free-air temperature			-55		125		0	70	°C

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**SN54LS373, SN54LS374, SN54S373, SN54S374,
SN74LS373, SN74LS374, SN74S373, SN74S374
OCTAL D-TYPE TRANSPARENT LATCHES AND EDGE-TRIGGERED FLIP-FLOPS**

SDLS165B – OCTOBER 1975 – REVISED AUGUST 2002

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (SN54S373, SN54S374, SN74S373, SN74S374)

PARAMETER		TEST CONDITIONS†				MIN	TYP‡	MAX	UNIT
V _{IH}						2			V
V _{IL}								0.8	V
V _{IK}		V _{CC} = MIN, I _I = -18 mA						-1.2	V
V _{OH}	SN54S'	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OH} = MAX				2.4	3.4		V
	SN74S'					2.4	3.1		
V _{OL}		V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OL} = 20 mA						0.5	V
I _{OZH}		V _{CC} = MAX, V _{IH} = 2 V, V _O = 2.4 V						50	μA
I _{OZL}		V _{CC} = MAX, V _{IH} = 2 V, V _O = 0.5 V						-50	μA
I _I		V _{CC} = MAX, V _I = 5.5 V						1	mA
I _{IH}		V _{CC} = MAX, V _I = 2.7 V						50	μA
I _{IL}		V _{CC} = MAX, V _I = 0.5 V						-250	μA
I _{OS} §		V _{CC} = MAX				-40		-100	mA
I _{CC}	V _{CC} = MAX	'S373	Outputs high	<div style="border: 2px solid red; padding: 5px; display: inline-block;"> 勝特力材料 886-3-5753170 勝特力电子(上海) 86-21-54151736 勝特力电子(深圳) 86-755-83298787 Http://www.100y.com.tw </div>				160	mA
			Outputs low					160	
			Outputs disabled					190	
		'S374	Outputs high					110	
			Outputs low					140	
			Outputs disabled					160	
			CLK and \overline{OC} at 4 V, D inputs at 0 V					180	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'S373			'S374			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f _{max}			R _L = 280 Ω, C _L = 15 pF, See Note 3				75	100		MHz
t _{PLH}	Data	Any Q	R _L = 280 Ω, C _L = 15 pF, See Note 3	7	12					ns
t _{PHL}				7	12					
t _{PLH}	C or CLK	Any Q	R _L = 280 Ω, C _L = 15 pF, See Note 3	7	14		8	15		ns
t _{PHL}				12	18		11	17		
t _{PZH}	\overline{OC}	Any Q	R _L = 280 Ω, C _L = 15 pF, See Note 3	8	15		8	15		ns
t _{PZL}				11	18		11	18		
t _{PHZ}	\overline{OC}	Any Q	R _L = 280 Ω, C _L = 5 pF	6	9		5	9		ns
t _{PLZ}				8	12		7	12		

NOTE 3. Maximum clock frequency is tested with all outputs loaded.

f_{max} = maximum clock frequency

t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

t_{PZH} = output enable time to high level

t_{PZL} = output enable time to low level

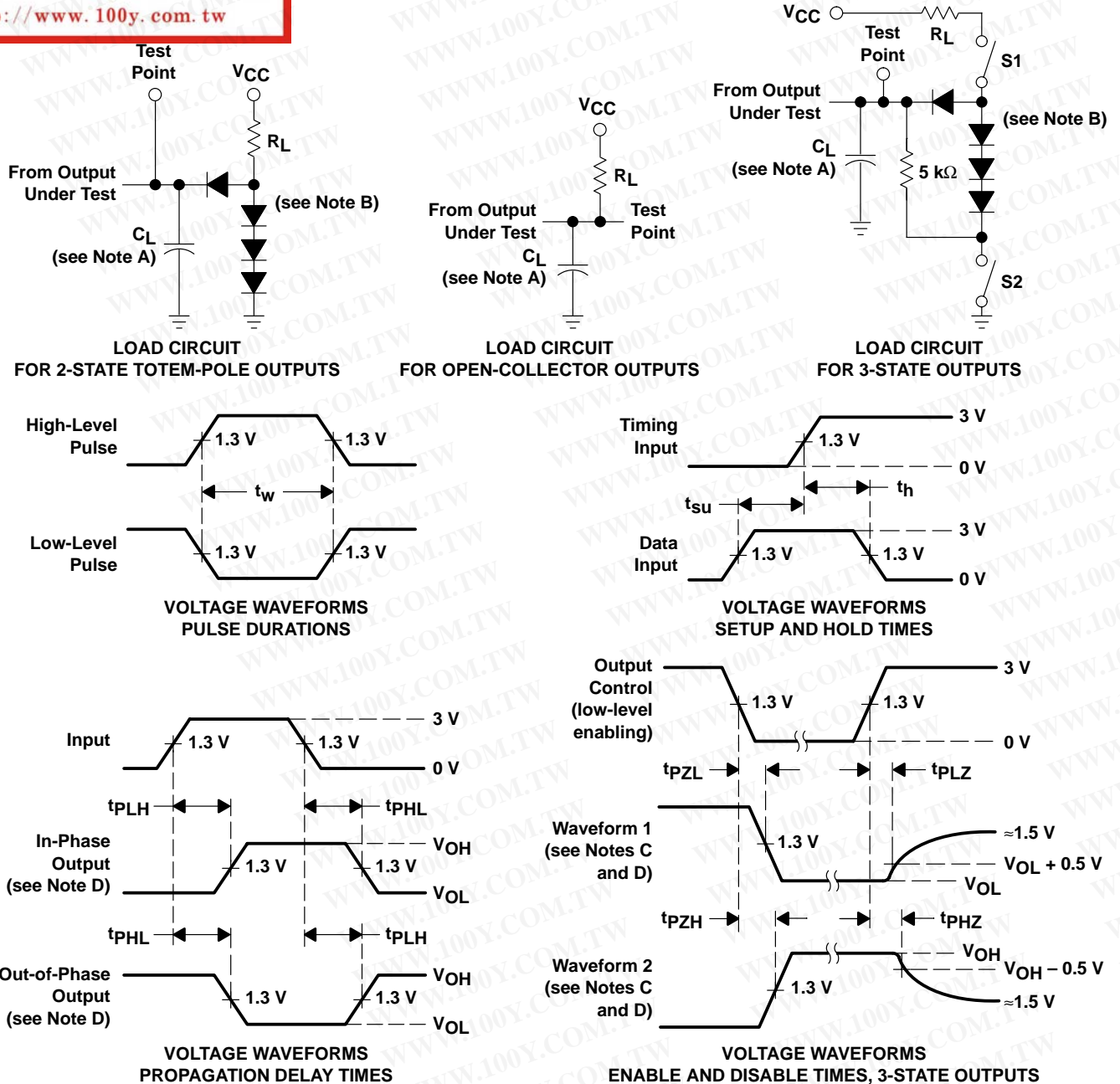
t_{PHZ} = output disable time from high level

t_{PLZ} = output disable time from low level



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PARAMETER MEASUREMENT INFORMATION
SERIES 54LS/74LS DEVICES



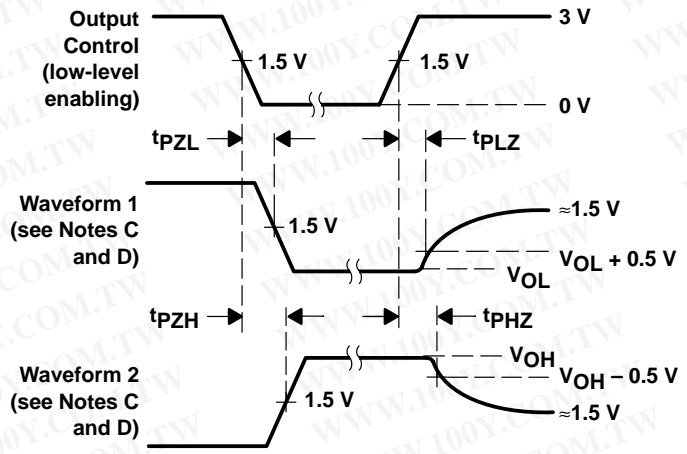
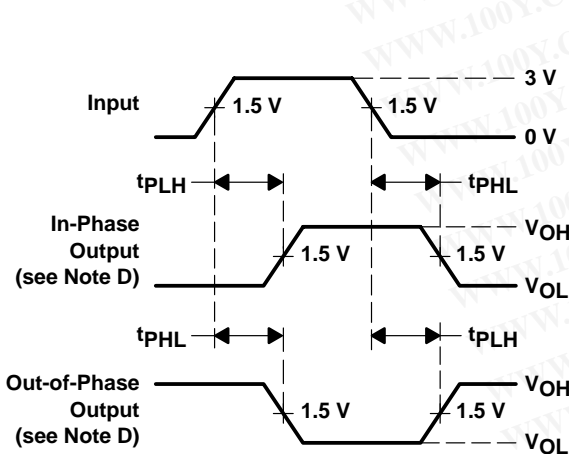
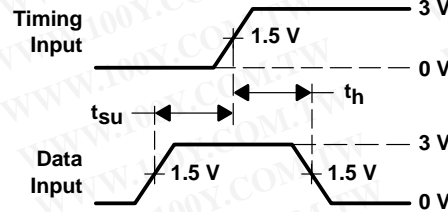
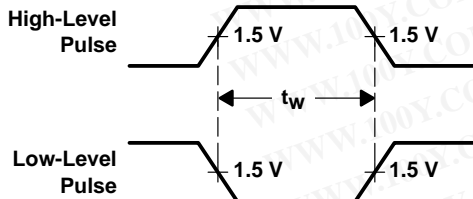
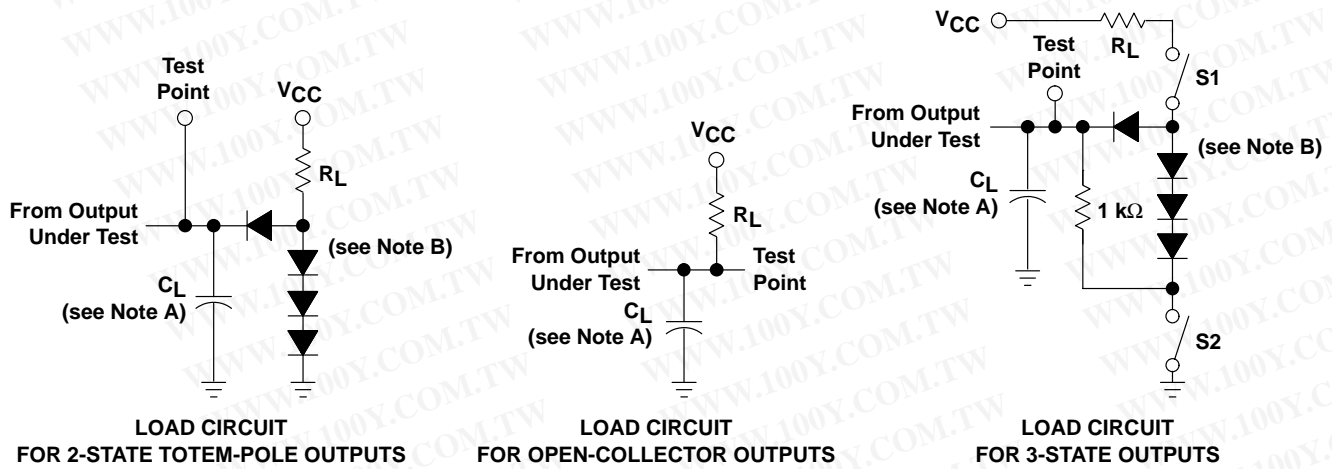
- NOTES: A. C_L includes probe and jig capacitance.
B. All diodes are 1N3064 or equivalent.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. S1 and S2 are closed for t_{PLH} , t_{PHL} , t_{PHZ} , and t_{PLZ} ; S1 is open and S2 is closed for t_{PZH} ; S1 is closed and S2 is open for t_{PZL} .
E. Phase relationships between inputs and outputs have been chosen arbitrarily for these examples.
F. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O \approx 50 \Omega$, $t_r \leq 1.5$ ns, $t_f \leq 2.6$ ns.
G. The outputs are measured one at a time with one input transition per measurement.
H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuits and Voltage Waveforms

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SN74LS373, SN74LS374, SN74S373, SN74S374
OCTAL D-TYPE TRANSPARENT LATCHES AND EDGE-TRIGGERED FLIP-FLOPS**

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**PARAMETER MEASUREMENT INFORMATION
SERIES 54S/74S DEVICES**



- NOTES: A. C_L includes probe and jig capacitance.
 B. All diodes are 1N3064 or equivalent.
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 D. S1 and S2 are closed for t_{pLH} , t_{pHL} , t_{pHZ} , and t_{pLZ} ; S1 is open and S2 is closed for t_{pZH} ; S1 is closed and S2 is open for t_{pZL} .
 E. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O \approx 50 \Omega$; t_r and $t_f \leq 7 \text{ ns}$ for Series 54/74 devices and t_r and $t_f \leq 2.5 \text{ ns}$ for Series 54S/74S devices.
 F. The outputs are measured one at a time with one input transition per measurement.
 G. All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuits and Voltage Waveforms

勝特力材料 886-3-5753170
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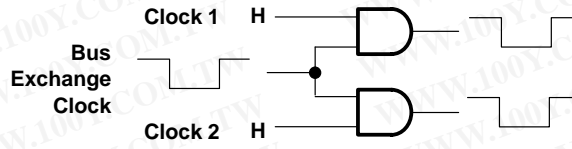
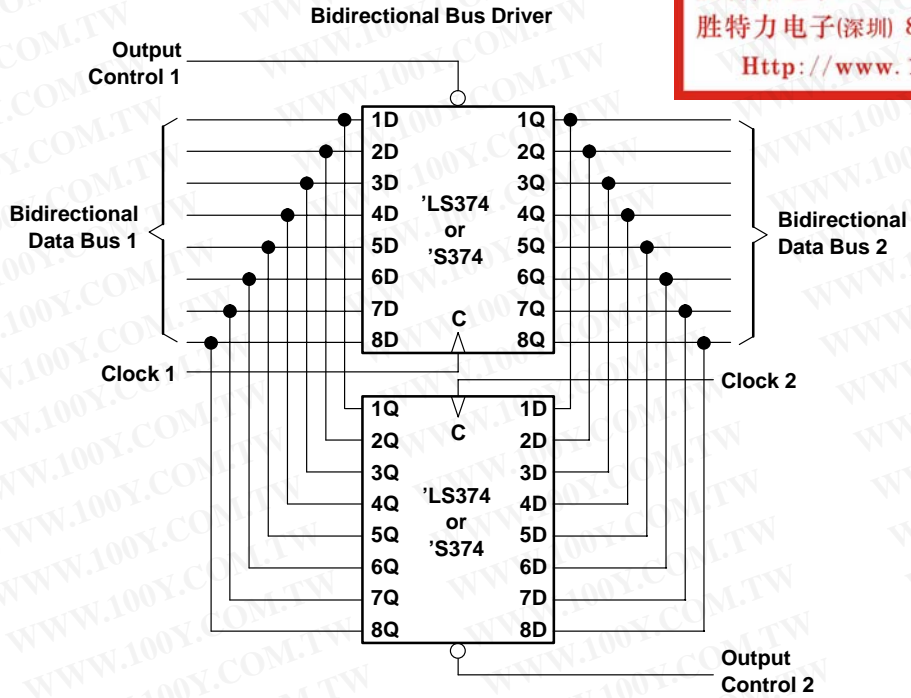


SN54LS373, SN54LS374, SN54S373, SN54S374, SN74LS373, SN74LS374, SN74S373, SN74S374

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TYPICAL APPLICATION DATA

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Clock Circuit for Bus Exchange

Expandable 4-Word by 8-Bit General Register File

