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TLC272, TLC272A, TLC272B, TLC272Y, TLC277 LinCMOS™ PRECISION DUAL OPERATIONAL AMPLIFIERS

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Trimmed Offset Voltage:

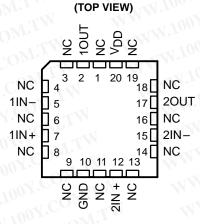
TLC277 . . . 500 μV Max at 25°C, V_{DD} = 5 V

- Input Offset Voltage Drift . . . Typically
 0.1 μV/Month, Including the First 30 Days
- Wide Range of Supply Voltages Over Specified Temperature Range:

0°C to 70°C ... 3 V to 16 V -40°C to 85°C ... 4 V to 16 V -55°C to 125°C ... 4 V to 16 V

- Single-Supply Operation
- Common-Mode Input Voltage Range Extends Below the Negative Rail (C-Suffix, I-Suffix types)
- Low Noise . . . Typically 25 nV/√Hz at f = 1 kHz
- Output Voltage Range Includes Negative Rail
- High Input impedance . . . $10^{12} \Omega$ Typ
- ESD-Protection Circuitry
- Small-Outline Package Option Also Available in Tape and Reel
- Designed-In Latch-Up Immunity

FK PACKAGE



DISTRIBUTION OF TLC277

NC - No internal connection

description

The TLC272 and TLC277 precision dual operational amplifiers combine a wide range of input offset voltage grades with low offset voltage drift, high input impedance, low noise, and speeds approaching those of general-purpose BiFET devices.

These devices use Texas Instruments silicongate LinCMOS $^{\text{TM}}$ technology, which provides offset voltage stability far exceeding the stability available with conventional metal-gate processes.

The extremely high input impedance, low bias currents, and high slew rates make these cost-effective devices ideal for applications previously reserved for BiFET and NFET products. Four offset voltage grades are available (C-suffix and I-suffix types), ranging from the low-cost TLC272 (10 mV) to the high-precision TLC277 (500 μV). These advantages, in combination with good common-mode rejection and supply voltage rejection, make these devices a good choice for new state-of-the-art designs as well as for upgrading existing designs.

INPUT OFFSET VOLTAGE 30 473 Units Tested From 2 Wafer Lots VDD = 5 V TA = 25°C P Package 30 473 Units Tested From 2 Wafer Lots VDD = 5 V TA = 25°C P Package

0

VIO - Input Offset Voltage - µV

LinCMOS is a trademark of Texas Instruments.

-800

400

800

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description (continued)

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AVAILABLE OPTIONS

1100	- 11	1.44	PAC	CKAGED DEVI	CES		00,
TAV.100	V _{IO} max AT 25°C	SMALL OUTLINE (D)	OUTLINE CARRIER DIP DIP		TSSOP (PW)	CHIP FORM (Y)	
MM	500 μV	TLC277CD	\$1 M.	TOOY.	TLC277CP		-11 100 Y.
200 (700	2 mV	TLC272BCD	-x1XV	N. 1	TLC272BCP	- WW	11.5
0°C to 70°c	5 mV	TLC272ACD		1007.	TLC272ACP	_	-1XI 1 00 '
	10mV	TLC272CD	- W	-00X	TLC272CP	TLC272CPW	TLC272Y
TANY	500 μV	TLC277ID		MNT	TLC277IP	N - 1	MA
4000 / 0500	2 mV	TLC272BID	_ ^	100	TLC272BIP	_	1.1V
-40°C to 85°C	5 mV	TLC272AID	V - V	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	TLC272AIP	W -	MMT.
	10 mV	TLC272ID	_	1.10	TLC272IP	<u> </u>	· W

The D package is available taped and reeled. Add R suffix to the device type (e.g., TLC277CDR).

In general, many features associated with bipolar technology are available on LinCMOS™ operational amplifiers without the power penalties of bipolar technology. General applications such as transducer interfacing, analog calculations, amplifier blocks, active filters, and signal buffering are easily designed with the TLC272 and TLC277. The devices also exhibit low voltage single-supply operation, making them ideally suited for remote and inaccessible battery-powered applications. The common-mode input voltage range includes the negative rail.

A wide range of packaging options is available, including small-outline and chip carrier versions for high-density system applications.

The device inputs and outputs are designed to withstand –100-mA surge currents without sustaining latch-up.

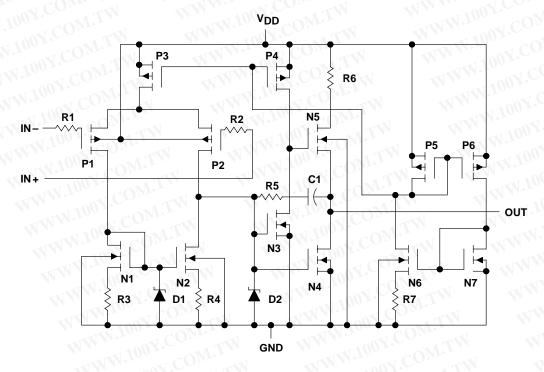
The TLC272 and TLC277 incorporate internal ESD-protection circuits that prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parametric performance.

The C-suffix devices are characterized for operation from 0° C to 70° C. The I-suffix devices are characterized for operation from -40° C to 85° C. The M-suffix devices are characterized for operation over the full military temperature range of -55° C to 125° C.



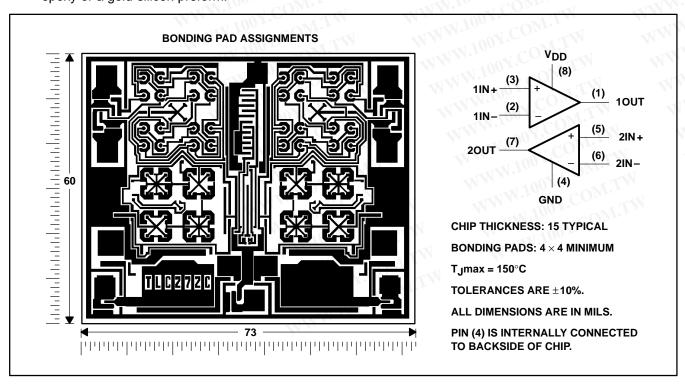
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equivalent schematic (each amplifier)



TLC272Y chip information

This chip, when properly assembled, displays characteristics similar to the TLC272C. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V _{DD} (see Note 1)	18 V
Differential input voltage, V _{ID} (see Note 2)	±V _{DD}
Input voltage range, V _I (any input)	
Input current, I ₁	±5 mA
output current, IO (each output)	±30 mA
Total current into V _{DD}	
Total current out of GND	
Duration of short-circuit current at (or below) 25°C (see Note 3)	unlimited
Continuous total dissipation	
	See Dissipation Rating Table
Continuous total dissipation	See Dissipation Rating Table 0°C to 70°C
Continuous total dissipation	See Dissipation Rating Table0°C to 70°C40°C to 85°C
Continuous total dissipation Operating free-air temperature, T _A : C suffix I suffix M suffix	See Dissipation Rating Table0°C to 70°C40°C to 85°C55°C to 125°C
Continuous total dissipation Operating free-air temperature, T _A : C suffix I suffix	See Dissipation Rating Table0°C to 70°C40°C to 85°C55°C to 125°C65°C to 150°C
Continuous total dissipation Operating free-air temperature, T _A : C suffix I suffix M suffix Storage temperature range	See Dissipation Rating Table0°C to 70°C40°C to 85°C55°C to 125°C65°C to 150°C260°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
 - 2. Differential voltages are at IN+ with respect to IN-.
 - 3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded (see application section).

DISSIPATION RATING TABLE

PACKAGE	T _A ≤ 25°C POWER RATING	DERATING FACTOR ABOVE T _A = 25°C	T _A = 70°C POWER RATING	T _A = 85°C POWER RATING	T _A = 125°C POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	N/A
FK	1375 mW	11 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
Р	1000 mW	8.0 mW/°C	640 mW	520 mW	N/A
PW	525 mW	4.2 mW/°C	336 mW	N/A	N/A

recommended operating conditions

	COM.	C SU	FFIX	I SUF	FIX	M SU	FFIX	(N
	WW. 100 Y. COM	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
Supply voltage, V _{DD}	MM. TIOOX.CO	3	16	4	16	4	16	V
0 1:	V _{DD} = 5 V	-0.2	3.5	-0.2	3.5	0	3.5	TW
Common-mode input voltage, V _{IC}	V _{DD} = 10 V	-0.2	8.5	-0.2	8.5	0	8.5	V
Operating free-air temperature, TA	W. 100	0	70	-40	85	-55	125	°C



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electrical characteristics at specified free-air temperature, $V_{DD} = 5 \text{ V}$ (unless otherwise noted)

MAN	PARAMETER	WW	TEST COND	TIONS	T _A †		C, TLC2 2BC, TLC		UNIT
			0.01100 1. CO			MIN	TYP	MAX	
W	NT 100Y.CO		$V_{O} = 1.4 \text{ V},$	V _{IC} = 0,	25°C	- XXI 1	001.1	10	11
		TLC272C	$R_S = 50 \Omega$,	$R_L = 10 \text{ k}\Omega$	Full range	M 4.	1007.	12	WIL
		TI 007040	V _O = 1.4 V,	V _{IC} = 0,	25°C	MAN.	0.9	5	mV
.,	N 1 100 Y. COM.	TLC272AC	$R_S = 50 \Omega$,	$R_L = 10 \text{ k}\Omega$	Full range	-TVI V	The	6.5	
V _{IO}	Input offset voltage	TI 007000	V _O = 1.4 V,	V _{IC} = 0,	25°C	N T	230	2000	M_T
		TLC272BC	$R_S = 50 \Omega$,	$R_L = 10 \text{ k}\Omega$	Full range	MAN	-11	3000	
		TI 00770	$V_0 = 1.4 \text{ V},$	$V_{IC} = 0$,	25°C	WV	200	500	μV
	W 1. 100 1. CC	TLC277C	$R_S = 50 \Omega$,	$R_L = 10 \text{ k}\Omega$	Full range	- 1	WW.	1500	CO_{N}
α_{VIO}	Temperature coefficient of inp	out offset voltage	WWW.I	ON.COM	25°C to 70°C		1.8	100	μV/°C
	, , , , , , , , , , , , , , , , , , ,	COM		100 TO	25°C		0.1	60	V.CC
liO	Input offset current (see Note	(4)	V 05V	1007.	70°C		7	300	pA
	1001	TV TV	$V_0 = 2.5 \text{ V},$	$V_{IC} = 2.5 V$	25°C		0.6	60	90 x
lΒ	Input bias current (see Note	4) CONT	WW WW		70°C		40	600	pA
.,	Common-mode input voltage	range	W WW	M.100X	25°C	-0.2 to 4	-0.3 to 4.2	MIN	(1V)
VICR	(see Note 5)	100X.COM	TW V		Full range	-0.2 to 3.5		WW	V
	MAG	1 100 Y.	17.7	W	25°C	3.2	3.8	44	
۷он	High-level output voltage		$V_{ID} = 100 \text{ mV},$	$R_L = 10 \text{ k}\Omega$	0°C	3	3.8	N	V
			DIV		70°C	3	3.8		
		M. Ing.	OM.		25°C	OMr.	0	50	
V_{OL}	Low-level output voltage		$V_{ID} = -100 \text{ mV},$	$I_{OL} = 0$	0°C	JOM.	0	50	mV
			TITY		70°C		0	50	
	4	WWW.	CO. TW	WV	25°C	5	23		
AVD	Large-signal differential volta	ge amplification	$V_0 = 0.25 \text{ V to 2 V},$	$R_L = 10 \text{ k}\Omega$	0°C	(4)	27	N	V/mV
		W 1 10	D. COMIT		70°C	4	20	_ 1	
		WW	OOY. CONT.TW		25°C	65	80	INA	
CMRR	Common-mode rejection ratio	o MMM.,	V _{IC} = V _{ICR} min		0°C	60	84	TW	dB
		WW.	COM	· A	70°C	60	85	W	
	0 1 1 1 1 1		100 . COM:	1	25°C	65	95	1.1	1
ksvr	Supply-voltage rejection ratio (ΔVDD/ΔVIO)	Mu	$V_{DD} = 5 \text{ V to } 10 \text{ V},$	$V_0 = 1.4 \text{ V}$	0°C	60	94	M.T.V	dB
	(4*IU/4*IU/	WW	M. COM	W	70°C	60	96	TIL	
			M. To COD	XI	25°C	W.F	1.4	3.2	
I_{DD}	Supply current (two amplifiers	s)	V _O = 2.5 V, No load	$V_{IC} = 2.5 V,$	0°C	UW.M	1.6	3.6	mA
			1.51000		70°C	4	1.2	2.6	

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.



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electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

V	PARAMETER	LM A	TEST CONDI	TIONS	T _A †	TLC272 TLC272			UNIT
			W. 100 1.			MIN	TYP	MAX	M·r.
	MM 1007.00	X N 00700	V _O = 1.4 V,	V _{IC} = 0,	25°C	M T	1.1	10	$M_{i,I}$
		TLC272C	$R_S = 50 \Omega$,	$R_L = 10 \text{ k}\Omega$	Full range	MM	-11	12	-11
		TI 007040	V _O = 1.4 V,	V _{IC} = 0,	25°C	WW	0.9	5	mV
.,	W 1100 X	TLC272AC	$R_S = 50 \Omega$,	$R_L = 10 \text{ k}\Omega$	Full range	-1	wW.	6.5	CON
V _{IO}	Input offset voltage	TI COTODO	V _O = 1.4 V,	V _{IC} = 0,	25°C		290	2000	~0
		TLC272BC	$R_S = 50 \Omega$,	$R_L = 10 \text{ k}\Omega$	Full range		144	3000	Y.C.
		COTION	$V_0 = 1.4 \text{ V},$	$V_{IC} = 0$,	25°C		250	800	μV
		TLC277C	$R_S = 50 \Omega$,	$R_L = 10 \text{ k}\Omega$	Full range			1900	. √ (
α_{VIO}	Temperature coefficient of in	nput offset voltage		N.100 X.	25°C to 70°C	N	2	WW.	μV/°C
		COM		11.100	25°C	κΝ	0.1	60	10
ΙO	Input offset current (see No	te 4)		100 X	70°C	4.4	7	300	pΑ
	MAN	"UNA'CO"	$V_0 = 5 V$,	$V_{IC} = 5 V$	25°C	L.M.	0.7	60	×1100
IΒ	Input bias current (see Note	(4) COM	. W V		70°C	TW	50	600	pΑ
	Common-mode input voltag	o rango	W.TW	WWW.IO	25°C	-0.2 to 9	-0.3 to 9.2	W	V
VICR	(see Note 5)	e range	OM.TW		Full range	-0.2 to 8.5	W	1	V
	V	100x.	-OM:IM	11	25°C	8	8.5		44
Vон	High-level output voltage		$V_{ID} = 100 \text{ mV},$	$R_L = 10 \text{ k}\Omega$	0°C	7.8	8.5		٧
· · ·			COM		70°C	7.8	8.4		W
		A. Too	COM	-31	25°C	A CO	0	50	1
VOL	Low-level output voltage		$V_{ID} = -100 \text{ mV},$	$I_{OL} = 0$	0°C	- ((0	50	mV
			OY.CO.		70°C	101.	0	50	4
		MW.	ON.COM	N	25°C	10	36	TW	
AVD	Large-signal differential volt	age amplification	$V_0 = 1 \text{ V to 6 V},$	R _L = 10 kΩ	0°C	7.5	42		V/mV
			1001. COM.		70°C	7.5	32	1.1	ī
		MM.	11007.00	TW	25°C	65	85	M^{T}	*
CMRR	Common-mode rejection rate	tio W	V _{IC} = V _{ICR} min		0°C	60	88	11	√dB
			M. Inc. CO.	1	70°C	60	88	O_{Mr}	
		4.	W.100 r.	Will	25°C	65	95	·OM·	1
ksvr	Supply-voltage rejection rati (ΔV _{DD} /ΔV _{IO})	0	$V_{DD} = 5 \text{ V to } 10 \text{ V},$	V _O = 1.4 V	0°C	60	94		dB
	(¬^DD/¬^ID)		WW.	UNT	70°C <	60	96	Co	TV
			WW.Inc	ONI	25°C	NW	1.9	4	N.F.
I_{DD}	Supply current (two amplifie	ers)	V _O = 5 V, No load	$V_{IC} = 5 V$	0°C	TANK Y	2.3	4.4	mA
			140 1040		70°C	M.	1.6	3.4	

[†] Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.



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electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

WW	PARAMETER	WA	TEST COND	ITIONS	T _A †		2I, TLC2 2BI, TL		UNIT
			W.1001.			MIN	TYP	MAX	- 1
W	TOOY.CO TITY		V _O = 1.4 V,	V _{IC} = 0,	25°C	-XXI 1	1.1	10	IA
		TLC272I	$R_S = 50 \Omega$,	$R_L = 10 \text{ k}\Omega$	Full range	Mari	1007	13	WIT
			V _O = 1.4 V,	V _{IC} = 0,	25°C	JWW.	0.9	5	mV
	N V 100Y	TLC272AI	$R_S = 50 \Omega$,	$R_L = 10 \text{ k}\Omega$	Full range	-TXXIV	The	7 (7)	M_{TT}
V _{IO}	Input offset voltage	TN	V _O = 1.4 V,	V _{IC} = 0,	25°C	M. A.	230	2000	M.I
		TLC272BI	$R_S = 50 \Omega$,	$R_L = 10 \text{ k}\Omega$	Full range	MAN	-110	3500	-3.1
		VI.	V _O = 1.4 V,	$V_{IC} = 0$,	25°C	WV	200	500	μV
		TLC2771	$R_S = 50 \Omega$,	$R_L = 10 \text{ k}\Omega$	Full range	-1	WW.	2000	COM
α_{VIO}	Temperature coefficient of inp	out offset voltage	WWW.1	ON COM	25°C to 85°C		1.8	100	μV/°C
	7, 100	COMIT	W.W.	100 -1 CO	25°C		0.1	60	S CC
ΙO	Input offset current (see Note	: 4)	MAN		85°C		24	15	pA
	WWW	I CONTAIN	$V_0 = 2.5 \text{ V},$	$V_{IC} = 2.5 V$	25°C		0.6	60	10 J.
lΒ	Input bias current (see Note	4) COM-	WW.		85°C		200	35	pA
	Common-mode input voltage	range COM.	WW WY	M.100X	25°C	-0.2 to	-0.3 to 4.2	MAN	(.1V)
VICR	(see Note 5)	100X.COM	TW V		Full range	-0.2 to 3.5		WW	V
	77	N.100 CO	W.L.	W.W.I	25°C	3.2	3.8	- 1	
Vон	High-level output voltage		$V_{ID} = 100 \text{ mV},$	$R_L = 10 \text{ k}\Omega$	-40°C	3	3.8	- W	V
	WW		UT.	MM M.	85°C	3	3.8		AM
		NW. Too	OM	WW	25°C	OME	0	50	WW
V_{OL}	Low-level output voltage		$V_{ID} = -100 \text{ mV},$	$I_{OL} = 0$	-40°C	-0M.	0	50	mV
-			MITH	1	85°C		0	50	771
		MANA	CO TW	WW	25°C	5	23		11
A_{VD}	Large-signal differential voltage	ge amplification	$V_{O} = 1 \text{ V to 6 V,}$	R _L = 10 kΩ	-40°C	3.5	32	N	V/mV
			COWITY	= 11	85°C	3.5	19	-31	
		MAI 1	ON.TW	V	25°C	65	80	A	
CMRR	Common-mode rejection ratio	MMM.,	V _{IC} = V _{ICR} min		-40°C	60	81	TW	dB
	•		COM		85°C	60	86	TW.	
		- 17	Jan . COM.	- 41	25°C	65	95	1.2	I
ksvr	Supply-voltage rejection ratio		$V_{DD} = 5 \text{ V to } 10 \text{ V},$	V _O = 1.4 V	-40°C	60	92	$M_{1,1,1}$	dB
	$(\Delta V_{DD}/\Delta V_{IO})$		M. Z	WT	85°C	60	96	Time	
		-31	M. LO	TIN	25°C	M	1.4	3.2	
I _{DD}	Supply current (two amplifiers	s)	$V_O = 2.5 \text{ V},$	$V_{IC} = 2.5 V$,	-40°C	M.10	1.9	4.4	mA
		W	No load		85°C		1.1	2.4	

[†] Full range is –40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.



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electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

V	PARAMETER	TW	TEST COND	TIONS	T _A †		21, TLC2 2BI, TL		UNIT
1			W. 1001.			MIN	TYP	MAX	M_{TT}
	MM 1007.Co	117	V _O = 1.4 V,	V _{IC} = 0,	25°C	M. A.	1.1	10	$M_{i,I}$
		TLC2721	$R_S = 50 \Omega$,	$R_L = 10 \text{ k}\Omega$	Full range	MM	-11	13	0×
		OM.	V _O = 1.4 V,	V _{IC} = 0,	25°C	WV	0.9	5	mV
.,	W 100x.	TLC272AI	$R_S = 50 \Omega$,	$R_L = 10 \text{ k}\Omega$	Full range	-1	wW.	7	CON
V _{IO}	Input offset voltage	TI 2070DI	V _O = 1.4 V,	V _{IC} = 0,	25°C	1/4	290	2000	~01
		TLC272BI	$R_S = 50 \Omega$,	$R_L = 10 \text{ k}\Omega$	Full range		MAN.	3500	Y.Co
		CONTRACTOR	$V_0 = 1.4 \text{ V},$	V _{IC} = 0,	25°C		250	800	μV
		TLC277I	$R_S = 50 \Omega$,	$R_L = 10 \text{ k}\Omega$	Full range			2900	~ * 7 (
α_{VIO}	Temperature coefficient of	input offset voltage	WW E	N.1001.	25°C to 85°C	Í	2	WW.	μV/°C
		OM.	- TX	M.Ino	25°C	(N)	0.1	60	10
ΙΟ	Input offset current (see No	ote 4)		XX 100 x	85°C	-7	26	1000	pA
	MM	100 Y.Co	$V_0 = 5 V$,	$V_{IC} = 5 V$	25°C	L.M.	0.7	60	osi 1.00
lΒ	Input bias current (see Not	e 4)	www.		85°C	TW	220	2000	pA
	VI TON	W. Too		MANTO	A CON	-0.2	-0.3		Mir
	MA		V.TV		25°C	to	to		V
VICR	Common-mode input volta (see Note 5)	ge range	WILL		001.00	9	9.2	1/1	11
	(see Note 5)		OM		Full range	-0.2 to			V
			001.100W:11		T dill rango	8.5			WW
		N . 100 1.	COMITY	VY V	25°C	8	8.5		
Vон	High-level output voltage		$V_{ID} = 100 \text{ mV},$	$R_L = 10 \text{ k}\Omega$	-40°C	7.8	8.5		V
J			COM TW	WV	85°C	7.8	8.5		W
		W.Io.	Z COM.	XXI	25°C	V.CO	0	50	
V_{OL}	Low-level output voltage		$V_{ID} = -100 \text{ mV},$	$I_{OL} = 0$	-40°C	-7 CC	0	50	mV
-			OV.COM.TV		85°C	01.	0	50	
		MMA	ONY.CO	N	25°C	10	36	TW	
AVD	Large-signal differential vo	Itage amplification	$V_0 = 1 \text{ V to 6 V},$	R _L = 10 kΩ	-40°C	7	46	TW	V/mV
			100 r. COM.		85°C	.1007	31	1	J
		N V	1100Y.	IM	25°C	65	85	$M_{i,I}$	
CMRR	Common-mode rejection ra	atio 🕠	V _{IC} = V _{ICR} min		-40°C	60	87	Time	dB
		XIV	M.M.COI	T. T.	85°C	60	88	Ober	TW
			MM.100	Mil	25°C	65	95	COM	-XXI
ksvr	Supply-voltage rejection ra $(\Delta V_{DD}/\Delta V_{IO})$	atio	$V_{DD} = 5 \text{ V to } 10 \text{ V},$	V _O = 1.4 V	−40°C	60	92	CON	dB
	(σ.Δ.Π.) (σ.Δ.Π.)		MAN. TOUX.C.	WTI	85°C √	60	96		TY
			WW.	COMP.	25°C	MWW	1.4	4	
I_{DD}	Supply current (two amplifi	ers)	$V_O = 5 V$, No load	$V_{IC} = 5 V$	-40°C	TINI	2.8	5	mA
			INO IOAU		85°C	44 .	1.5	3.2	

[†] Full range is –40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.



^{5.} This range also applies to each input individually.

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electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

MAN	DADAMETER	MA	TEST COND	UTIONS	T. #	TLC27	2M, TLC	277M	
	PARAMETER	WV	TEST COND	ITIONS	TAT	MIN	TYP	MAX	UNIT
11	W.100 COM.	TI 007014	V _O = 1.4 V,	$V_{IC} = 0$,	25°C	11.10	1.1	10	σN,
, 11 V	Leville 100 Property Company	TLC272M	$R_S = 50 \Omega$,	$R_L = 10 \text{ k}\Omega$	Full range	T.W.T	JU -	12	mV
VIO	Input offset voltage	TI 007714	V _O = 1.4 V,	$V_{IC} = 0$,	25°C		200	500	$\Gamma_{I,A}$
	MAN. 102 ON COM.	TLC277M	$R_S = 50 \Omega$,	$R_L = 10 \text{ k}\Omega$	Full range	11111	1005	3750	μV
ανιο	Temperature coefficient of input o voltage	ffset	WWW.100Y	.CON.T	25°C to 125°C	WWW	2.1	N.CO	μV/°C
	M.M. O.A.CO.	W	WWW	1.00	25°C	MM	0.1	60	pA
lio	Input offset current (see Note 4)		W. W. W. Too	COM.	125°C	W	1.4	15	nA
	M. 100 x 20M	LA	$V_0 = 2.5 \text{ V}$	$V_{IC} = 2.5 V$	25°C	-1	0.6	60	pA
I _{IB}	Input bias current (see Note 4)		MM		125°C		9	35	nA
	Common-mode input voltage rang		MMM	100X.CO	25°C	0 to 4	-0.3 to 4.2	N.100	V
VICR	(see Note 5)	OM.TV	A MM		Full range	0 to 3.5	M	NW.1	
	WWW.I	COMP	VV VV	MAN.	25°C	3.2	3.8	M. A.	400
Vон	High-level output voltage		V _{ID} = 100 mV,	$R_L = 10 \text{ k}\Omega$	−55°C	3	3.8	NW I	V
			In		125°C	3	3.8		N.10
	MM	N.Co	TW I	N 11 10	25°C	In	0	50	-xv 1
VOL	Low-level output voltage		$V_{ID} = -100 \text{ mV},$	$I_{OL} = 0$	−55°C	TW	0	50	mV
			MILL		125°C		0	50	MM.
	W.	100 1.	OM_{-1}		25°C	5	23	,	TAN V
AVD	Large-signal differential voltage a	mplification	$V_0 = 0.25 \text{ V to 2 V}$	$R_L = 10 \text{ k}\Omega$	−55°C	3.5	35		V/m\
			COM		125°C	3.5	16		WW
		M.Ing	COM		25°C	65	80		WV
CMRR	Common-mode rejection ratio		V _{IC} = V _{ICR} min		-55°C	60	81		dB
			Y.COMITW		125°C	60	84		W
	W	MAN	V.Com	W	25°C	65	95		
SVR	Supply-voltage rejection ratio (ΔVDD/ΔVIO)		$V_{DD} = 5 \text{ V to } 10 \text{ V},$	V _O = 1.4 V	−55°C	60	90	W	dB
	(\(\text{TA}\)\(\text{D}\)\(\text{TA}\)		DOY. COM.TV	-	125°C	60	97	- 1	
		MAN	1007. TIME	W	25°C	00 x .	1.4	3.2	
I_{DD}	Supply current (two amplifiers)		$V_O = 2.5 V$, No load	$V_{IC} = 2.5 V,$	−55°C	anny.	2	5	mA
			INO IDAU		125°C	.10	CG	2.2	I

[†] Full range is –55°C to 125°C.

WWW.100Y.COM.TW NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

5. This range also applies to each input individually. WWW.100Y.COM.TW



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electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

W	BARAMETER	. W	TEOT CONE	ITIONIC .	T. +	TLC272	M, TLC	277M	7.7.
	PARAMETER		TEST COND	ITIONS	T _A †	MIN	TYP	MAX	UNIT
	COM	=100=014	$V_0 = 1.4 V$,	$V_{IC} = 0$,	25°C	VWI	1.1	10	Mrs
.,	MM, 100, 100	TLC272M	$R_S = 50 \Omega$,	$R_L = 10 \text{ k}\Omega$	Full range	-XXI	W.10	12	mV
V_{IO}	Input offset voltage	TI 007714	$V_0 = 1.4 V$,	V _{IC} = 0,	25°C	W.	250	800	LOOL
		TLC277M	$R_S = 50 \Omega$,	$R_L = 10 \text{ k}\Omega$	Full range	W	14.	4300	μV
ανιο	Temperature coefficient of in voltage	put offset	WWW.	100 Y.COM	25°C to 125°C	W	2.2	1007	μV/°C
		TW	M.M.	TOUX.CO.	25°C		0.1	60	pA
lo	Input offset current (see Not	e 4)		. Joseph CC	125°C		1.8	15	nA
	77 771,100	"COM.	$V_0 = 5 V$,	$V_{IC} = 5 V$	25°C		0.7	60	pA
lΒ	Input bias current (see Note	4)	A All		125°C		10	35	nA
	Common-mode input voltag	e range	M MA	MM.100X.	25°C	0 to 9	-0.3 to 9.2	MM	1002 1007
VICR	(see Note 5)	100X'CON	LTW V		Full range	0 to 8.5	4	MM	V V
	TWV	V. Jan CO	NI.	WWW	25°C	8	8.5	W	MAG
∨он	High-level output voltage		V _{ID} = 100 mV,	$R_L = 10 \text{ k}\Omega$	−55°C	7.8	8.5		V
			WIIN		125°C	7.8	8.4	V	-TVN
	W	MAN.	WIT	MM	25°C	TILL	0	50	N.A.
V_{OL}	Low-level output voltage		$V_{ID} = -100 \text{ mV},$	$I_{OL} = 0$	−55°C	Obe	0	50	mV
			COMIT		125°C	COM.	0	50	- XI VN
		100	OM.TW	111	25°C	10	36		44
AVD	Large-signal differential volta amplification	age	$V_0 = 1 \text{ V to 6 V},$	$R_L = 10 \text{ k}\Omega$	−55°C	7	50		V/mV
	amplification		COMP		125°C	(C7)	27	N	1
		W.I	in COM.	×1	25°C	65	85	- 1	
CMRR	Common-mode rejection rat	io	V _{IC} = V _{ICR} min		−55°C	60	87	1.4	dB
			TOON.CO		125°C	60	86	TW	
		WWW	· COMP	TV	25°C	65	95	W	
ksvr	Supply-voltage rejection rati	0	$V_{DD} = 5 \text{ V to } 10 \text{ V},$	V _O = 1.4 V	−55°C	60	90	11.	_ dB
	(ΔV _{DD} /ΔV _{IO})		W 100Y.	LT^{N}	125°C	60	97	M_{-1}	-7
		W	4007.00	WILL	25°C	100	1.9	4	M
I_{DD}	Supply current (two amplifie	rs)	V _O = 5 V, No load	$V_{IC} = 5 V$	−55°C	Miss.	3	6	mA
			140 loau		125°C	VIN'I	1.3	2.8	- 11

[†] Full range is -55°C to 125°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

5. This range also applies to each input individually. WWW.100Y.COM.TW



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electrical characteristics, $V_{DD} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$ (unless otherwise noted)

	1007.00	TEST SOM	DITIONS	100 T	LC272Y	M.T	
WIT	PARAMETER	TEST CONI	DITIONS	MIN	TYP	MAX	UNIT
V _{IO}	Input offset voltage	$V_{O} = 1.4 \text{ V},$ $R_{S} = 50 \Omega,$	$V_{IC} = 0$, $R_L = 10 \text{ k}\Omega$	WW.L	001.1 ^C	10	mV
ανιο	Temperature coefficient of input offset voltage	100Y.CO	N N	NV V	1.8		μV/°C
lio	Input offset current (see Note 4)	VON EV	0.514	MAN AN	0.1	Cor	pA
l _{IB}	Input bias current (see Note 4)	$V_0 = 2.5 \text{ V},$	$V_{IC} = 2.5 V$	TINV	0.6	<1 CO	pA
VICR	Common-mode input voltage range (see Note 5)	M.100X.COM	I.TW	-0.2 to 4	-0.3 to 4.2	OY.C	N. A.
VOH	High-level output voltage	$V_{ID} = 100 \text{ mV},$	$R_L = 10 \text{ k}\Omega$	3.2	3.8	00x.	V
VOL	Low-level output voltage	$V_{ID} = -100 \text{ mV},$	$I_{OL} = 0$	W	0	50	mV
AVD	Large-signal differential voltage amplification	$V_0 = 0.25 \text{ V to 2 V}$	$R_L = 10 \text{ k}\Omega$	5	23		V/mV
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}min$	OM	65	80	1.Inc	dB
ksvr	Supply-voltage rejection ratio (ΔV _{DD} /ΔV _{IO})	$V_{DD} = 5 \text{ V to } 10 \text{ V},$	V _O = 1.4 V	65	95	W.10	dB
I _{DD}	Supply current (two amplifiers)	V _O = 2.5 V, No load	V _{IC} = 2.5 V,	10	1.4	3.2	mA

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

5. This range also applies to each input individually.

electrical characteristics, V_{DD} = 10 V, T_A = 25°C (unless otherwise noted)

		7507.001	1007	T	LC272Y		-x1 10
	PARAMETER	TEST CON	DITIONS	MIN	TYP	MAX	UNIT
V _{IO}	Input offset voltage	$V_{O} = 1.4 \text{ V},$ $R_{S} = 50 \Omega,$	$V_{IC} = 0$, $R_L = 10 \text{ k}\Omega$	M.TV	1.1	10	mV
α_{VIO}	Temperature coefficient of input offset voltage	THE WIN	1100X.C	Time	1.8		μV/°C
lιο	Input offset current (see Note 4)	. 1 W - 1 W	N. Jan.	OP.	0.1		pA
I _{IB}	Input bias current (see Note 4)	$V_O = 5 V$	$V_{IC} = 5 V$	CO_{Mr} .	0.7		pA
VICR	Common-mode input voltage range (see Note 5)	ONTAN A	NWW.100	-0.2 to 9	-0.3 to 9.2	×1	٧
Vон	High-level output voltage	$V_{ID} = 100 \text{ mV},$	$R_L = 10 \text{ k}\Omega$	8	8.5	-1	V
V_{OL}	Low-level output voltage	$V_{ID} = -100 \text{ mV},$	IOL = 0	101.	0	50	mV
AVD	Large-signal differential voltage amplification	$V_0 = 1 \text{ V to 6 V},$	$R_L = 10 \text{ k}\Omega$	10	36	TW	V/mV
CMRR	Common-mode rejection ratio	V _{IC} = V _{ICR} min	WW.	65	85	TV.	dB
ksvr	Supply-voltage rejection ratio (ΔV _{DD} /ΔV _{IO})	$V_{DD} = 5 \text{ V to } 10 \text{ V},$	V _O = 1.4 V	65	95	1.1.	dB
I _{DD}	Supply current (two amplifiers)	V _O = 5 V, No load	V _{IC} = 5 V,	W.1003	1.9	4	mA

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.



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operating characteristics at specified free-air temperature, $V_{DD} = 5 \text{ V}$

V	PARAMETER	TEST CO	NDITIONS	TA	TLC272 TLC272	C, TLC2 BC, TLC		UNIT
4		1 100 r.	COM.1		MIN	TYP	MAX	M_{TT}
	WWW.100Y.CO.TTW	100	T.IV	25°C	M.	3.6	17.0	M.T.
		OWW.	V _{IPP} = 1 V	√ 0°C	MM	4	WY.C	717
0.0	ON.100 x	$R_L = 10 \text{ k}\Omega$	COM.	70°C	TIV.	3		COM
SR	Slew rate at unity gain	C _L = 20 pF, See Figure 1	OM.	25°C		2.9	Ing	V/μs
		Gee rigare r	V _{IPP} = 2.5 V	0°C		3.1	1007	
		MMM.	OON.CO	70°C		2.5	100	Y.Co.
٧n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	$R_S = 20 \Omega$,	25°C		25	W.10	nV/√ Hz
	MMM. CO.CO. TW	MM	TOON CO	25°C	N	320	-11	00 X.C
ВОМ	Maximum output-swing bandwidth	$V_O = V_{OH}$, $R_L = 10 \text{ k}\Omega$,	C _L = 20 pF,	0°C	VV	340	MAN	kHz
		$R_L = 10 \text{ Ksz},$	See Figure 1	70°C		260		700
	WW. 1007. CM.TW		1001	25°C	1.	1.7	-11	1.100
В1	Unity-gain bandwidth	V _I = 10 mV, See Figure 3	$C_L = 20 pF$,	0°C		2	MA	MHz
		See rigure 5	WWW.I	70°C	TW	1.3	WW	W
	11 100 COM.	L C	IN In.	25°C	NI.	46°	- 11	M.To
φm	Phase margin	$V_{I} = 10 \text{ mV},$ $C_{L} = 20 \text{ pF},$	f = B ₁ , See Figure 3	0°C	MIT	47°		-XV.1
		OL = 20 pF,	See Figure 3	70°C	TITY	43°		-XI

operating characteristics at specified free-air temperature, V_{DD} = 10 V

	PARAMETER	TEST CO	NDITIONS	TAO	TLC272			UNIT
		COMP	VV	11.7.	MIN	TYP	MAX	W
	W. 100 .	OMIT		25°C	-1 CO	5.3	*1	
		V.T.M	V _{IPP} = 1 V	0°C	0.7.0	5.9	44	
0.0	WWW.	$R_L = 10 \text{ k}\Omega$	W V	70°C	CON.	4.3		\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
SR	Slew rate at unity gain	C _L = 20 pF, See Figure 1	N .	25°C	anv.C	4.6	TW	V/μs
		Goo'r igure 'r	V _{IPP} = 5.5 V	0°C	100	5.1		
		100X.COM	LIN	70°C	11007.	3.8	V.I.A.	
Vn	Equivalent input noise voltage	f = 1 kHz, See Figure 2	$R_S = 20 \Omega$,	25°C	V.1005	25	M.T	nV/√Hz
	Marie	1007.	Willy	25°C	W.100	200	oM^{1}	
Вом	Maximum output-swing bandwidth	V _O = V _{OH} ,	C _L = 20 pF,	0°C	110	220	1100	kHz
G	VV	$R_L = 10 \text{ k}\Omega$	See Figure 1	70°C	MAN.	140	CO.	TW
	7	M. Too	OM	25°C	WW.	2.2	$CO_{\tilde{D}}$	
В1	Unity-gain bandwidth	$V_I = 10 \text{ mV},$	$C_L = 20 pF$,	0°C	-3141	2.5	- c0	MHz
•		See Figure 3	WT.IV	70°C	MAL	1.8	Y.	
		MW.	V.COP	√ 25°C	WW	49°		
φm	Phase margin	$V_{I} = 10 \text{ mV},$ $C_{L} = 20 \text{ pF},$	f = B ₁ , See Figure 3	0°C		50°		
		CL = 20 pr,	See Figure 3	70°C		46°		

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operating characteristics at specified free-air temperature, V_{DD} = 5 V

WW	PARAMETER	TEST CO	NDITIONS	TA		2I, TLC2 2BI, TL		UNIT
4/1/1/		N.1001.	M^{-1}	4	MIN	TYP	MAX	- * T
W	MI 100X'CO LIM MM	1007.0	WILM	25°C	-xx 1	3.6	Mos	1.41
× 1		VV.	V _{IPP} = 1 V	-40°C	Mari	4.5		WT
0.0	OM:	$R_L = 10 \text{ k}\Omega$	COM	85°C	JWW.	2.8	1.COE	W
SR	Slew rate at unity gain	C _L = 20 pF, See Figure 1	COM.I.	25°C	- TANIV	2.9	-1 CO	V/μs
		N Goo'r igai'o'r	V _{IPP} = 2.5 V	−40°C	11	3.5	1.	M.T.
		M.M.	Y.COM	√ 85°C	MM	2.3	10 X.C	-31 J
Vn	Equivalent input noise voltage	f = 1 kHz, See Figure 2	$R_S = 20 \Omega$,	25°C	WV	25	00Y.	nV/√ Hz
	MANN ON COME TW	MMA	OUX.CO	25°C	W	320	1007	
Вом	Maximum output-swing bandwidth	$V_O = V_{OH}$, $R_I = 10 \text{ k}\Omega$,	C _L = 20 pF, See Figure 1	−40°C	1	380		kHz
		KL = 10 KS2,	See rigure r	85°C		250	N'Inc	47 CO
	WW. 100X.C. TW	M. A.	x 100 y	25°C		1.7	xV.10) y.
B ₁	Unity-gain bandwidth	V _I = 10 mV, See Figure 3	$C_L = 20 pF$,	-40°C		2.6	-11	MHz
		See Figure 3	W. To OV.C	85°C	N	1.2	MAN	. NOV.
	M. 100 COM. I.		VW.100	25°C	.	46°		In.
φm	Phase margin	$V_{I} = 10 \text{ mV},$ $C_{L} = 20 \text{ pF},$	f = B ₁ , See Figure 3	-40°C	N.	49°		1.100 x
		OL = 20 μr,	See Figure 3	85°C		43°	MAA.	100

operating characteristics at specified free-air temperature, V_{DD} = 10 V

	PARAMETER	TEST CO	NDITIONS	T _A CO		2I, TLC2 2BI, TL0		UNIT
	WW.IV	N. Tank		av.C	MIN	TYP	MAX	
		OJUL	WWW	25°C	OM	5.3		WIN
		MIL	$V_{IPP} = 1 V$	-40°C	Mo	6.8		
SR	Slew rate at unity gain	$R_L = 10 \text{ k}\Omega$, $C_L = 20 \text{ pF}$,	WW	85°C		4		V/μs
OK.	Siew rate at utility gain	See Figure 1	WW	25°C	$C_{O_{2a}}$	4.6		ν/μδ
		OM	V _{IPP} = 5.5 V	-40°C	1,00	5.8	« 1	
		Y.V. TW		85°C	1.0	3.5	N.A.	
٧n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	$R_S = 20 \Omega$,	25°C	101.Ce	25	N.	nV/√H:
	WW	00 1.	14	25°C	100 1.	200	LA	
Вом	Maximum output-swing bandwidth	$V_O = V_{OH}$	C _L = 20 pF,	-40°C	1007	260	TW	kHz
•	WW	$R_L = 10 \text{ k}\Omega$	See Figure 1	85°C		130		
	W. T.	V.100	1.1.	25°C	M.Too.	2.2	Mr.	* I
B ₁	Unity-gain bandwidth	$V_I = 10 \text{ mV},$	$C_L = 20 pF$,	-40°C	- N 100	3.1	W.I	MHz
•	WW	See Figure 3		85°C	10	1.7		
		11 Jan 2 C	OMI. A	25°C	114.5	49°		
ф т	Phase margin	$V_{I} = 10 \text{ mV},$	$f = B_1$	−40°C		52°		1
	W.	C _L = 20 pF,	See Figure 3	85°C		46°		1

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operating characteristics at specified free-air temperature, V_{DD} = 5 V

V	W. O. Co	1007:	TW		TLC27	2M, TLC	277M	$V_{i,j,j,j}$
	PARAMETER	TEST CO	NDITIONS	TA	MIN	TYP	MAX	UNIT
	1. 100 COM.	M.Inc	COM	25°C		3.6	A CC	Mr.
		M. 100.	V _{IPP} = 1 V	−55°C	- 1	4.7	-1 (OM_{T}
0.0	WWW.COS.COS	$R_L = 10 \text{ k}\Omega$	Y.Com.T	125°C	11 4.	2.3	10 A.	.oM.T
SR	Slew rate at unity gain	C _L = 20 pF, See Figure 1	V.Co.	25°C	W	2.9	ooy.	V/μs
		occ rigare r	V _{IPP} = 2.5 V	−55°C	×N	3.7	.07	CO_{Mr}
			100 y	125°C	4.	2	700.	COD
Vn	Equivalent input noise voltage	f = 1 kHz, See Figure 2	$R_S = 20 \Omega$,	25°C		25	N.100	nV/√ Hz
	M. 1001. CONT. 1.	41	N.100	25°C	ſ	320	M'In	- <1 C
Вом	Maximum output-swing bandwidth	$V_O = V_{OH}$, $R_L = 10 \text{ k}\Omega$,	C _L = 20 pF, See Figure 1	−55°C		400	-TXV.1	kHz
		K_ = 10 KS2,	See Figure 1	125°C		230	VV 1	100Y.
	MAN TO COM	TO U	WW. To av	25°C		1.7	MA	You
В1	Unity-gain bandwidth	V _I = 10 mV, See Figure 3	$C_L = 20 pF$,	-55°C	-31	2.9	TIN V	MHz
		See Figure 3	100	125°C	T.A.	1.1	/V '	W.100
	MAN	TW	WW 100	25°C	TW	46°	MA	110
φm	Phase margin	$V_{I} = 10 \text{ mV},$ $C_{I} = 20 \text{ pF},$	f = B ₁ , See Figure 3	-55°C	W	49°	W	1111
		OL = 20 pr,	Coor iguid 3	125°C	110.	41°		MM.T

operating characteristics at specified free-air temperature, $V_{DD} = 10 \text{ V}$

			NO TIONS	-01/	TLC27	2M, TLC	277M	MA
	PARAMETER	TEST CO	NDITIONS	TA	MIN	TYP	MAX	UNIT
	M. 100x	J.M.I.	NA .	25°C	CON	5.3	ĭ	4
		TITT	V _{IPP} = 1 V	−55°C		7.1		
00	NWW.10	$R_L = 10 \text{ k}\Omega$	W	125°C	N.Co.	3.1	N	\ \ \ \ \
SR	Slew rate at unity gain	C _L = 20 pF, See Figure 1	J	25°C	V.C	4.6	W	V/μs
		GGG T Iguro T	V _{IPP} = 5.5 V	−55°C	10-	6.1	-31	
	MM	007.00		125°C	1007.	2.7	1.14	
٧n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	$R_S = 20 \Omega$,	25°C	1.100Y	25	I.TW	nV/√Hz
	Mari	1 100Y.	LTW	25°C	W 100	200	$M_{i,L}$	
Вом	Maximum output-swing bandwidth	$V_O = V_{OH}$	C _L = 20 pF,	−55°C	-1100	280	-117	kHz
		$R_L = 10 \text{ k}\Omega$	See Figure 1	125°C	111.	110	Oh	TW
	77	111.100	OM.	25°C	MM^{-1}	2.2	OM	-33
В1	Unity-gain bandwidth	V _I = 10 mV, See Figure 3	$C_L = 20 pF$,	−55°C	-TXN .1	3.4	401	MHz
		See Figure 3	TW	125°C	N	1.6		VII
	4	MININ	COM	25°C	MANAN	49°	V.CO	
φm	Phase margin	$V_{I} = 10 \text{ mV},$ $C_{L} = 20 \text{ pF},$	f = B ₁ , See Figure 3	_55°C		52°		1
		OL = 20 pr,	See Figure 3	125°C	14	44°		

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operating characteristics, V_{DD} = 5 V, T_A = 25°C

MM.	1007.	11007.	FOT COMPLETE	NO	10VT	LC272Y	W.T.	
- XIVN	PARAMETER	WWW. C	EST CONDITIC	ONS	MIN	TYP	MAX	UNIT
00	AN John CONT.	$R_{\parallel} = 10 \text{ k}\Omega$	C _L = 20 pF,	V _{IPP} = 1 V	W.To	3.6	Olar.	
SR	Slew rate at unity gain	See Figure 1		V _{IPP} = 2.5 V	ALW.Y	2.9	COM	V/μs
v _n	Equivalent input noise voltage	f = 1 kHz,	$R_S = 20 \Omega$,	See Figure 2	TXX	25	- O1	nV/√ Hz
Вом	Maximum output-swing bandwidth	V _O = V _{OH} , See Figure 1	C _L = 20 pF,	$R_L = 10 \text{ k}\Omega$,		320	*1 CO	kHz
B ₁	Unity-gain bandwidth	V _I = 10 mV,	$C_L = 20 pF$,	See Figure 3	- T	1.7		MHz
φm	Phase margin	V _I = 10 mV, See Figure 3	f = B ₁ ,	C _L = 20 pF,		46°	01.0	OM.T

operating characteristics, V_{DD} = 10 V, T_A = 25°C

	PARAMETER	TEST CO	NDITIONS	TLC	272Y	LINUT
	TANAMETER	I LST CO	NDITIONS	MIN T	YP MAX	UNIT
CD	Clauresta et matical de COM-1	$R_L = 10 \text{ k}\Omega$, $C_L = 2$	20 pF, VIPP = 1 V		5.3	Si.C
SR	Slew rate at unity gain	See Figure 1	V _{IPP} = 5.5 V		4.6	V/µs
٧n	Equivalent input noise voltage	$f = 1 \text{ kHz}, \qquad R_S = 2$	20 Ω, See Figure 2		25	nV/√Hz
ВОМ	Maximum output-swing bandwidth	$V_O = V_{OH}, C_L = 2$ See Figure 1	$R_{L} = 10 \text{ k}\Omega,$	N :	200	kHz
B ₁	Unity-gain bandwidth	$V_{I} = 10 \text{ mV}, C_{L} = 2$	20 pF, See Figure 3	. A.	2.2	MHz
φm	Phase margin	$V_I = 10 \text{ mV}, f = B_1,$ See Figure 3	C _L = 20 pF,	TW	49°	W.10

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PARAMETER MEASUREMENT INFORMATION

single-supply versus split-supply test circuits

Because the TLC272 and TLC277 are optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The use of either circuit gives the same result.

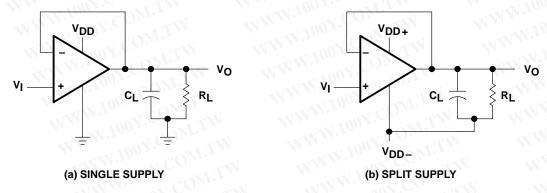


Figure 1. Unity-Gain Amplifier

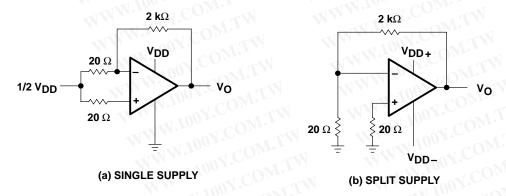


Figure 2. Noise-Test Circuit

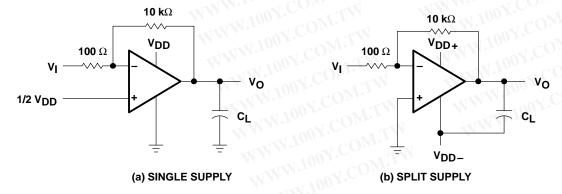


Figure 3. Gain-of-100 Inverting Amplifier



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PARAMETER MEASUREMENT INFORMATION

input bias current

Because of the high input impedance of the TLC272 and TLC277 operational amplifiers, attempts to measure the input bias current can result in erroneous readings. The bias current at normal room ambient temperature is typically less than 1 pA, a value that is easily exceeded by leakages on the test socket. Two suggestions are offered to avoid erroneous measurements:

- 1. Isolate the device from other potential leakage sources. Use a grounded shield around and between the device inputs (see Figure 4). Leakages that would otherwise flow to the inputs are shunted away.
- Compensate for the leakage of the test socket by actually performing an input bias current test (using a picoammeter) with no device in the test socket. The actual input bias current can then be calculated by subtracting the open-socket leakage readings from the readings obtained with a device in the test socket.

One word of caution: many automatic testers as well as some bench-top operational amplifier testers use the servo-loop technique with a resistor in series with the device input to measure the input bias current (the voltage drop across the series resistor is measured and the bias current is calculated). This method requires that a device be inserted into the test socket to obtain a correct reading; therefore, an open-socket reading is not feasible using this method.

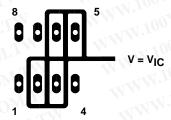


Figure 4. Isolation Metal Around Device Inputs (JG and P packages)

low-level output voltage

To obtain low-supply-voltage operation, some compromise was necessary in the input stage. This compromise results in the device low-level output being dependent on the common-mode input voltage level as well as the differential input voltage level. When attempting to correlate low-level output readings with those quoted in the electrical specifications, these two conditions should be observed. If conditions other than these are to be used, please refer to Figures 14 through 19 in the Typical Characteristics of this data sheet.

input offset voltage temperature coefficient

Erroneous readings often result from attempts to measure temperature coefficient of input offset voltage. This parameter is actually a calculation using input offset voltage measurements obtained at two different temperatures. When one (or both) of the temperatures is below freezing, moisture can collect on both the device and the test socket. This moisture results in leakage and contact resistance, which can cause erroneous input offset voltage readings. The isolation techniques previously mentioned have no effect on the leakage since the moisture also covers the isolation metal itself, thereby rendering it useless. It is suggested that these measurements be performed at temperatures above freezing to minimize error.



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PARAMETER MEASUREMENT INFORMATION

full-power response

Full-power response, the frequency above which the operational amplifier slew rate limits the output voltage swing, is often specified two ways: full-linear response and full-peak response. The full-linear response is generally measured by monitoring the distortion level of the output while increasing the frequency of a sinusoidal input signal until the maximum frequency is found above which the output contains significant distortion. The full-peak response is defined as the maximum output frequency, without regard to distortion, above which full peak-to-peak output swing cannot be maintained.

Because there is no industry-wide accepted value for significant distortion, the full-peak response is specified in this data sheet and is measured using the circuit of Figure 1. The initial setup involves the use of a sinusoidal input to determine the maximum peak-to-peak output of the device (the amplitude of the sinusoidal wave is increased until clipping occurs). The sinusoidal wave is then replaced with a square wave of the same amplitude. The frequency is then increased until the maximum peak-to-peak output can no longer be maintained (Figure 5). A square wave is used to allow a more accurate determination of the point at which the maximum peak-to-peak output is reached.

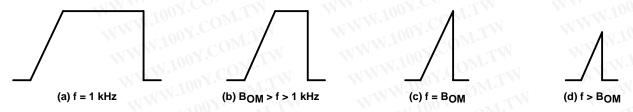


Figure 5. Full-Power-Response Output Signal

test time

Inadequate test time is a frequent problem, especially when testing CMOS devices in a high-volume, short-test-time environment. Internal capacitances are inherently higher in CMOS than in bipolar and BiFET devices and require longer test times than their bipolar and BiFET counterparts. The problem becomes more pronounced with reduced supply levels and lower temperatures.



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TYPICAL CHARACTERISTICS

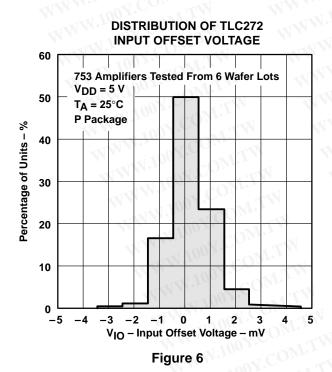
Table of Graphs

-7 (ON. TO COMMITTEE OF COMMITTEE O	ONI.	FIGURE
VIO	Input offset voltage	Distribution	6, 7
ανιο	Temperature coefficient of input offset voltage	Distribution	8, 9
Vон	High-level output voltage	vs High-level output current vs Supply voltage vs Free-air temperature	10, 11 12 13
VoL	Low-level output voltage	vs Common-mode input voltage vs Differential input voltage vs Free-air temperature vs Low-level output current	14, 15 16 17 18, 19
A _{VD}	Large-signal differential voltage amplification	vs Supply voltage vs Free-air temperature vs Frequency	20 21 32, 33
I _{IB}	Input bias current	vs Free-air temperature	22
I _{IO}	Input offset current	vs Free-air temperature	22
VIC	Common-mode input voltage	vs Supply voltage	23
I _{DD}	Supply current	vs Supply voltage vs Free-air temperature	24 25
SR	Slew rate	vs Supply voltage vs Free-air temperature	26 27
	Normalized slew rate	vs Free-air temperature	28
VO(PP)	Maximum peak-to-peak output voltage	vs Frequency	29
B ₁	Unity-gain bandwidth	vs Free-air temperature vs Supply voltage	30 31
φm	Phase margin	vs Supply voltage vs Free-air temperature vs Load capacitance	34 35 36
٧n	Equivalent input noise voltage	vs Frequency	37
	Phase shift	vs Frequency	32, 33

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TYPICAL CHARACTERISTICS



DISTRIBUTION OF TLC272 AND TLC277 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT

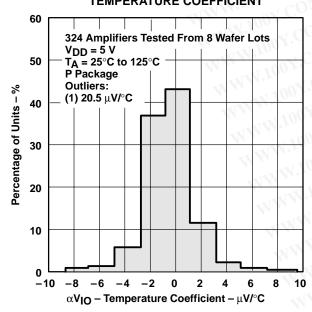


Figure 8

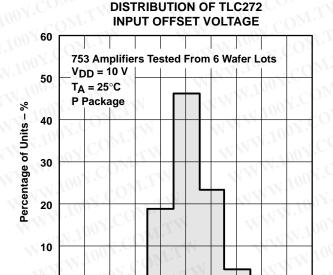


Figure 7

0

VIO - Input Offset Voltage - mV

2 3

DISTRIBUTION OF TLC272 AND TLC277 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT

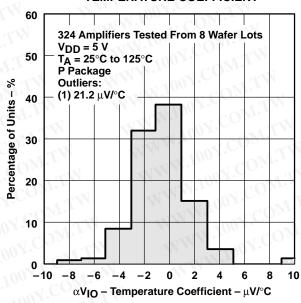
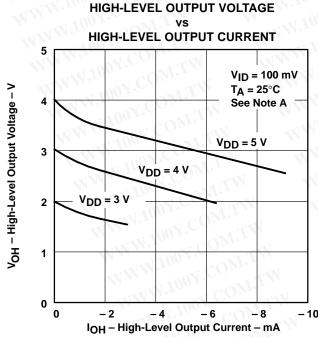


Figure 9

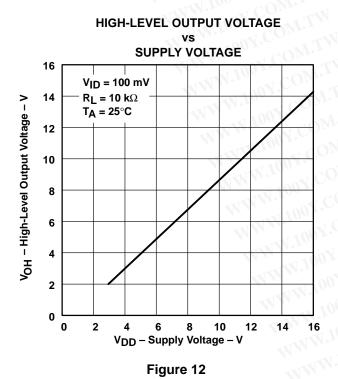
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TYPICAL CHARACTERISTICS†



NOTE A: The 3-V curve only applies to the C version.

Figure 10



HIGH-LEVEL OUTPUT VOLTAGE
VS
HIGH-LEVEL OUTPUT CURRENT

16

V_{ID} = 100 mV
T_A = 25°C

V_{DD} = 16 V

V_{DD} = 10 V

6

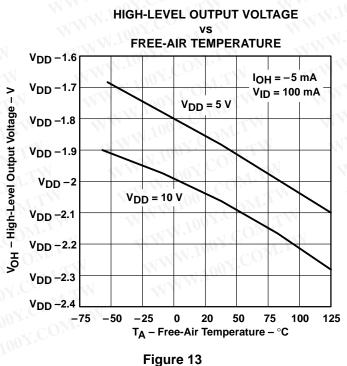
V_{DD} = 10 V

2

Figure 11

-15 -20 -25

IOH – High-Level Output Current – mA

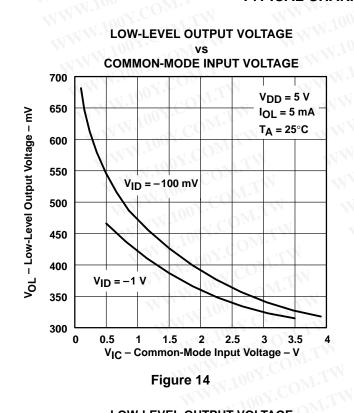


† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

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TYPICAL CHARACTERISTICS[†]



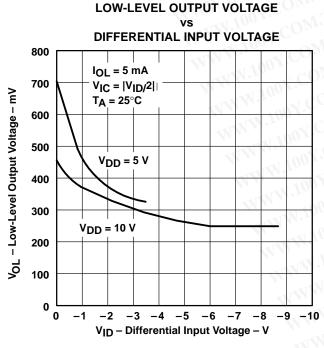


Figure 16

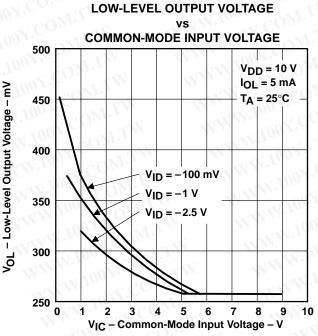
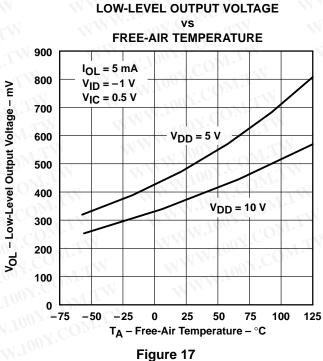


Figure 15



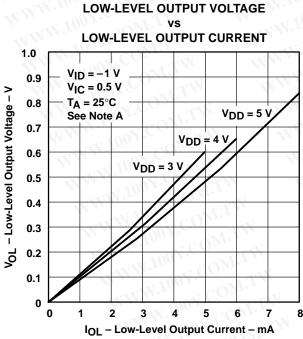
† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.



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LOW-LEVEL OUTPUT VOLTAGE

TYPICAL CHARACTERISTICS[†]



NOTE A: The 3-V curve only applies to the C version. **Figure 18**

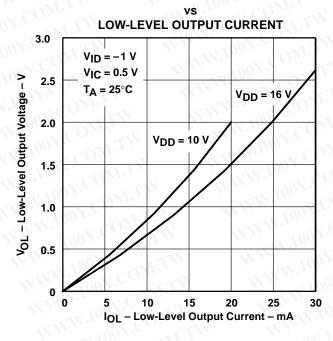
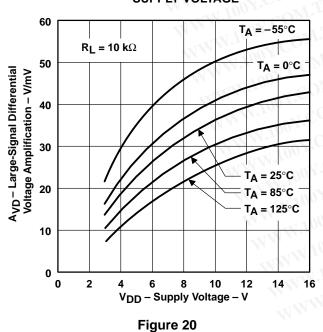


Figure 19

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs SUPPLY VOLTAGE



LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

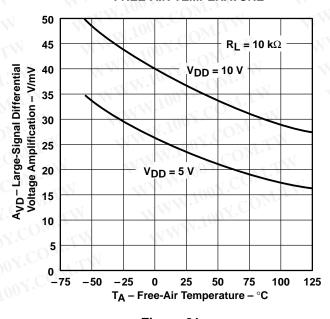


Figure 21

[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

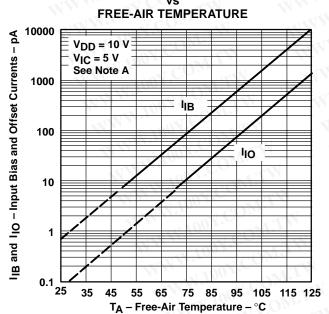


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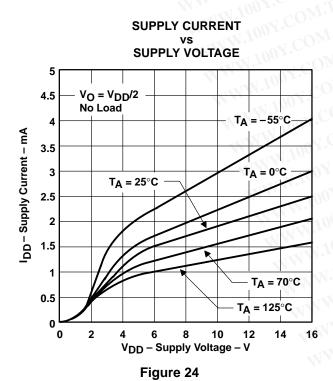
TYPICAL CHARACTERISTICS[†]

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT



NOTE A: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

Figure 22



COMMON-MODE INPUT VOLTAGE POSITIVE LIMIT VS

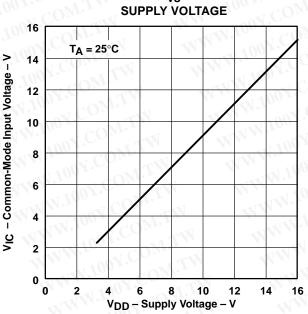


Figure 23

SUPPLY CURRENT vs

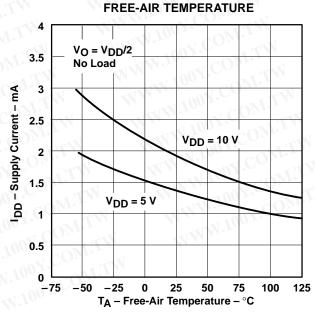


Figure 25

[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.



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TYPICAL CHARACTERISTICS[†]

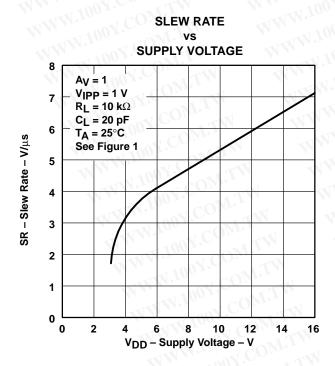
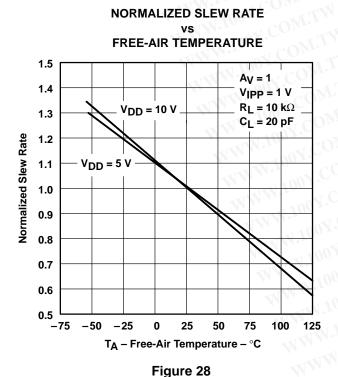
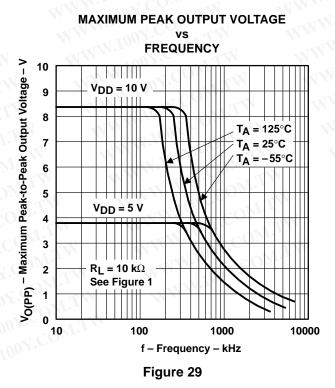


Figure 26



SLEW RATE vs FREE-AIR TEMPERATURE $A_V = 1$ $R_L = 10 k\Omega$ 7 $V_{DD} = 10 V$ $C_L = 20 pF$ V_{IPP} = 5.5 V See Figure 1 6 Rate - V/µs $V_{DD} = 10 V$ 5 $V_{IPP} = 1 V$ 4 - Slew 3 SR $V_{DD} = 5 V$ 2 $V_{IPP} = 1 V$ $V_{DD} = 5 V$ 1 V_{IPP} = 2.5 V 0 -75 -50-25 0 25 50 75 100 T_A - Free-Air Temperature - °C

Figure 27



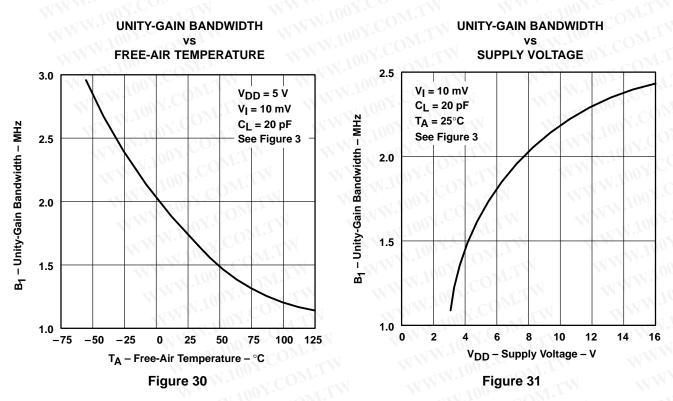
[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.



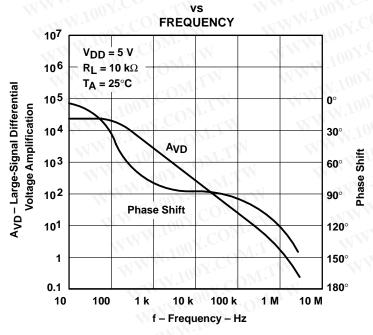
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TYPICAL CHARACTERISTICS[†]



LARGE-SIGNAL DIFFERENTIAL VOLTAGE **AMPLIFICATION AND PHASE SHIFT**



[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.



Figure 32

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TYPICAL CHARACTERISTICS†

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT

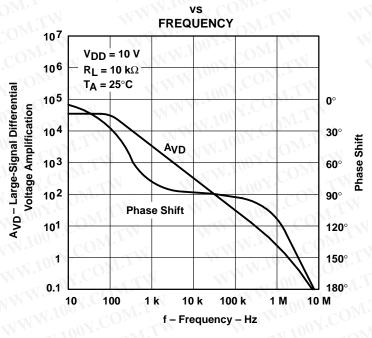
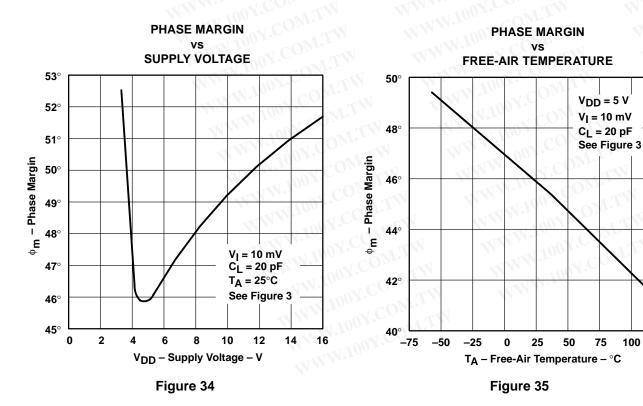


Figure 33



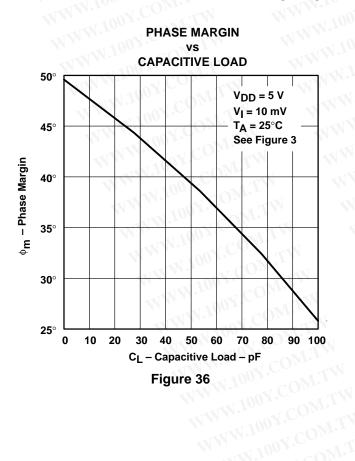
[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

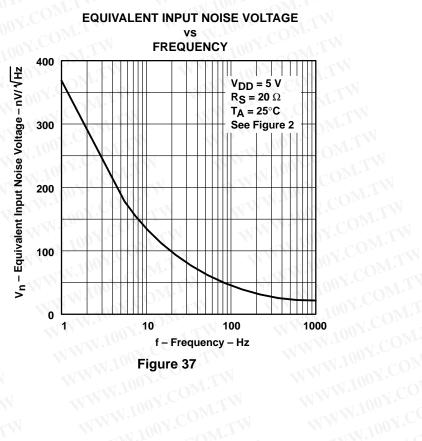


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TYPICAL CHARACTERISTICS





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APPLICATION INFORMATION

single-supply operation

While the TLC272 and TLC277 perform well using dual power supplies (also called balanced or split supplies), the design is optimized for single-supply operation. This design includes an input common-mode voltage range that encompasses ground as well as an output voltage range that pulls down to ground. The supply voltage range extends down to 3 V (C-suffix types), thus allowing operation with supply levels commonly available for TTL and HCMOS; however, for maximum dynamic range, 16-V single-supply operation is recommended.

Many single-supply applications require that a voltage be applied to one input to establish a reference level that is above ground. A resistive voltage divider is usually sufficient to establish this reference level (see Figure 38). The low input bias current of the TLC272 and TLC277 permits the use of very large resistive values to implement the voltage divider, thus minimizing power consumption.

The TLC272 and TLC277 work well in conjunction with digital logic; however, when powering both linear devices and digital logic from the same power supply, the following precautions are recommended:

- Power the linear devices from separate bypassed supply lines (see Figure 39); otherwise, the linear device supply rails can fluctuate due to voltage drops caused by high switching currents in the digital logic.
- 2. Use proper bypass techniques to reduce the probability of noise-induced errors. Single capacitive decoupling is often adequate; however, high-frequency applications may require RC decoupling.

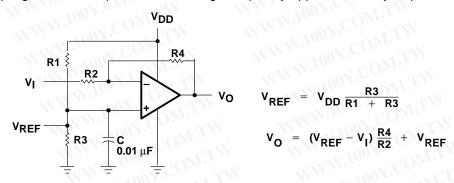


Figure 38. Inverting Amplifier With Voltage Reference

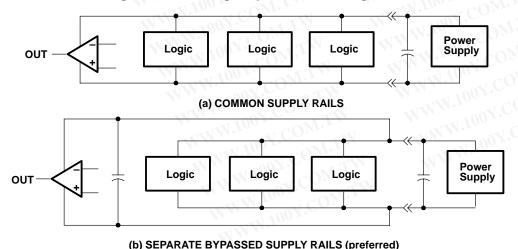


Figure 39. Common vs Separate Supply Rails

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input characteristics

The TLC272 and TLC277 are specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction. Exceeding this specified range is a common problem, especially in single-supply operation. Note that the lower range limit includes the negative rail, while the upper range limit is specified at $V_{DD}-1$ V at $T_A=25^{\circ}$ C and at $V_{DD}-1.5$ V at all other temperatures.

The use of the polysilicon-gate process and the careful input circuit design gives the TLC272 and TLC277 very good input offset voltage drift characteristics relative to conventional metal-gate processes. Offset voltage drift in CMOS devices is highly influenced by threshold voltage shifts caused by polarization of the phosphorus dopant implanted in the oxide. Placing the phosphorus dopant in a conductor (such as a polysilicon gate) alleviates the polarization problem, thus reducing threshold voltage shifts by more than an order of magnitude. The offset voltage drift with time has been calculated to be typically 0.1 μ V/month, including the first month of operation.

Because of the extremely high input impedance and resulting low bias current requirements, the TLC272 and TLC277 are well suited for low-level signal processing; however, leakage currents on printed-circuit boards and sockets can easily exceed bias current requirements and cause a degradation in device performance. It is good practice to include guard rings around inputs (similar to those of Figure 4 in the Parameter Measurement Information section). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input (see Figure 40).

Unused amplifiers should be connected as grounded unity-gain followers to avoid possible oscillation.

noise performance

The noise specifications in operational amplifier circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias current requirements of the TLC272 and TLC277 result in a very low noise current, which is insignificant in most applications. This feature makes the devices especially favorable over bipolar devices when using values of circuit impedance greater than 50 k Ω , since bipolar devices exhibit greater noise currents.

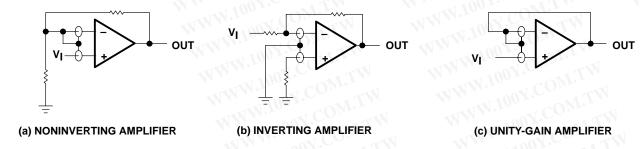


Figure 40. Guard-Ring Schemes

output characteristics

The output stage of the TLC272 and TLC277 is designed to sink and source relatively high amounts of current (see typical characteristics). If the output is subjected to a short-circuit condition, this high current capability can cause device damage under certain conditions. Output current capability increases with supply voltage.

All operating characteristics of the TLC272 and TLC277 are measured using a 20-pF load. The devices can drive higher capacitive loads; however, as output load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation (see Figure 41). In many cases, adding a small amount of resistance in series with the load capacitance alleviates the problem.



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output characteristics (continued)

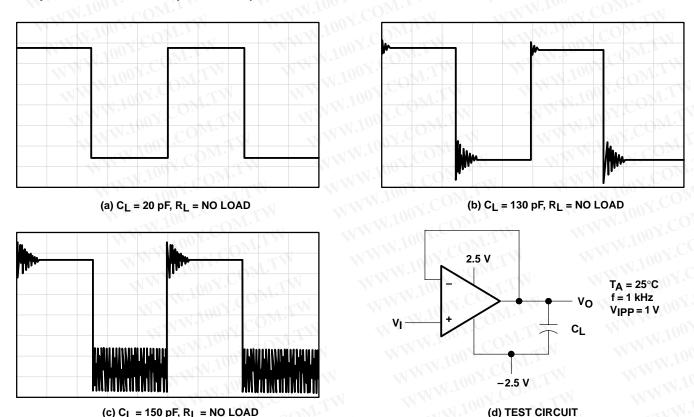


Figure 41. Effect of Capacitive Loads and Test Circuit

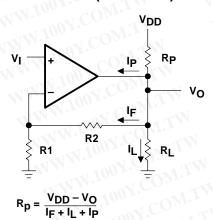
Although the TLC272 and TLC277 possess excellent high-level output voltage and current capability, methods for boosting this capability are available, if needed. The simplest method involves the use of a pullup resistor (Rp) connected from the output to the positive supply rail (see Figure 42). There are two disadvantages to the use of this circuit. First, the NMOS pulldown transistor N4 (see equivalent schematic) must sink a comparatively large amount of current. In this circuit, N4 behaves like a linear resistor with an on resistance between approximately 60 Ω and 180 Ω , depending on how hard the operational amplifier input is driven. With very low values of Rp, a voltage offset from 0 V at the output occurs. Second, pullup resistor Rp acts as a drain load to N4 and the gain of the operational amplifier is reduced at output voltage levels where N5 is not supplying the output current.

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output characteristics (continued)



I_p = Pullup current required by the operational amplifier (typically 500 μA)

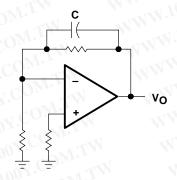


Figure 42. Resistive Pullup to Increase VOH

Figure 43. Compensation for Input Capacitance

feedback

Operational amplifier circuits almost always employ feedback, and since feedback is the first prerequisite for oscillation, some caution is appropriate. Most oscillation problems result from driving capacitive loads (discussed previously) and ignoring stray input capacitance. A small-value capacitor connected in parallel with the feedback resistor is an effective remedy (see Figure 43). The value of this capacitor is optimized empirically.

electrostatic discharge protection

The TLC272 and TLC277 incorporate an internal electrostatic discharge (ESD) protection circuit that prevents functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2. Care should be exercised, however, when handling these devices as exposure to ESD may result in the degradation of the device parametric performance. The protection circuit also causes the input bias currents to be temperature dependent and have the characteristics of a reverse-biased diode.

latch-up

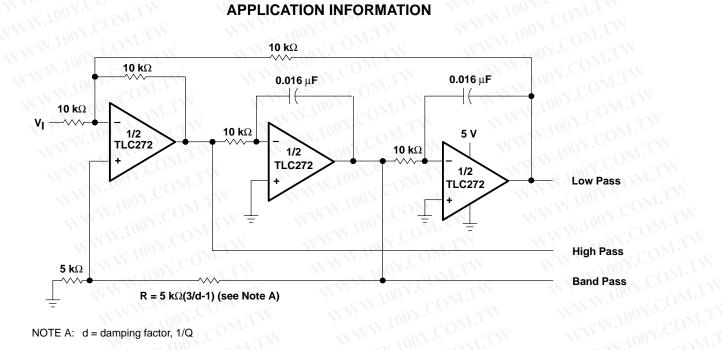
Because CMOS devices are susceptible to latch-up due to their inherent parasitic thyristors, the TLC272 and TLC277 inputs and outputs were designed to withstand -100-mA surge currents without sustaining latch-up; however, techniques should be used to reduce the chance of latch-up whenever possible. Internal protection diodes should not, by design, be forward biased. Applied input and output voltage should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 μ F typical) located across the supply rails as close to the device as possible.

The current path established if latch-up occurs is usually between the positive supply rail and ground and can be triggered by surges on the supply lines and/or voltages on either the output or inputs that exceed the supply voltage. Once latch-up occurs, the current flow is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor and usually results in the destruction of the device. The chance of latch-up occurring increases with increasing temperature and supply voltages.



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NOTE A: d = damping factor, 1/Q

Figure 44. State-Variable Filter

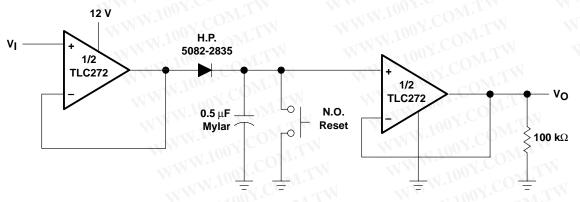
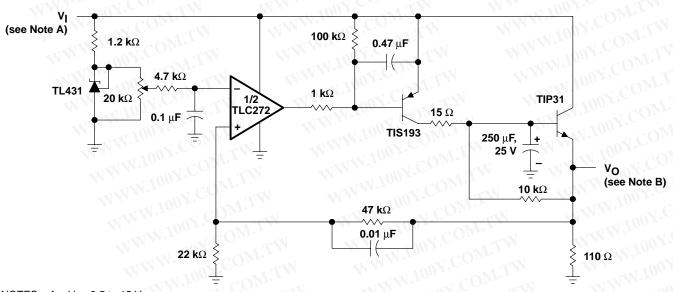


Figure 45. Positive-Peak Detector

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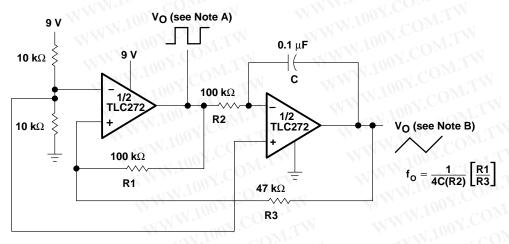
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NOTES: A. $V_I = 3.5 \text{ to } 15 \text{ V}$ B. $V_O = 2 \text{ V}$, 0 to 1 A

Figure 46. Logic-Array Power Supply



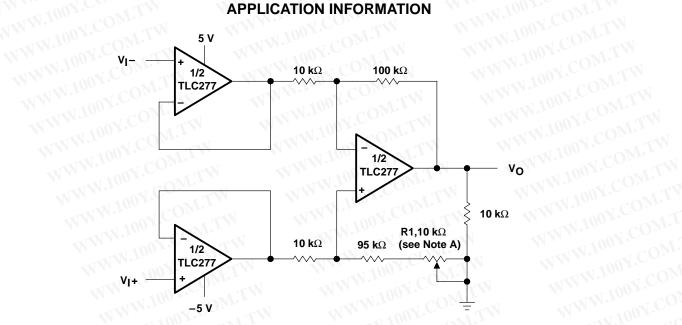
NOTES: A. $V_{O(PP)} = 8 \text{ V}$ B. $V_{O(PP)} = 4 \text{ V}$

Figure 47. Single-Supply Function Generator



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NOTE B: CMRR adjustment must be noninductive.

Figure 48. Low-Power Instrumentation Amplifier

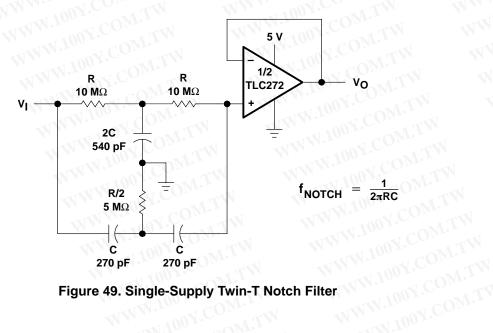


Figure 49. Single-Supply Twin-T Notch Filter

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