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- Trimmed Offset Voltage:
 TLC279...900 μV Max at 25°C, V_{DD} = 5 V
- Input Offset Voltage Drift . . . Typically
 0.1 μV/Month, Including the First 30 Days
- Wide Range of Supply Voltages Over Specified Temperature Range:

0°C to 70°C...3 V to 16 V -40°C to 85°C...4 V to 16 V -55°C to 125°C...4 V to 16 V

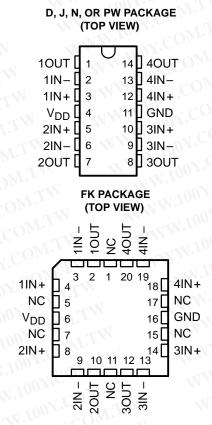
- Single-Supply Operation
- Common-Mode Input Voltage Range Extends Below the Negative Rail (C-Suffix and I-Suffix Versions)
- Low Noise . . . Typically 25 nV/√Hz at f = 1 kHz
- Output Voltage Range Includes Negative Rail
- High Input Impedance . . . 10¹² Ω Typ
- ESD-Protection Circuitry
- Small-Outline Package Option Also Available in Tape and Reel
- Designed-In Latch-Up Immunity

description

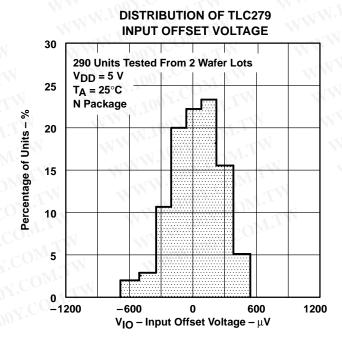
The TLC274 and TLC279 quad operational amplifiers combine a wide range of input offset voltage grades with low offset voltage drift, high input impedance, low noise, and speeds approaching that of general-purpose BiFET devices.

These devices use Texas Instruments silicon-gate LinCMOS™ technology, which provides offset voltage stability far exceeding the stability available with conventional metal-gate processes.

The extremely high input impedance, low bias currents, and high slew rates make these cost-effective devices ideal for applications which have previously been reserved for BiFET and NFET products. Four offset voltage grades are available (C-suffix and I-suffix types), ranging from the low-cost TLC274 (10 μV) to the high-precision TLC279 (900 μV). These advantages, in combination with good common-mode rejection and supply voltage rejection, make these devices a good choice for new state-of-the-art designs as well as for upgrading existing designs.



NC - No internal connection



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description (continued)

In general, many features associated with bipolar technology are available on LinCMOS™ operational amplifiers, without the power penalties of bipolar technology. General applications such as transducer interfacing, analog calculations, amplifier blocks, active filters, and signal buffering are easily designed with the TLC274 and TLC279. The devices also exhibit low voltage single-supply operation, making them ideally suited for remote and inaccessible battery-powered applications. The common-mode input voltage range includes the negative rail.

A wide range of packaging options is available, including small-outline and chip-carrier versions for high-density system applications.

The device inputs and outputs are designed to withstand – 100-mA surge currents without sustaining latch-up.

The TLC274 and TLC279 incorporate internal ESD-protection circuits that prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parametric performance.

The C-suffix devices are characterized for operation from 0° C to 70° C. The I-suffix devices are characterized for operation from -40° C to 85° C. The M-suffix devices are characterized for operation over the full military temperature range of -55° C to 125° C.

AVAILABLE OPTIONS

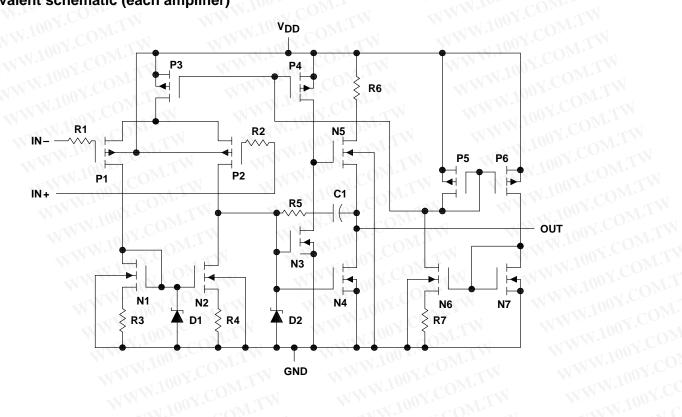
<u> </u>		WY.Co	PA	CKAGED DEV	ICES	TW	CLUD
T _A	V _{IO} max AT 25°C	SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)	TSSOP (PW)	CHIP FORM (Y)
	900 μV	TLC279CD	NI.	- W	TLC279CN) Name	
0°C to 70°C	2 mV	TLC274BCD	7 T		TLC274BCN	$OM^{-\frac{1}{L}}$	<u> </u>
0.0 10 70.0	5 mV	TLC274ACD	DIV. TON		TLC274ACN	W.	-1/1/
	10 mV	TLC274CD	OM-	_	TLC274CN	TLC274CPW	TLC274Y
	900 μV	TLC279ID	TH	- 1	TLC279IN	TH	_ //
-40°C to 85°C	2 mV	TLC274BID	$CO_{\overline{M}_{\bullet}}$		TLC274BIN	CO	- 1
-40 C 10 65 C	5 mV	TLC274AID	- OT	_	TLC274AIN	COA	_
	10 mV	TLC274ID	LCOS AT	$N - \cdot$	TLC274IN	1.0-11	N - 1
–55°C to 125°C	900 μV	TLC279MD	TLC279MFK	TLC279MJ	TLC279MN	ON COM	W -
-55 6 10 125 6	10 mV	TLC274MD	TLC274MFK	TLC274MJ	TLC274MN	OW:	<u> </u>

The D package is available taped and reeled. Add R suffix to the device type (e.g., TLC279CDR).

TLC274, TLC274A, TLC274B, TLC274Y, TLC279 LinCMOS™ PRECISION QUAD OPERATIONAL AMPLIFIERS

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equivalent schematic (each amplifier)

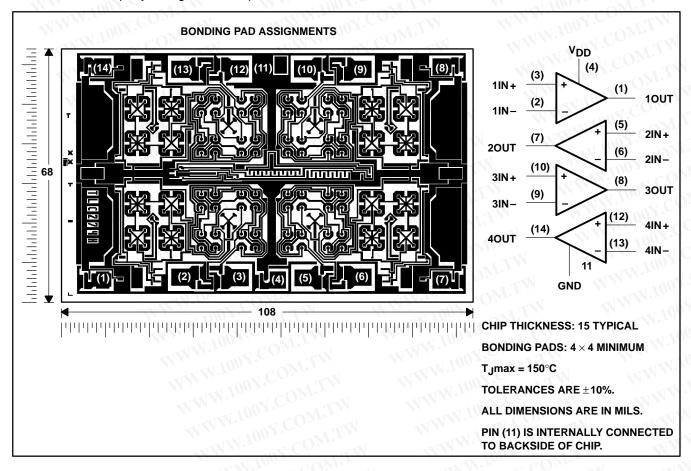


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TLC274Y chip information

These chips, when properly assembled, display characteristics similar to the TLC274C. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

M. S. CO.
±V _{DD}
0.3 V to V _{DD}
±5 mA
±30 mA
45 mA
45 mA
unlimited
. See Dissipation Rating Table
0°C to 70°C
–40°C to 85°C
–55°C to 125°C
–65°C to 150°C
260°C
package 260°C
300°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
 - 2. Differential voltages are at the noninverting input with respect to the inverting input.
 - 3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded (see application section).

DISSIPATION RATING TABLE

PACKAGE	T _A ≤ 25°C POWER RATING	DERATING FACTOR ABOVE T _A = 25°C	T _A = 70°C POWER RATING	T _A = 85°C POWER RATING	T _A = 125°C POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW	UN - W.
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
J	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
N	1575 mW	12.6 mW/°C	1008 mW	819 mW	W. F
PW	700 mW	5.6 mW/°C	448 mW	1007.0	M.TV

recommended operating conditions

Supply voltage, VDD 3 16 4 16 4 16 Common-mode input voltage, VIC VDD = 5 V -0.2 3.5 -0.2 3.5 0 3.5 VDD = 10 V -0.2 8.5 -0.2 8.5 0 8.5		TANN TOO COM.	C SU	FFIX	I SUI	FFIX	M SU	FFIX	LIMIT
Common-mode input voltage, $V_{ C }$			MIN	MAX	MIN	MAX	MIN	MAX	UNIT
Common-mode input voltage, V_{IC} $V_{DD} = 10 \text{ V}$ $-0.2 8.5 -0.2 8.5$	Supply voltage, V _{DD}	WW. 100X.Com.T.	3	16	4	16	4	16	V
$V_{DD} = 10 \text{ V}$ $-0.2 8.5 -0.2 8.5 0 8.5$	Common made input voltage V	V _{DD} = 5 V	-0.2	3.5	-0.2	3.5	0	3.5	V
Operating free-air temperature, TA 0 70 -40 85 -55 125	Common-mode input voltage, VIC	V _{DD} = 10 V	-0.2	8.5	-0.2	8.5	7 (0)	8.5	V
W. W. CON. C. J. J. W. W. COLLEGE	Operating free-air temperature, TA	W. 100 P. COM	0	70	-40	85	-55	125	°C
	Operating free-air temperature, TA	MAM.1007.COM	0	70	-40	85	-55	12	5

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electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

WW	PARAMETER		TEST CON	DITIONS	T _A †	TLC274 TLC274	C, TLC2 IBC, TL		UNIT
			WW.100 -			MIN	TYP	MAX	
W	11007.	TI 00740	V _O = 1.4 V,	V _{IC} = 0,	25°C	-TV 1	1.1	10	T.
		TLC274C	$R_S = 50 \Omega$,	$R_L = 10 \text{ k}\Omega$	Full range	NA .	100%	12	
		TI 007440	V _O = 1.4 V,	V _{IC} = 0,	25°C	MAI	0.9	5	mV
.,	100	TLC274AC	$R_S = 50 \Omega$,	$R_L = 10 \text{ k}\Omega$	Full range	TIN V	.To.	6.5	M.
VIO	Input offset voltage	TI 007 4D0	V _O = 1.4 V,	V _{IC} = 0,	25°C	- 41	340	2000	$M_{i,j}$
		TLC274BC	$R_S = 50 \Omega$,	$R_L = 10 \text{ k}\Omega$	Full range	1/1/1/	-x110	3000	
		TI 00700	V _O = 1.4 V,	V _{IC} = 0,	25°C	WV	320	900	μV
		TLC279C	$R_S = 50 \Omega$,	$R_L = 10 \text{ k}\Omega$	Full range	- 1	WW.	1500	$CO_{\tilde{M}}$
αVIO	Average temperature coe offset voltage	efficient of input	MMA	100 r. CO	25°C to 70°C		1.8	100	μV/°C
	land affect some at (a.e.	Net-CO ^M	V 05V	V OFV	25°C		0.1	N	V.C
liO	Input offset current (see	Note 4)	$V_0 = 2.5 \text{ V},$	$V_{IC} = 2.5 \text{ V}$	70°C		7	300	pA
	Lancet Library Name of Assistant	10%	V 05V	V 105V	25°C		0.6	-TXV.1)0 r.
İΙΒ	Input bias current (see N	ote 4)	$V_0 = 2.5 V$,	$V_{IC} = 2.5 V$	70°C		40	600	pΑ
	Common-mode input vol	tage range	TW V	MMN.100,	25°C	-0.2 to	-0.3 to 4.2	MAA	100
VICR	(see Note 5)	M:100X:CO	M.TW		Full range	-0.2 to 3.5		WW	V
	11.	1001.	ONT	TW.	25°C	3.2	3.8	-1	WW.
Vон	High-level output voltage	1007.	$V_{ID} = 100 \text{ mV},$	$R_L = 10 \text{ k}\Omega$	0°C	3	3.8	W	٧
			COM		70°C	3	3.8		M.
	·	M.In.	COM	WW	25°C	DIA	0	50	WW
VOL	Low-level output voltage		$V_{ID} = -100 \text{ mV},$	$I_{OL} = 0$	0°C	\sim O_{M} .	0	50	mV
			T. W.TW		70°C		0	50	111.
		MMA	MY.CO TY	M.	25°C	5	23		1//
AVD	Large-signal differential vamplification	voltage	$V_0 = 0.25 \text{ V to 2 V},$	$R_L = 10 \text{ k}\Omega$	0°C	(C4	27	N	V/mV
	amplification		100 r. COW.1		70°C	4	20		
		MAL	1007.	L.A.	25°C	65	80	. 41	
CMRR	Common-mode rejection	ratio	V _{IC} = V _{ICR} min		0°C	60	84	TW	dB
		TW.	W. To. COM	TW	70°C	60	85	W	
			W.100 - CO	A. I	25°C	65	95	1.2	
ksvr	Supply-voltage rejection (ΔV _{DD} /ΔV _{IO})	ratio	$V_{DD} = 5 \text{ V to } 10 \text{ V},$	$V_0 = 1.4 \text{ V}$	0°C	60	94	$M_{-L,A}$	dB
	(AADD\AAIQ)		MAN. TOUX.CC		70°C	60	96	TIME	N
		<	UNIV. JUNIO C	OM.	25°C	M	2.7	6.4	
I _{DD}	Supply current (four amp	lifiers)	V _O = 2.5 V, No load	$V_{IC} = 2.5 \text{ V},$	0°C	VW.10	3.1	7.2	mA
			110 1000		70°C		2.3	5.2	

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.



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electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

MM.	PARAMETER	W V	TEST CONI	DITIONS	TAT	TLC274			UNIT
			W.100 r.		1	MIN	TYP	MAX	-XXI
11/1	11007.0	TI 00740	V _O = 1.4 V,	V _{IC} = 0,	25°C	-TXV.1	1.1	10	T
		TLC274C	$R_S = 50 \Omega$,	$R_L = 10 \text{ k}\Omega$	Full range	NY T	1001	12	
		TI 007440	V _O = 1.4 V,	V _{IC} = 0,	√ 25°C √	MAN.	0.9	5	mV
.,	M 1, 100 1.	TLC274AC	$R_S = 50 \Omega$,	$R_L = 10 \text{ k}\Omega$	Full range	TINVI	Ton	6.5	M·
VIO	Input offset voltage	TI 0074D0	V _O = 1.4 V,	V _{IC} = 0,	25°C	- XT	390	2000	Mir
		TLC274BC	$R_S = 50 \Omega$	$R_L = 10 \text{ k}\Omega$	Full range	MA	-x110	3000	
		TLC279C	V _O = 1.4 V,	$V_{IC} = 0$,	25°C	WV	370	1200	μV
		11.02/90	$R_S = 50 \Omega$,	$R_L = 10 \text{ k}\Omega$	Full range	-31	MW.	1900	CO_{N_I}
αVIO	Average temperature co offset voltage	pefficient of input	N WW	N.100 Y.C.	25°C to 70°C		2	100	μV/°C
L	Input offeet ourrent (e.e.	Note 4	V- EV	W. EVV	25°C		0.1	N. P	1 0 C
ΙΟ	Input offset current (see	e Note 4)	V _O =.5 V,	$V_{IC} = 5 V$	70°C		7	300	pΑ
1	lanut bias sumant (sas l		W- FV	Vie LEV	25°C		0.7	-TXV.1)() <u>.</u>
ΙΒ	Input bias current (see I	Note 4)	$V_0 = 5 V$,	$V_{IC} = 5 V$	70°C		50	600	pA
.,	Common-mode input vo	oltage range	N.TW	WWW.100	25°C	-0.2 to 9	-0.3 to 9.2	MAN	1007
VICR	(see Note 5)	N.1009.	OW.TW		Full range	-0.2 to 8.5		WW	V.O
	1/1	1001.	COMITY	NA TOTAL	25°C	8	8.5	-1	L. Win
Vон	High-level output voltag	e	$V_{ID} = 100 \text{ mV},$	$R_L = 10 \text{ k}\Omega$	0°C	7.8	8.5	W	V
0			CONT.	WW	70°C	7.8	8.4		MAIN
		100	COM	W.	25°C	Dir	0 📉	50	OVV
VOL	Low-level output voltage	e W 10	$V_{ID} = -100 \text{ mV},$	$I_{OL} = 0$	0°C	COM.	0	50	mV
			OY.COMITY	N.	70°C	Mo	0	50	1/1/1/
		MMM	on V.Co.	N V	25°C	10	36		
AVD	Large-signal differential	voltage	$V_0 = 1 \text{ V to 6 V},$	$R_L = 10 \text{ k}\Omega$	0°C	7.5	42	N	V/mV
	amplification		100 J. COM.		70°C	7.5	32	-1	
		MAG	1100Y.	IN	25°C	65	85		
CMRR	Common-mode rejectio	n ratio	V _{IC} = V _{ICR} min		0°C	60	88	TW	dB
			M. Inc. COJ		70°C	60	88	W	
		71	M.100	M.I.	25°C	65	95	1.2	ſ
ksvr	Supply-voltage rejection	n ratio	$V_{DD} = 5 \text{ V to } 10 \text{ V},$	$V_0 = 1.4 \text{ V}$	0°C	60	94	$M_{1,1,1}$	dB
	$(\Delta V_{DD}/\Delta V_{IO})$		WW.	TW	70°C	60	96	TIM	N
			MW.In	COMP	25°C	MASSI	3.8	8	
I_{DD}	Supply current (four am	plifiers)	V _O = 5 V, No load	$V_{IC} = 5 V$,	0°C	M. 10	4.5	8.8	mA
			INU IUau		70°C		3.2	6.8	

†Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.



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electrical characteristics at specified free-air temperature, $V_{DD} = 5 \text{ V}$ (unless otherwise noted)

	PARAMETER		TEST CONI	DITIONS	TAT		4I, TLC2 4BI, TL		UNIT
			MW.100		-13	MIN	TYP	MAX	-XXI
W	11007.00	TLC274I	$V_0 = 1.4 \text{ V},$	$V_{IC} = 0$,	25°C	-TXV 1	1.1	10	1.
		11.02/41	$R_S = 50 \Omega$,	$R_L = 10 \text{ k}\Omega$	Full range		OOY.	13	mV
		TI 007441	V _O = 1.4 V,	V _{IC} = 0,	25°C	MW.	0.9	5	IIIV
V	lament offent voltage	TLC274AI	$R_S = 50 \Omega$,	$R_L = 10 \text{ k}\Omega$	Full range		1700.	7	$M_{I,I}$,
VIO	Input offset voltage	TI 0074DI	V _O = 1.4 V,	V _{IC} = 0,	∑ 25°C	MAA.	340	2000	Tim
		TLC274BI	$R_S = 50 \Omega$,	$R_L = 10 \text{ k}\Omega$	Full range	WW	Miss	3500	
		TI 00701	V _O = 1.4 V,	$V_{IC} = 0$,	25°C	- 1	320	900	μV
		TLC279I	$R_S = 50 \Omega$,	$R_L = 10 \text{ k}\Omega$	Full range	M	- XI 1	2000	
αVIO	Average temperature coe offset voltage	fficient of input	WWW	100 A CO.	25°C to 85°C	W	1.8	100 Y	μV/°C
	You.	COTT	V 0.5W	100 251	25°C		0.1	1 100	
ΙO	Input offset current (see N	Note 4)	$V_0 = 2.5 \text{ V},$	$V_{IC} = 2.5 V$	85°C		24	1000	pA
	71,100	· COM.	V 05V	W. Joo	25°C		0.6	11.10	<7.C
ΙΒ	Input bias current (see No	ote 4)	$V_0 = 2.5 \text{ V},$	$V_{IC} = 2.5 V$	85°C		200	2000	pA
	Common-mode input volt	age range	IM MA	MM:100X;	25°C	-0.2 to 4	-0.3 to 4.2	MW.	100
VICR	(see Note 5)	100 Y.COM	TIM I		Full range	-0.2 to 3.5	1	WWW	V
	MAN	TOON CO	TW	11/10	25°C	3.2	3.8	44,44	-x11(
Vон	High-level output voltage		$V_{ID} = 100 \text{ mV},$	$R_L = 10 \text{ k}\Omega$	-40°C	3	3.8	W	V
			PW:		85°C	3	3.8	1	WW.
	W.	1007.	TIME	W.	25°C	$M_{i,I,A}$	0	50	-111
V_{OL}	Low-level output voltage		$V_{ID} = -100 \text{ mV},$	$I_{OL} = 0$	-40°C		0	50	mV
			COM.		85°C	Diar.	0	50	ww.
		100	TOW.I'M	_1	25°C	5	23		-41
AVD	Large-signal differential v amplification	oitage	$V_0 = 0.25 \text{ V to 2 V},$	$R_L = 10 \text{ k}\Omega$	−40°C	3.5	32		V/mV
	amplinoation		Ly CONT.		85°C	3.5	19		W
		W.11	D. CON'I	7	25°C	65	80	« 1	
CMRR	Common-mode rejection	ratio	V _{IC} = V _{ICR} min		−40°C	60	81	la la	dB
		WWW.	LON.COM.	V v	85°C	60	86	V	4
	Occupation of the state of the	W	Tan COM:	-31	25°C	65	95	- CA	
ksvr	Supply-voltage rejection (ΔVDD/ΔVIO)	atio	$V_{DD} = 5 \text{ V to } 10 \text{ V},$	$V_0 = 1.4 \text{ V}$	-40°C	60	92	11.	dB
	(¬,00,¬,10)		A. CON.		85°C	60	96	WIL	
		-133	Wa DEVICON	V.= \0.5 V	25°C		2.7	6.4	
I_{DD}	Supply current (four ampl	ifiers)	V _O = 2.5 V, No load	$V_{IC} = 2.5 V,$	−40°C	1.100	3.8	8.8	mA
			A. A. Long		85°C	400	2.1	4.8	W

[†] Full range is –40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

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electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

	PARAMETER	W I	TEST CON	DITIONS	TAT		4I, TLC2 4BI, TL		UNIT
M.			WW.100 12 C			MIN	TYP	MAX	
1/1	71100Y.C 311.T	TI 00741	V _O = 1.4 V,	V _{IC} = 0,	25°C	-TXV.1	1.1	10	1.4
W		TLC274I	$R_S = 50 \Omega$,	$R_L = 10 \text{ k}\Omega$	Full range	NY T	100X	13	
		7,00744	V _O = 1.4 V,	V _{IC} = 0,	25°C	MAA	0.9	5	mV
	N 100 1. COM	TLC274AI	$R_S = 50 \Omega$	$R_L = 10 \text{ k}\Omega$	Full range	TINY	To.	7 (7)	M· -
VIO	Input offset voltage	TI 007 (D)	V _O = 1.4 V,	V _{IC} = 0,	25°C	- T	390	2000	Mir
		TLC274BI	$R_S = 50 \Omega$	$R_L = 10 \text{ k}\Omega$	Full range	MA	-x110	3500	- A.I
		TI C0701	V _O = 1.4 V,	$V_{IC} = 0$,	25°C	WV	370	1200	μV
		TLC279I	$R_S = 50 \Omega$,	$R_L = 10 \text{ k}\Omega$	Full range		WW.	2900	CO_{DJ}
αVIO	Average temperature coeff offset voltage	icient of input	WWW.	100 Y. CO.	25°C to 85°C		2	100	μV/°C
I	Input offeet ourrent (eee No	46 (10 N)	N- EV	VI OF VCC	25°C		0.1	1.5	120
IIO	Input offset current (see No	ne 4)	$V_0 = 5 V$,	$V_{IC} = 5 V$	85°C		26	1000	pΑ
1	lanut hian aumant (ann Nat		W- 5V	-V/-10EV	25°C		0.7	-1XV.1	20 z.
IB	Input bias current (see Not	e 4)	$V_O = 5 V$	$V_{IC} = 5 V$	85°C		220	2000	pA
	Common-mode input volta	ge range	IN W	MM.TOOA	25°C	-0.2 to 9	-0.3 to 9.2		100 ^X
VICR	(see Note 5)	N.100Y.CO	M.TW		Full range	-0.2 to 8.5		WW	VO
	W.	W.100 F.	OM	WW.	25°C	8	8.5	- 1	WW.
Vон	High-level output voltage		$V_{ID} = 100 \text{ mV},$	$R_L = 10 \text{ k}\Omega$	-40°C	7.8	8.5	NA.	V
			COM		85°C	7.8	8.5		M. I.
		WW. To	COM	WW	25°C	Oh.	0	50	WW
VOL	Low-level output voltage		$V_{ID} = -100 \text{ mV},$	$I_{OL} = 0$	-40°C	OM.	0	50	mV
		WW 100	T.OM.TW		85°C	MOD	0	50	W.
		M.M.	Y.Co. TW	W	25°C	10	36		4/1/
AVD	Large-signal differential vol amplification	tage	$V_0 = 1 \text{ V to 6 V},$	$R_L = 10 \text{ k}\Omega$	-40°C	(C7)	47	N	V/mV
	amplification		Mir. COWIT.	×1	85°C	70	31	- XX	
		WW	T.MO.	//	25°C	65	85		
CMRR	Common-mode rejection ra	atio	V _{IC} = V _{ICR} min		-40°C	60	87		dB
		-XIXV	M. To. COM.		85°C	60	88		
	•	, «X	W.Ing COM	. 1	25°C	65	95	1	
ksvR	Supply-voltage rejection ra (ΔV _{DD} /ΔV _{IO})	tio	$V_{DD} = 5 \text{ V to } 10 \text{ V},$	$V_0 = 1.4 \text{ V}$	−40°C	60	92	Mir	dB
	_ \U\'\ \U\'\ \U\'\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\	W	A A CO.	WTI	85°C	60	96	Time	
		<1	JNN. J. CC)IA.	25°C	NV	3.8	8	
I_{DD}	Supply current (four amplif	ers)	V _O = 5 V, No load	$V_{IC} = 5 V$	−40°C	M. Le	5.5	10	mA
			THO IOUG		85°C		2.9	6.4	

[†]Full range is –40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.



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electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

MM.	1007 200 1007	4/1/	TEST CON	NTIONO.	1	TLC27	4M, TLC	279M	LINUT
	PARAMETER		TEST CONI	DITIONS	T _A †	MIN	TYP	MAX	UNIT
-73	M.In. COM.	TI 0074M	V _O = 1.4 V,	V _{IC} = 0,	25°C	Mir	1.1	10	
. 11	-11110	TLC274M	$R_S = 50 \Omega$,	$R_L = 10 \text{ k}\Omega$	Full range	MW.T	JU -1	12	mV
VIO	Input offset voltage	TI 007014	V _O = 1.4 V,	V _{IC} = 0,	25°C	-TXN	320	900	LIN
	MM. To ON COM.	TLC279M	$R_S = 50 \Omega$,	$R_L = 10 \text{ k}\Omega$	Full range		1005	3750	μV
αΛΙΟ	Average temperature coefficient offset voltage	t of input	MMM.100	Z.CON.T	25°C to 125°C	NW	2.1	N.CO	μV/°C
li a	Input offset surrent (see Note 4)	TW	V- 25V	V:- 25V	25°C	11/4	0.1	O.F.	pA
liO	Input offset current (see Note 4)	TV	$V_0 = 2.5 \text{ V},$	V _{IC} = 2.5 V	125°C	WV	1.4	15	nA
1	Input bigg gurrant (age Note 4)	1.1	V- 25V	V-5 2.5 V	25°C	- N	0.6		pA
IB	Input bias current (see Note 4)	MTW	$V_0 = 2.5 \text{ V},$	$V_{IC} = 2.5 V$	125°C	4.	9	35	nA
.,	Common-mode input voltage ra	nge	MMA	100X.CC	25°C	0 to 4	-0.3 to 4.2	N.100	V.V.O
VICR	(see Note 5)	COM.T	N WW		Full range	0 to 3.5	WW	NW.1	00 V
	VI 1001	· · · · ·	7	-111.100 X	25°C	3.2	3.8	W.	100
Vон	High-level output voltage		V _{ID} = 100 mV,	$R_L = 10 \text{ k}\Omega$	−55°C	3	3.8		V
			WW V		125°C	3	3.8	MAN	- 100
	W.10	-1 CON	1.2	TWW.10	25°C		0	50	M . >
V_{OL}	Low-level output voltage		$V_{ID} = -100 \text{ mV},$	$I_{OL} = 0$	−55°C		0	50	mV
			WIN	MM	125°C	1.1.11	0	50	-wi 1
	MMM.	ON.C	On TW	MM	25°C	5	23	V	N.
A_{VD}	Large-signal differential voltage amplification		$V_0 = 0.25 \text{ V to 2 V},$	$R_L = 10 \text{ k}\Omega$	−55°C	3.5	35	<	V/mV
	amplification		COMITY		125°C	3.5	16		TINV
	MA	100Y	TI	M. A.	25°C	65	80		NA .
CMRR	Common-mode rejection ratio		$V_{IC} = V_{ICR}min$		−55°C	60	81		dB
			A COMP.		125°C	60	84		W
	A.	W.10	COM	7	25°C	65	95	«1	- 1
ksvr	Supply-voltage rejection ratio (Δ	V _{DD} /ΔV _{IO})	$V_{DD} = 5 \text{ V to } 10 \text{ V},$	V _O = 1.4 V	−55°C	60	90		dB
			ONY.COM		125°C	60	97		
			To COM.		25°C	OV.C	2.7	6.4	
I_{DD}	Supply current (four amplifiers)		V _O = 2.5 V, No load	$V_{IC} = 2.5 V,$	−55°C	4 7 (4	10	mA
			140 loau		125°C	100 r.	1.9	4.4	

† Full range is -55° C to 125° C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

5. This range also applies to each input individually. WWW.100Y.COM.TW

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electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless) otherwise noted)

MM	DADAMETED		TEST CON	DITIONS	_ +	TLC27	4M, TLC	279M	UNIT
WW	PARAMETER	N N	TEST CON	DITIONS	TAT	MIN	TYP	MAX	UNII
-11	M.Ing COM.	TLC274M	V _O = 1.4 V,	V _{IC} = 0,	25°C	111.5	1.1	10	mV
V	Input offset voltage	TLC274W	$R_S = 50 \Omega$,	$R_L = 10 \text{ k}\Omega$	Full range	I^{-1}	V	12	IIIV
VIO	input offset voltage	TLC279M	V _O = 1.4 V,	V _{IC} = 0,	25°C	-1XN	370	1200	
	MAN. TOW. COM.	TLC279IVI	$R_S = 50 \Omega$,	$R_L = 10 \text{ k}\Omega$	Full range		1005	4300	μV
αΛΙΟ	Average temperature coe offset voltage	fficient of input	WWW.100	Y.COM.T	25°C to 125°C	WWV	2.2	X.Co	μV/°C
li o	Input offset current (see N	loto (1)	V _O = 5 V,	V _{IC} = 5 V	25°C	11 44	0.1	01.0	pA
ΙO	input onset current (see i	vote 4)	VO = 2V	AIC = 2 A	125°C	WV	1.8	15	nA
l	Input bias current (see No	2to 4)	V _O = 5 V,	V. Z LEV	25°C	**************************************	0.7	V	pA
IВ	input bias current (see No	ne 4)	ν _O = 5 ν,	$V_{IC} = 5 V$	125°C		10	35	nA
\\	Common-mode input volt	age range	MMA	V.100Y.CC	25°C	0 to 9	-0.3 to 9.2	N.100	V.V.C
VICR	(see Note 5)	OY.COM.T	WW WW		Full range	0 to 8.5	WW	1.77	00 V
	WW.	On TOW.	14.	W.100	25°C	8	8.5	W.	In.
Vон	High-level output voltage		$V_{ID} = 100 \text{ mV},$	$R_L = 10 \text{ k}\Omega$	−55°C	7.8	8.5	1	V
			TW		125°C	7.8	8.4	MAG	100
	TAX Y	Airas - CO	NI. Z	-TINN.IO	25°C		0	50	M.
V_{OL}	Low-level output voltage		$V_{ID} = -100 \text{ mV},$	$I_{OL} = 0$	−55°C	. 1	0	50	mV
			WIN		125°C	1.1.11	0	50	-TXV .3
	W	N. W. COX.C	TW	MM	25°C	10	36		M.
A_{VD}	Large-signal differential ve amplification	oltage	$V_0 = 1 \text{ V to 6 V},$	$R_L = 10 \text{ k}\Omega$	−55°C	7	50	<	V/mV
	amplification		COMIT		125°C	7	27		TIN V
		100	TIME	W.	25°C	65	85		T
CMRR	Common-mode rejection	ratio	$V_{IC} = V_{ICR}min$		−55°C	60	87		dB
			COM		125°C	60	86		
		W.11	OM.I.	-1	25°C	65	95	\$ 1	
ksvr	Supply-voltage rejection r (ΔV _{DD} /ΔV _{IO})	atio	$V_{DD} = 5 \text{ V to } 10 \text{ V},$	V _O = 1.4 V	−55°C	60	90		dB
	(7 A DD) 7 A IQ)	MMM.	LOOY.CUM. T	W	125°C	60	97		1
		WWW	To COM.	- XX	25°C	OV.C	3.8	8	
I_{DD}	Supply current (four ampl	ifiers)	V _O = 5 V, No load	$V_{IC} = 5 V$	−55°C	V V × 1 (6.0	12	mA
			140 load		125°C	100 r.	2.5	5.6	

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

5. This range also applies to each input individually. WWW.100Y.COM.TW

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operating characteristics at specified free-air temperature, V_{DD} = 5 V

MA	PARAMETER	TEST C	ONDITIONS	тд		C274A	,	UNIT
		WW. 100X.		V	MIN	TYP	MAX	TW
	M. In COM.	WW.I	COM	25°C		3.6	Co_{r}	W
		1 100 x	$V_{IPP} = 1 V$	0°C	TAT VI	4	-1 CO	M.r.
CD.	Silan are artificial and	$R_L = 10 \Omega$,	70°C	MA	N TYP MAX 3.6 4 3 2.9 3.1 2.5 25 n 320 340 260 1.7	100		
SR	Slew rate at unity gain	C _L = 20 pF, See Figure 1	O.CO.	25°C	WW	MIN TYP MAX 3.6 4 3 2.9 3.1 2.5 25 n 320 340 260 1.7 2 1.3		V/μs
		33N.10	$V_{IPP} = 2.5 V$	0°C		3.1	- - 1 (OM.
		MM.	ON.T	70°C	NA.	2.5	00 r.	OM
٧n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	$R_S = 20 \Omega$,	25°C	W	25	100X	nV/√ Hz
	WW. 100Y.Co. ITW	Al Ar	100 X.	25°C		320	1.100	
Вом	Maximum output-swing bandwidth	VO = VOH,	C _L = 20 pF, See Figure 1	0°C		340	- 40	kHz
		$R_L = 10 \text{ k}\Omega$	See Figure 1	70°C	1	260	11.2	~ CO
	W 11007.0 M.T.		1001	25°C	1	1.7	LVV.1	10 >
B ₁	Unity-gain bandwidth	V _I = 10 mV, See Figure 3	$C_L = 20 pF$,	0°C		2	0 kHz	MHz
		See Figure 3		70°C	N	1.3	MAA.	N.Vac
	M. 1001. ONL.	10	100	25°C	- 1	46°	V	Too
φm	Phase margin	$V_{I} = 10 \text{ mV},$ $C_{L} = 20 \text{ pF},$	= 10 mV, f = B ₁ , 25°C 46°	M 4	1 100 X			
		10L = 20 Pi,		70°C	TV	44°	WW	W

operating characteristics at specified free-air temperature, V_{DD} = 10 V

	PARAMETER	TEST C	TA	TLC274 TL TLC274	UNIT		
		WT		OOY.	MIN	TYP MAX	MM
	W. IV	COM.	WWW	25°C	$C_{O_{2i}}$	5.3	WW
		OWITH	V _{IPP} = 1 V	0°C	COM	5.9	
CD	Class note at smith main	$R_L = 10 \Omega$	MAN	70°C		4.3	\//
SR	Slew rate at unity gain	C _L = 20 pF, See Figure 1	I WIN	25°C	V.Co.	4.6	V/μs
		COMP	V _{IPP} = 5.5 V	0°C	-1 CO	5.1	1
		WY. CONT. T		70°C	00 7.	3.8	
٧n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	$R_S = 20 \Omega$	25°C	100Y.C	25	nV/√Hz
	Mari	1007.	1111	25°C	100 1.	200	
Вом	Maximum output-swing bandwidth	VO = VOH,	C _L = 20 pF,	0°C	1001	220	kHz
		$R_L = 10 \text{ k}\Omega$	See Figure 1	70°C	11.70	140	X
	Mar	11001.	W.I.M	25°C	N 100	2.2	
B ₁	Unity-gain bandwidth	V _I = 10 mV, See Figure 3	$C_L = 20 PF$	0°C	10	2.5	MHz
		See Figure 3		70°C	MAIN	1.8	1
	44	100 E	OMIT	25°C	TIVI.	49°	
φm	Phase margin	$V_{I} = 10 \text{ mV},$ $C_{L} = 20 \text{ pF},$	f = B ₁ , See Figure 3	0°C		50°	1
		OL - 20 PI,	Gee Figure 3	70°C		46°	1

TLC274, TLC274A, TLC274B, TLC274Y, TLC279 LinCMOS™ PRECISION QUAD OPERATIONAL AMPLIFIERS

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operating characteristics at specified free-air temperature, $V_{DD} = 5 \text{ V}$

WW	PARAMETER	TEST C	ONDITIONS	TA		4I, TLC2 4BI, TL		UNIT
4// /		M.100 1.			MIN	TYP	MAX	T XXI
W	1100Y.C. TI.TW	11 11 100	T.M.T.W	25°C	TXN	3.6	401	
		MANA	V _{IPP} = 1 V	-40°C √		4.5		MILIN
CD		$R_L = 10 \text{ k}\Omega$	OV.CONI.	85°C	MW	2.8	V.CU	1///10
SR	Slew rate at unity gain	C _L = 20 pF, See Figure 1	COM	25°C	TXV.	2.9	- 1 C	V/μs
		OOY.COM.TW WWW.1	V _{IPP} = 2.5 V	-40°C	NA.	3.5	N F.	OM_{II}
			100Y.CO	85°C	1/1/1	2.3	001.	T.Ma
Vn	Equivalent input noise voltage	f = 1 kHz, See Figure 2	$R_S = 20 \Omega$,	25°C	W	25	100X	nV/√ Hz
	WWW. LOOY.CO. TW	MA	1100 Y.	25°C		320	si 100	
Вом	Maximum output-swing bandwidth	$V_O = V_{OH}$, $R_L = 10 \text{ k}\Omega$,	C _L = 20 pF, See Figure 1	-40°C		380	- 10	kHz
		KL = 10 KS2,	See Figure 1	85°C		250	11.10	ON CO
	M. 1003.		100	25°C		1.7	1.1	-7 C
B ₁	Unity-gain bandwidth	V _I = 10 mV, See Figure 3	$C_L = 20 pF$,	-40°C		2.6	-31	MHz
		See Figure 3		85°C		1.2	M. A.	TOOY.
	M. Ina . CON	1.1	MW.In	25°C	XX	46°	NWV	· V
ϕ_{m}	Phase margin	$V_{I} = 10 \text{ mV},$ $C_{L} = 20 \text{ pF},$	f = B ₁ , See Figure 3	-40°C		49°		N.100
		OL = 20 PF,	See Figure 3	85°C	1711	43°	M.	100

operating characteristics at specified free-air temperature, V_{DD} = 10 V

			TLC274I, TLC274AI, TLC274BI, TLC279I		UNIT			
		COM	WWW	LOOY.C	MIN	TYP	MAX	
	W.100	CONL	Wir	25°C	CO_{Mr}	5.3		WW
		TOMITW	V _{IPP} = 1 V	-40°C	COM	6.7		
CD	Clausete et units en la	$R_L = 10 \Omega$		85°C		4		Miss
SR	Slew rate at unity gain	C _L = 20 pF, See Figure 1	W W	25°C	M.Co.	4.6		V/μs
		(O)	V _{IPP} = 5.5 V	-40°C	√ CO	5.8	XX	
		1007.	May 1	85°C	00 -	3.5	- 1	
٧n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	$R_S = 20 \Omega$,	25°C	1001.	25	TW	nV/√Hz
		VI.100	Mir	25°C	In	200	10.2	ſ
Вом	Maximum output-swing bandwidth	$V_O = V_{OH}$, $R_L = 10 \text{ k}\Omega$,	C _L = 20 pF, See Figure 1	-40°C	11.100	260	M: I	kHz
		KL = 10 KS2,	See Figure 1	85°C	100	130	TI	
	-31	M. In C	Olyn.	25°C	1111	2.2	7112	
B ₁	Unity-gain bandwidth	V _I = 10 mV, See Figure 3	$C_L = 20 pF$,	-40°C	M.In	3.1	O_{M} .	MHz
		See Figure 3		85°C	-TXV.1	1.7		
		1007	V.CO.	25°C \	14.	49°		
ϕ_{m}	Phase margin	$V_{I} = 10 \text{ mV},$ $C_{L} = 20 \text{ pF},$	f = B ₁ , See Figure 3	-40°C		52°		
		GL = 20 PF,	See Figure 3	85°C		46°		

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operating characteristics at specified free-air temperature, V_{DD} = 5 V

WW	N TON	1202	OUDITIONS.		TLC274	4M, TLC	279M	
	PARAMETER	IESIC	ONDITIONS	TA	MIN	TYP	MAX	UNIT
41	M. Too COM.	WW.Ioo	COMP.	25°C	MM.T	3.6	$\mathbb{C}_{\mathbf{O}_{M_{\mathbf{r}}}}$	TIN
		V 1, 100	V _{IPP} = 1 V	−55°C	WIW.	4.7	COD	
CD V	MAN CONTRACTOR	$R_L = 10 \text{ k}\Omega$	T.M.TW	125°C	N TO	2.3		1
SR	Slew rate at unity gain	C _L = 20 pF, See Figure 1	N.CO.	25°C	MAL	2.9	Y.C.	V/μs
		GGG T Iguiro	V _{IPP} = 2.5 V	-55°C		3.7	N.C	DIAT.
		W TIN !	$G_{0,T}$	125°C		2	-1($O_{M',r}$
٧n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	$R_S = 20 \Omega$,	25°C	W	25	001 001	nV/√ Hz
	M. 100		N.Jan. CON	25°C		320	100	
Вом	Maximum output-swing bandwidth	$V_O = V_{OH}$, $R_L = 10 \text{ k}\Omega$,	C _L = 20 pF, See Figure 1	−55°C		400	V.100	kHz
		K_ = 10 K12,	See Figure 1	125°C		230	×110	N.Co
	MAN. TO TO COM.	N W	WW.	25°C		1.7	Air	ny.Co
В ₁	Unity-gain bandwidth	V _I = 10 mV, See Figure 3	$C_L = 20 pF$,	−55°C		2.9	1111.7	MHz
		See Figure 3		125°C		1.1	www.	1001.
	MAN OON CO.	TW	M M 1007	25°C	W	46°	A	1007.
φm	Phase margin	$V_{I} = 10 \text{ mV},$	$f = B_1$	−55°C	TV	49°	MIN	You
		$C_L = 20 pF$,	See Figure 3	125°C	- 1	41°		N'Jan

operating characteristics at specified free-air temperature, V_{DD} = 10 V

	DADAMETED ON C	TTOT O	ONDITIONS	hor.	TLC27	4M, TLC	279M	
	PARAMETER	TEST C	ONDITIONS	TA	MIN	TYP	MAX	UNIT
	W. 100 x.	dOM:	VIV	25°C	OM	5.3		
		WI.M.	V _{IPP} = 1 V	−55°C	Low	7.1		
SR	Claw rate at unity rain	$R_L = 10 \Omega$,	WW.	125°C		3.1		1////
SK	Slew rate at unity gain	C _L = 20 pF, See Figure 1	N W	25°C	$^{1}CO_{M}$	4.6		V/μs
		OMIT	V _{IPP} = 5.5 V	−55°C	7.00	6.1	\$ 1	
	WW	ODY. COM. T	M. M.	125°C		2.7		
٧n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	$R_S = 20 \Omega$,	25°C	10 Y.C.	25		nV/√H:
	W	1001.	1.1.11	25°C	100.	200	11.	
Вом	Wayimum output-swing bandwidth Vo = VoH, CL = 20 pF,	100 X.	280	IIN	kHz			
		$R_L = 10 \text{ k}\Omega$	See Figure 1	125°C	· ooy	110	TV	
	7	M. M. Too	OM.	25°C	N.Io.	2.2	Mr.	N
B ₁	Unity-gain bandwidth	V _I = 10 mV, See Figure 3	$C_L = 20 pF$,	−55°C	W.100	3.4	Mi	MHz
		See rigule 3	$V_{IPP} = 5.5 \text{ V}$ $R_S = 20 \Omega$, $C_L = 20 \text{ pF}$,	125°C	10	1.6	.Mo	
	4	NWW.	CONTRACTOR	25°C	M.A.	49°		
φm	Phase margin	$V_{I} = 10 \text{ mV},$ $C_{L} = 20 \text{ pF},$	f = B ₁ , See Figure 3	−55°C	INW.	52°		
		OL = 20 pr,	Occ riguic o	125°C		44°		

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electrical characteristics, $V_{DD} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$ (unless otherwise noted)

MM	DAD THEFT	TEST SOLU	DITIONS	100	LC274Y	MIL	LINUT
	PARAMETER	TEST CON	DITIONS	MIN	TYP	MAX	UNIT
V _{IO}	Input offset voltage	$V_{O} = 1.4 \text{ V},$ R _S = 50 Ω ,	$V_{IC} = 0,$ $R_L = 10 \text{ k}\Omega$	W. 1	001.1	10	mV
lo 📢	Input offset current (see Note 4)	$V_0 = 2.5 \text{ V},$	V _{IC} = 2.5 V	- XI	0.1	.01	pA
I _{IB}	Input bias current (see Note 4)	$V_0 = 2.5 V$,	V _{IC} = 2.5 V		0.6	Co.	pA
VICR	Common-mode input voltage range (see Note 5)	MAN TOON COM	TW	-0.2 to 4	-0.3 to 4.2	VY.CO	V
Vон	High-level output voltage	V _{ID} = 100 mV,	R _L = 10 kΩ	3.2	3.8	- ▼ 1 (V
VOL	Low-level output voltage	$V_{ID} = -100 \text{ mV},$	I _{OL} = 0		0	50	mV
AVD	Large-signal differential voltage amplification	$V_0 = 0.25 \text{ V to 2 V},$	R _L = 10 kΩ	5	23	1007	V/mV
CMRR	Common-mode rejection ratio	V _{IC} = V _{ICR} min	OM	65	80		dB
ksvr	Supply-voltage rejection ratio (ΔV _{DD} /ΔV _{IO})	$V_{DD} = 5 \text{ V to } 10 \text{ V},$	V _O = 1.4 V	65	95	V.In.	dB
I _{DD}	Supply current (four amplifiers)	V _O = 2.5 V, No load	V _{IC} = 2.5 V,		2.7	6.4	mA

electrical characteristics, $V_{DD} = 10 \text{ V}$, $T_A = 25^{\circ}\text{C}$ (unless otherwise noted)

	With the top of the to	TEGT COM	DITIONS	T	LC274Y	TXTV	100
	PARAMETER	TEST CON	DITIONS	MIN	TYP	MAX	UNIT
V _{IO}	Input offset voltage	$V_{O} = 1.4 \text{ V},$ $R_{S} = 50 \Omega,$	$V_{IC} = 0$, $R_L = 10 \text{ k}\Omega$	LTW	1.1	10	mV
lιο	Input offset current (see Note 4)	V _O = 5 V,	V _{IC} = 5 V	TIV	0.1	44.	pА
I _{IB}	Input bias current (see Note 4)	V _O = 5 V,	V _{IC} = 5 V	VIII	0.7	1	pA
VICR	Common-mode input voltage range (see Note 5)	TW WW	AM: 100X:C	-0.2 to 9	-0.3 to 9.2	1	V
Vон	High-level output voltage	V _{ID} = 100 mV,	$R_L = 10 \text{ k}\Omega$	8	8.5		V
VOL	Low-level output voltage	$V_{ID} = -100 \text{ mV},$	I _{OL} = 0	COM	0	50	mV
A_{VD}	Large-signal differential voltage amplification	$V_0 = 1 \text{ V to 6 V},$	R _L = 10 kΩ	10	36		V/mV
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min	WW	65	85		dB
ksvr	Supply-voltage rejection ratio (ΔV _{DD} /ΔV _{IO})	$V_{DD} = 5 \text{ V to } 10 \text{ V},$	V _O = 1.4 V	65	95	W	dB
I _{DD}	Supply current (four amplifiers)	V _O = 5 V, No load	V _{IC} = 5 V,	noy.C	3.8	8	mA

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

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operating characteristics, V_{DD} = 5 V, T_A = 25°C

MW	100BABAMETER TV	WW -1100	TEST COMPLETE	NIC .	TLC274	Y	LINIT
WW	PARAMETER	MMM	TEST CONDITIO	NS	MIN TYP	MAX	UNIT
SR	Slow rate at unity gain	$R_L = 10 \text{ k}\Omega$,	C _L = 20 pF,	V _{IPP} = 1 V	3.6	Con.	V/us
SK	Slew rate at unity gain	See Figure 1	TOO . COM	V _{IPP} = 2.5 V	2.9		V/μS
V _n √	Equivalent input noise voltage	f = 1 kHz,	$R_S = 20 \Omega$,	See Figure 2	25		nV/√Hz
ВОМ	Maximum output-swing bandwidth	V _O = V _{OH} , See Figure 1	C _L = 20 _P F,	$R_L = 10 \text{ k}\Omega$,	320		kHz
B ₁	Unity-gain bandwidth	$V_I = 10 \text{ mV},$	C _L = 20 _P F,	See Figure 3	1.7	00 -	MHz
φm	Phase margin	V _I = 10 mV, See Figure 3	f = B ₁ ,	C _L = 20 pF,	46°	100 1.	COM.

operating characteristics, V_{DD} = 10 V, T_A = 25°C

	PARAMETER	TIN	TEST CONDITIO	MC	T	LC274Y	X 10	UNIT
	PARAMETER	W	TEST CONDITIC	N. COB	MIN	TYP	MAX	UNIT
CD	Clay rate at unity rain	$R_L = 10 \text{ k}\Omega$,	C _L = 20 pF,	V _{IPP} = 1 V		5.3	111.	Miss
SR	Slew rate at unity gain	See Figure 1		V _{IPP} = 5.5 V	_ 7	4.6	WW	V/µs
۷ _n	Equivalent input noise voltage	f = 1 kHz,	$R_S = 20 \Omega$,	See Figure 2	1/4	25	- 1	nV/√Hz
Вом	Maximum output-swing bandwidth	V _O = V _{OH} , See Figure 1	C _L = 20 pF,	$R_L = 10 \text{ k}\Omega$,	L.M.	200		kHz
B ₁	Unity-gain bandwidth	$V_I = 10 \text{ mV},$	C _L = 20 _P F,	See Figure 3	JA	2.2	MA.	MHz
m	Phase margin	V _I = 10 mV, See Figure 3	$f = B_1$	C _L = 20 _P F,	LTW	49°		WW.19

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PARAMETER MEASUREMENT INFORMATION

single-supply versus split-supply test circuits

Because the TLC274 and TLC279 are optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The use of either circuit gives the same result.

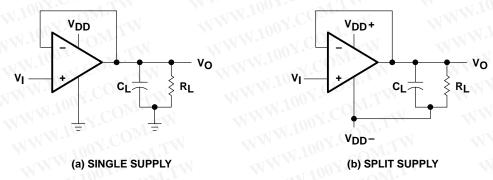


Figure 1. Unity-Gain Amplifier

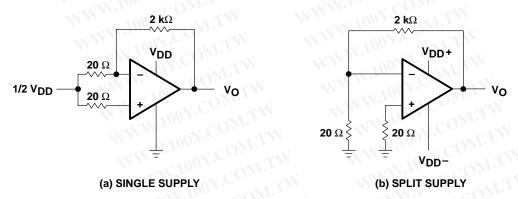


Figure 2. Noise-Test Circuit

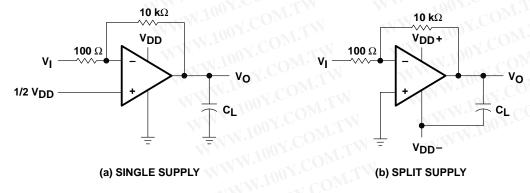


Figure 3. Gain-of-100 Inverting Amplifier

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PARAMETER MEASUREMENT INFORMATION

input bias current

Because of the high input impedance of the TLC274 and TLC279 operational amplifiers, attempts to measure the input bias current can result in erroneous readings. The bias current at normal room ambient temperature is typically less than 1 pA, a value that is easily exceeded by leakages on the test socket. Two suggestions are offered to avoid erroneous measurements:

- 1. Isolate the device from other potential leakage sources. Use a grounded shield around and between the device inputs (see Figure 4). Leakages that would otherwise flow to the inputs are shunted away.
- Compensate for the leakage of the test socket by actually performing an input bias current test (using a picoammeter) with no device in the test socket. The actual input bias current can then be calculated by subtracting the open-socket leakage readings from the readings obtained with a device in the test socket.

One word of caution: many automatic testers as well as some bench-top operational amplifier testers use the servo-loop technique with a resistor in series with the device input to measure the input bias current (the voltage drop across the series resistor is measured and the bias current is calculated). This method requires that a device be inserted into the test socket to obtain a correct reading; therefore, an open-socket reading is not feasible using this method.

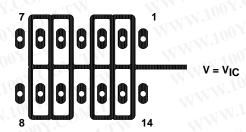


Figure 4. Isolation Metal Around Device Inputs (J and N packages)

low-level output voltage

To obtain low-supply-voltage operation, some compromise was necessary in the input stage. This compromise results in the device low-level output being dependent on both the common-mode input voltage level as well as the differential input voltage level. When attempting to correlate low-level output readings with those quoted in the electrical specifications, these two conditions should be observed. If conditions other than these are to be used, please refer to Figures 14 through 19 in the Typical Characteristics of this data sheet.

input offset voltage temperature coefficient

Erroneous readings often result from attempts to measure temperature coefficient of input offset voltage. This parameter is actually a calculation using input offset voltage measurements obtained at two different temperatures. When one (or both) of the temperatures is below freezing, moisture can collect on both the device and the test socket. This moisture results in leakage and contact resistance, which can cause erroneous input offset voltage readings. The isolation techniques previously mentioned have no effect on the leakage since the moisture also covers the isolation metal itself, thereby rendering it useless. It is suggested that these measurements be performed at temperatures above freezing to minimize error.

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PARAMETER MEASUREMENT INFORMATION

full-power response

Full-power response, the frequency above which the operational amplifier slew rate limits the output voltage swing, is often specified two ways: full-linear response and full-peak response. The full-linear response is generally measured by monitoring the distortion level of the output while increasing the frequency of a sinusoidal input signal until the maximum frequency is found above which the output contains significant distortion. The full-peak response is defined as the maximum output frequency, without regard to distortion, above which full peak-to-peak output swing cannot be maintained.

Because there is no industry-wide accepted value for significant distortion, the full-peak response is specified in this data sheet and is measured using the circuit of Figure 1. The initial setup involves the use of a sinusoidal input to determine the maximum peak-to-peak output of the device (the amplitude of the sinusoidal wave is increased until clipping occurs). The sinusoidal wave is then replaced with a square wave of the same amplitude. The frequency is then increased until the maximum peak-to-peak output can no longer be maintained (Figure 5). A square wave is used to allow a more accurate determination of the point at which the maximum peak-to-peak output is reached.

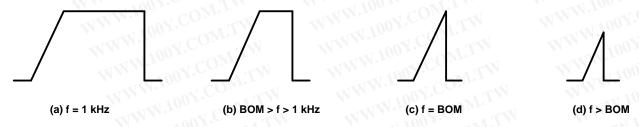


Figure 5. Full-Power-Response Output Signal

test time

Inadequate test time is a frequent problem, especially when testing CMOS devices in a high-volume, short-test-time environment. Internal capacitances are inherently higher in CMOS than in bipolar and BiFET devices and require longer test times than their bipolar and BiFET counterparts. The problem becomes more pronounced with reduced supply levels and lower temperatures.

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TYPICAL CHARACTERISTICS

Table of Graphs

N (COM. CAN MAN.	MAN.	FIGUR
V _{IO}	Input offset voltage	Distribution	6, 7
ανιο	Temperature coefficient of input offset voltage	Distribution	8, 9
Vон	High-level output voltage	vs High-level output current vs Supply voltage vs Free-air temperature	10, 1 ² 12 13
VoL	Low-level output voltage	vs Common-mode input voltage vs Differential input voltage vs Free-air temperature vs Low-level output current	14, 15 16 17 18, 19
AVD	Large-signal differential voltage amplification	vs Supply voltage vs Free-air temperature vs Frequency	20 21 32, 33
I _{IB}	Input bias current	vs Free-air temperature	22
lio	Input offset current	vs Free-air temperature	22
V _{IC}	Common-mode input voltage	vs Supply voltage	23
I _{DD}	Supply current	vs Supply voltage vs Free-air temperature	24 25
SR	Slew rate	vs Supply voltage vs Free-air temperature	26 27
	Normalized slew rate	vs Free-air temperature	28
V _{O(PP)}	Maximum peak-to-peak output voltage	vs Frequency	29
B ₁	Unity-gain bandwidth	vs Free-air temperature vs Supply voltage	30 31
φm	Phase margin	vs Supply voltage vs Free-air temperature vs Load capacitance	34 35 36
Vn	Equivalent input noise voltage	vs Frequency	37
	Phase shift	vs Frequency	32, 33

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TYPICAL CHARACTERISTICS

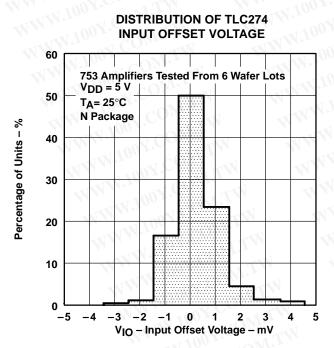


Figure 6

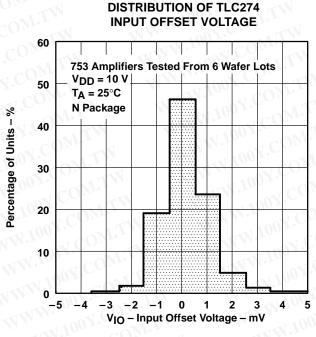


Figure 7

DISTRIBUTION OF TLC274 AND TLC279 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT

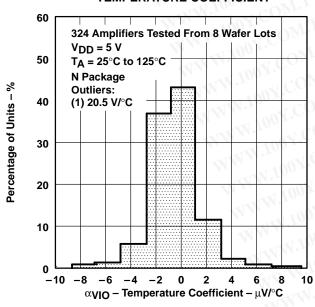


Figure 8

DISTRIBUTION OF TLC274 AND TLC279 INPUT OFFSET VOLTAGE

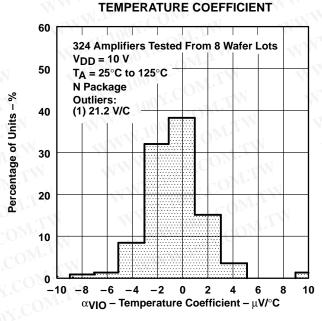


Figure 9

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TYPICAL CHARACTERISTICS[†]

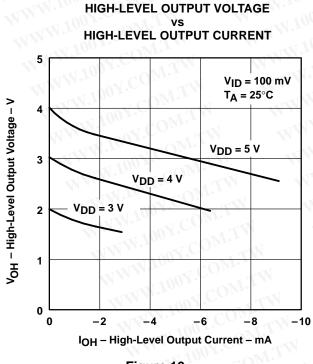
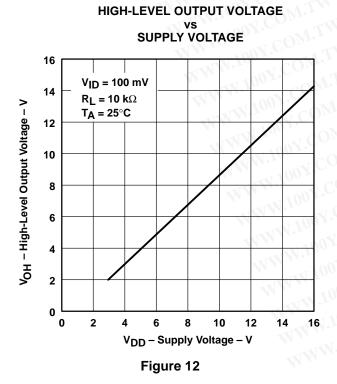


Figure 10



HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

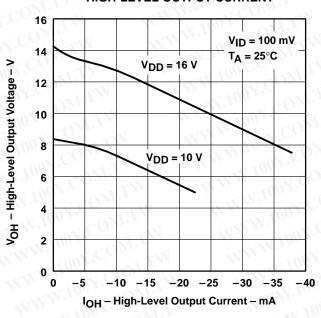


Figure 11

HIGH-LEVEL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

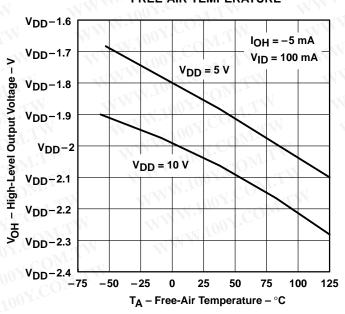


Figure 13

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.



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TYPICAL CHARACTERISTICS[†]

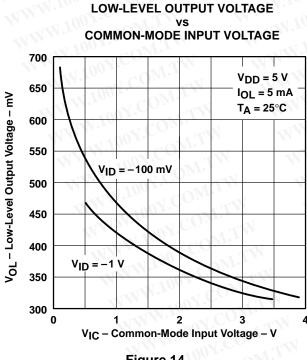


Figure 14

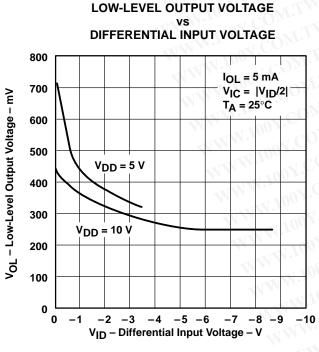


Figure 16

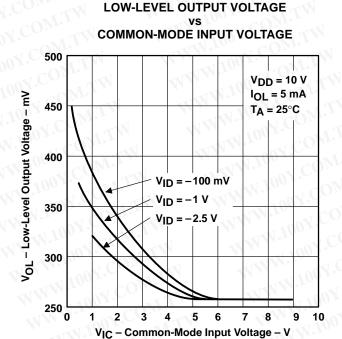


Figure 15



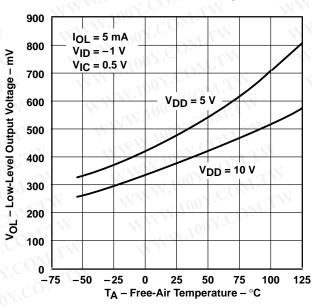


Figure 17

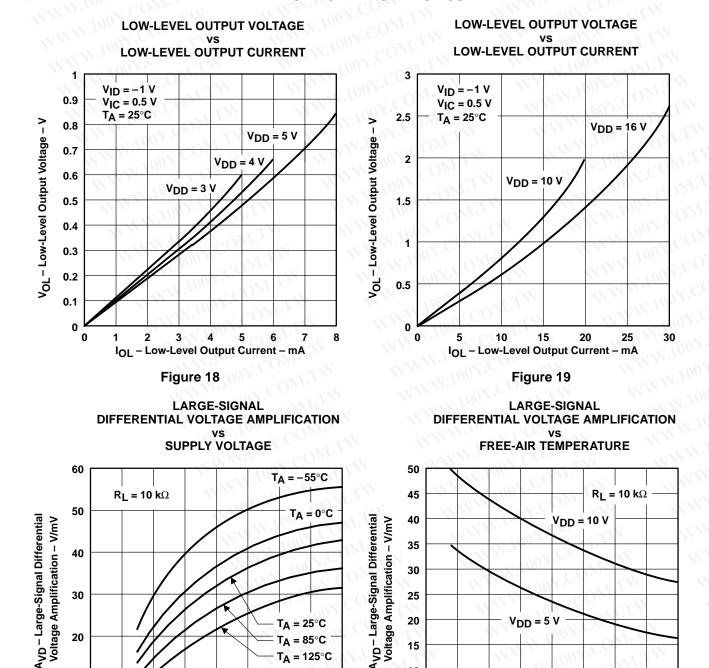
† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.



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TYPICAL CHARACTERISTICS[†]



† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.



10

5

-75

-50

-25

25

Figure 21

T_A – Free-Air Temperature – °C

50

75

100

125

10

0

0

2

8

V_{DD} – Supply Voltage – V

Figure 20

10

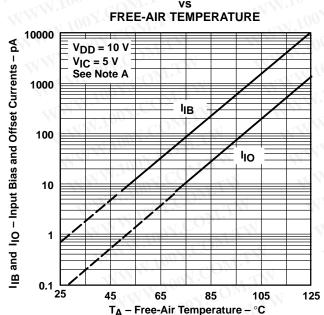
12

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COMMON-MODE

TYPICAL CHARACTERISTICS[†]

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT



NOTE A: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

INPUT VOLTAGE POSITIVE LIMIT SUPPLY VOLTAGE 16 T_A = 25°C 14 - Common-Mode Input Voltage 12 10 8 6 <u>د</u> 2 10 12 0 14

Figure 22

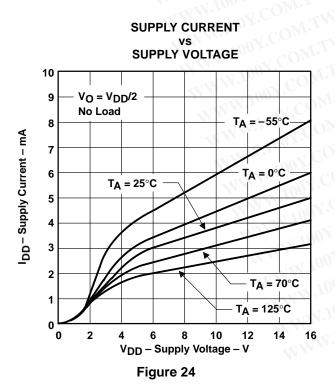
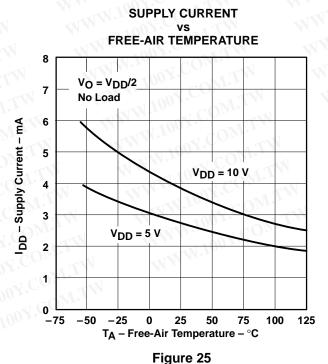


Figure 23

V_{DD} - Supply Voltage - V

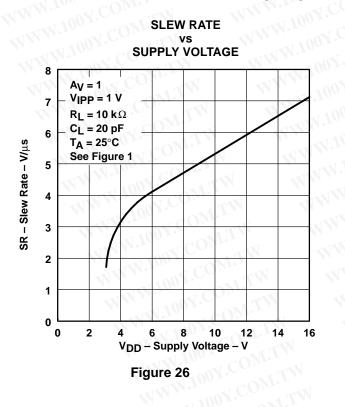


† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

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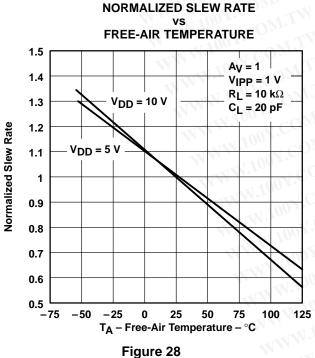
TYPICAL CHARACTERISTICS[†]



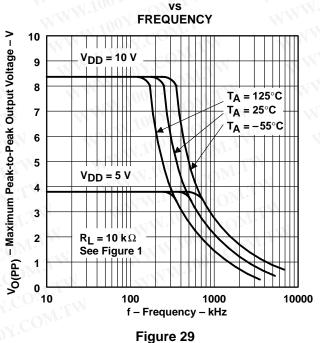
VS FREE-AIR TEMPERATURE $A_V = 1$ $R_L = 10 k\Omega$ $V_{DD} = 10 V$ $C_L = 20 pF$ $V_{IPP} = 5.5 V$ See Figure 1 Slew Rate - V/us $V_{DD} = 10 V$ 5 $V_{IPP} = 1 V$ 4 3 $V_{DD} = 5 V$ 2 V_{IPP} = 1 V $V_{DD} = 5 V$ $V_{IPP} = 2.5 V$ -50 -25 0 25 50 75 100 125 T_A - Free-Air Temperature - °C

SLEW RATE

Figure 27



MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE

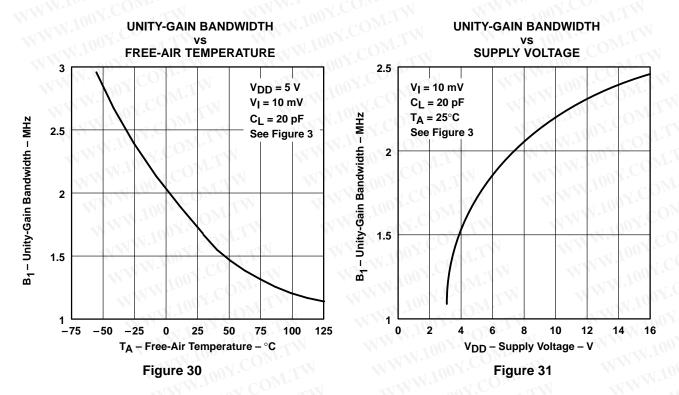


† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

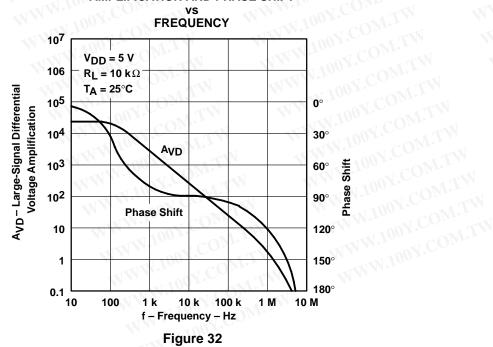


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TYPICAL CHARACTERISTICS[†]



LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT



[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.



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TYPICAL CHARACTERISTICS[†]

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT

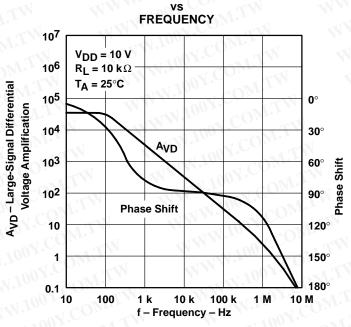
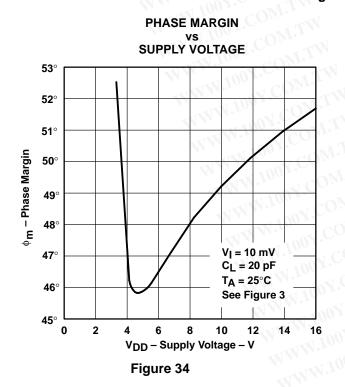
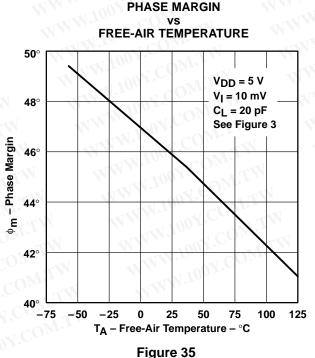


Figure 33





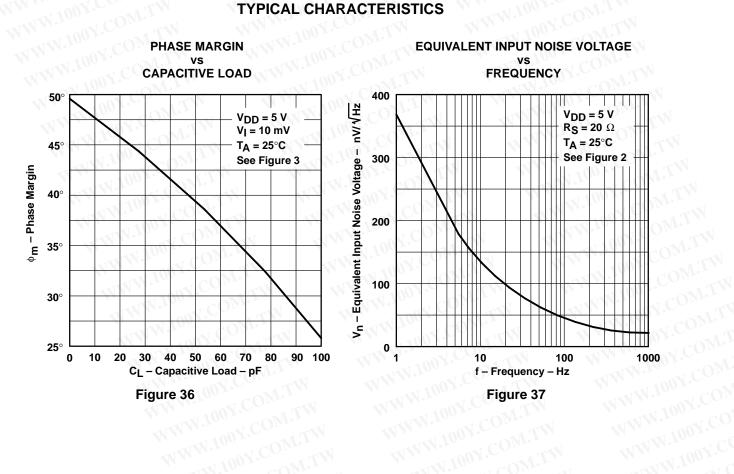
† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.



TLC274, TLC274A, TLC274B, TLC274Y, TLC279 Lincmos™ Precision quad operational amplifiers

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TYPICAL CHARACTERISTICS



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APPLICATION INFORMATION

single-supply operation

While the TLC274 and TLC279 perform well using dual power supplies (also called balanced or split supplies), the design is optimized for single-supply operation. This design includes an input common-mode voltage range that encompasses ground as well as an output voltage range that pulls down to ground. The supply voltage range extends down to 3 V (C-suffix types), thus allowing operation with supply levels commonly available for TTL and HCMOS; however, for maximum dynamic range, 16-V single-supply operation is recommended.

Many single-supply applications require that a voltage be applied to one input to establish a reference level that is above ground. A resistive voltage divider is usually sufficient to establish this reference level (see Figure 38). The low input bias current of the TLC274 and TLC279 permits the use of very large resistive values to implement the voltage divider, thus minimizing power consumption.

The TLC274 and TLC279 work well in conjunction with digital logic; however, when powering both linear devices and digital logic from the same power supply, the following precautions are recommended:

- Power the linear devices from separate bypassed supply lines (see Figure 39); otherwise the linear device supply rails can fluctuate due to voltage drops caused by high switching currents in the digital logic.
- 2. Use proper bypass techniques to reduce the probability of noise-induced errors. Single capacitive decoupling is often adequate; however, high-frequency applications may require R_C decoupling.

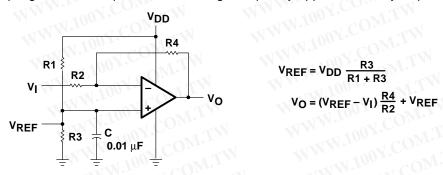


Figure 38. Inverting Amplifier With Voltage Reference

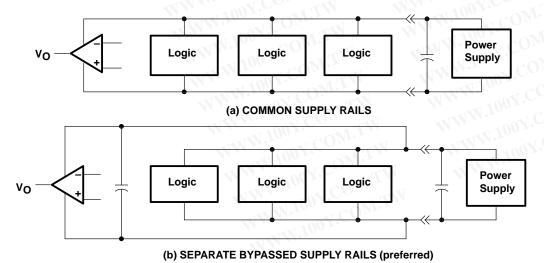


Figure 39. Common Versus Separate Supply Rails

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APPLICATION INFORMATION

input characteristics

The TLC274 and TLC279 are specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction. Exceeding this specified range is a common problem, especially in single-supply operation. Note that the lower range limit includes the negative rail, while the upper range limit is specified at $V_{DD} - 1$ V at $T_A = 25^{\circ}$ C and at $V_{DD} - 1.5$ V at all other temperatures.

The use of the polysilicon-gate process and the careful input circuit design gives the TLC274 and TLC279 very good input offset voltage drift characteristics relative to conventional metal-gate processes. Offset voltage drift in CMOS devices is highly influenced by threshold voltage shifts caused by polarization of the phosphorus dopant implanted in the oxide. Placing the phosphorus dopant in a conductor (such as a polysilicon gate) alleviates the polarization problem, thus reducing threshold voltage shifts by more than an order of magnitude. The offset voltage drift with time has been calculated to be typically 0.1 μ V/month, including the first month of operation.

Because of the extremely high input impedance and resulting low bias current requirements, the TLC274 and TLC279 are well suited for low-level signal processing; however, leakage currents on printed-circuit boards and sockets can easily exceed bias current requirements and cause a degradation in device performance. It is good practice to include guard rings around inputs (similar to those of Figure 4 in the Parameter Measurement Information section). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input (see Figure 40).

Unused amplifiers should be connected as grounded unity-gain followers to avoid possible oscillation.

noise performance

The noise specifications in operational amplifier circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias current requirements of the TLC274 and TLC279 result in a very low noise current, which is insignificant in most applications. This feature makes the devices especially favorable over bipolar devices when using values of circuit impedance greater than 50 k Ω , since bipolar devices exhibit greater noise currents.

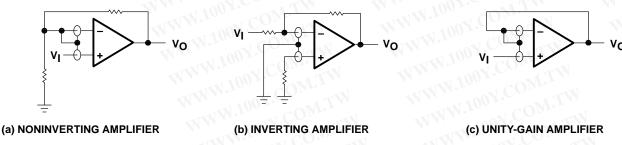


Figure 40. Guard-Ring Schemes

output characteristics

The output stage of the TLC274 and TLC279 is designed to sink and source relatively high amounts of current (see typical characteristics). If the output is subjected to a short-circuit condition, this high current capability can cause device damage under certain conditions. Output current capability increases with supply voltage.

All operating characteristics of the TLC274 and TLC279 were measured using a 20-pF load. The devices drive higher capacitive loads; however, as output load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation (see Figure 41). In many cases, adding a small amount of resistance in series with the load capacitance alleviates the problem.



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(d) TEST CIRCUIT

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output characteristics (continued)

(c) $C_L = 150 pF$, $R_L = NO LOAD$

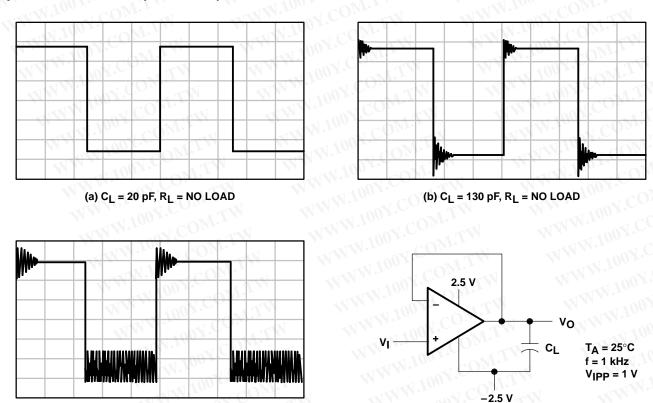


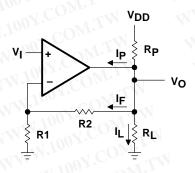
Figure 41. Effect of Capacitive Loads and Test Circuit

Although the TLC274 and TLC279 possess excellent high-level output voltage and current capability, methods for boosting this capability are available, if needed. The simplest method involves the use of a pullup resistor (R_P) connected from the output to the positive supply rail (see Figure 42). There are two disadvantages to the use of this circuit. First, the NMOS pulldown transistor N4 (see equivalent schematic) must sink a comparatively large amount of current. In this circuit, N4 behaves like a linear resistor with an on-resistance between approximately $60~\Omega$ and $180~\Omega$, depending on how hard the op amp input is driven. With very low values of R_P, a voltage offset from 0~V at the output occurs. Second, pullup resistor R_P acts as a drain load to N4 and the gain of the operational amplifier is reduced at output voltage levels where N5 is not supplying the output current.

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output characteristics (continued)



$$Rp = \frac{V_{DD} - V_{O}}{I_F + I_1 + I_F}$$

Ip = Pullup current required by the operational amplifier (typically 500 μA)

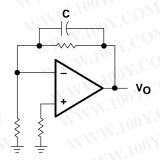


Figure 43. Compensation for Input Capacitance

Figure 42. Resistive Pullup to Increase VOH

feedback

Operational amplifier circuits nearly always employ feedback, and since feedback is the first prerequisite for oscillation, some caution is appropriate. Most oscillation problems result from driving capacitive loads (discussed previously) and ignoring stray input capacitance. A small-value capacitor connected in parallel with the feedback resistor is an effective remedy (see Figure 43). The value of this capacitor is optimized empirically.

electrostatic discharge protection

The TLC274 and TLC279 incorporate an internal electrostatic discharge (ESD) protection circuit that prevents functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2. Care should be exercised, however, when handling these devices as exposure to ESD may result in the degradation of the device parametric performance. The protection circuit also causes the input bias currents to be temperature-dependent and have the characteristics of a reverse-biased diode.

latch-up

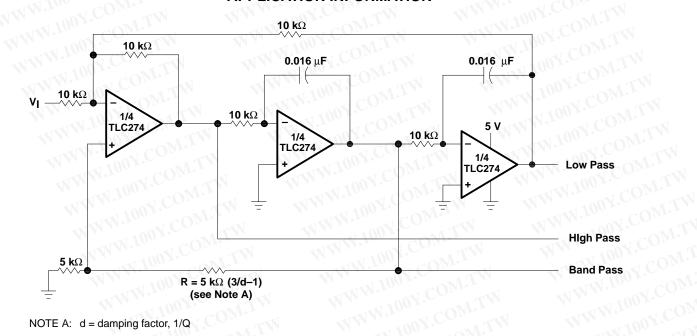
Because CMOS devices are susceptible to latch-up due to their inherent parasitic thyristors, the TLC274 and TLC279 inputs and outputs were designed to withstand -100-mA surge currents without sustaining latch-up; however, techniques should be used to reduce the chance of latch-up whenever possible. Internal protection diodes should not, by design, be forward biased. Applied input and output voltage should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 μ F typical) located across the supply rails as close to the device as possible.

The current path established if latch-up occurs is usually between the positive supply rail and ground and can be triggered by surges on the supply lines and/or voltages on either the output or inputs that exceed the supply voltage. Once latch-up occurs, the current flow is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor and usually results in the destruction of the device. The chance of latch-up occurring increases with increasing temperature and supply voltages.

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NOTE A: d = damping factor, 1/Q

Figure 44. State-Variable Filter

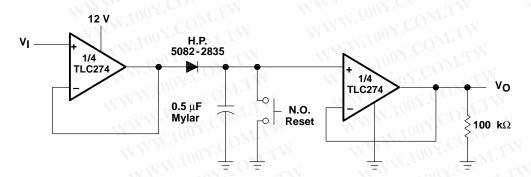
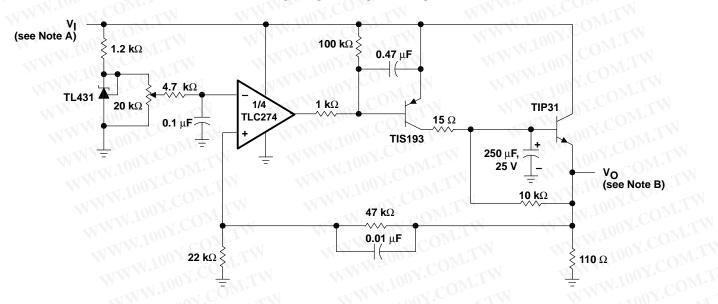


Figure 45. Positive-Peak Detector

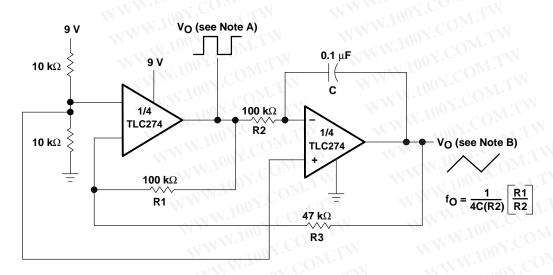
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NOTES: A. $V_I = 3.5 \text{ V to } 15 \text{ V}$ B. $V_O = 2 \text{ V}, 0 \text{ to } 1 \text{ A}$

Figure 46. Logic-Array Power Supply



NOTES: A. $V_{O(PP)} = 8 \text{ V}$ B. $V_{O(PP)} = 4 \text{ V}$

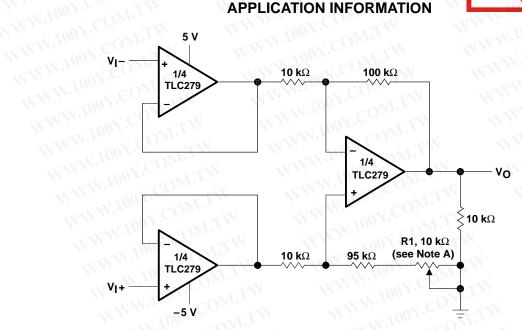
Figure 47. Single-Supply Function Generator

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NOTE A: CMRR adjustment must be noninductive.

Figure 48. Low-Power Instrumentation Amplifier

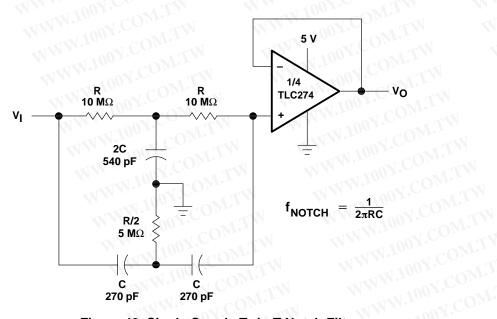


Figure 49. Single-Supply Twin-T Notch Filter

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