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- Trimmed Offset Voltage: TLC27L7 . . . 500 μV Max at 25°C, V_{DD} = 5 V
- Input Offset Voltage Drift . . . Typically
 0.1 μV/Month, Including the First 30 Days
- Wide Range of Supply Voltages Over Specified Temperature Range:

0°C to 70°C . . . 3 V to 16 V -40°C to 85°C . . . 4 V to 16 V -55°C to 125°C . . . 4 V to 16 V

- Single-Supply Operation
- Common-Mode Input Voltage Range Extends Below the Negative Rail (C-Suffix, I-Suffix Types)
- Ultra-Low Power . . . Typically 95 μW at 25°C, V_{DD} = 5 V
- Output Voltage Range Includes Negative Rail
- High Input Impedance . . . 10¹² Ω Typ
- ESD-Protection Circuitry
- Small-Outline Package Option Also Available in Tape and Reel
- Designed-In Latch-Up immunity

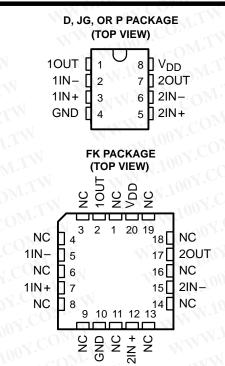
description

The TLC27L2 and TLC27L7 dual operational amplifiers combine a wide range of input offset voltage grades with low offset voltage drift, high input impedance, extremely low power, and high gain.

AVAILABLE OPTIONS

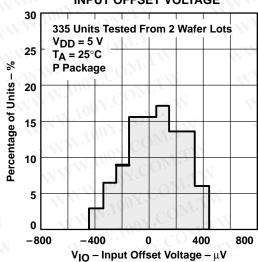
			PACK	AGE	COM
TA	V _{IO} max AT 25°C	SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)
0°C to 70°C	500 μV 2 mV 5 mV 10 mV	TLC27L7CD TLC27L2BCD TLC27L2ACD TLC27L2CD	-	MMM.100	TLC27L7CP TLC27L2BCP TLC27L2ACP TLC27L2CP
-40°C to 85°C	500 μV 2 mV 5 mV 10 mV	TLC27L7ID TLC27L2BID TLC27L2AID TLC27L2ID	ı	WWW.	TLC27L7IP TLC27L2BIP TLC27L2AIP TLC27L2IP
−55°C to 125°C	500 μV 10 mV	TLC27L7MD TLC27L2MD	TLC27L7MFK TLC27L2MFK	TLC27L7MJG TLC27L2MJG	TLC27L7MP TLC27L2MP

The D package is available taped and reeled. Add R suffix to the device type (e.g., TLC27L7CDR).



NC - No internal connection

DISTRIBUTION OF TLC27L7 INPUT OFFSET VOLTAGE



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TEXAS INSTRUMENTS

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description (continued)

These devices use Texas Instruments silicon-gate LinCMOS™ technology, which provides offset voltage stability far exceeding the stability available with conventional metal-gate processes.

The extremely high input impedance, low bias currents, and low power consumption make these cost-effective devices ideal for high gain, low frequency, low power applications. Four offset voltage grades are available (C-suffix and I-suffix types), ranging from the low-cost TLC27L2 (10 mV) to the high-precision TLC27L7 (500 μ V). These advantages, in combination with good common-mode rejection and supply voltage rejection, make these devices a good choice for new state-of-the-art designs as well as for upgrading existing designs.

In general, many features associated with bipolar technology are available in LinCMOS™ operational amplifiers, without the power penalties of bipolar technology. General applications such as transducer interfacing, analog calculations, amplifier blocks, active filters, and signal buffering are easily designed with the TLC27L2 and TLC27L7. The devices also exhibit low voltage single-supply operation and ultra-low power consumption, making them ideally suited for remote and inaccessible battery-powered applications. The common-mode input voltage range includes the negative rail.

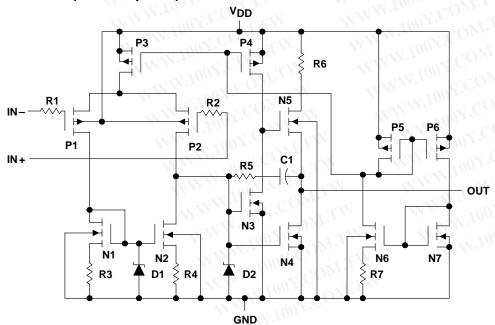
A wide range of packaging options is available, including small-outline and chip-carrier versions for high-density system applications.

The device inputs and outputs are designed to withstand –100-mA surge currents without sustaining latch-up.

The TLC27L2 and TLC27L7 incorporate internal ESD-protection circuits that prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parametric performance.

The C-Suffix devices are characterized for operation from 0° C to 70° C. The I-suffix devices are characterized for operation from -40° C to 85° C. The M-suffix devices are characterized for operation over the full military temperature range of -55° C to 125° C.

equivalent schematic (each amplifier)





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TLC27L2, TLC27L2A, TLC27L2B, TLC27L7 LinCMOS™ PRECISION DUAL OPERATIONAL AMPLIFIERS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

W. T. COM.	TONN OF TOUR TON	W. CO.
Supply voltage, V _{DD} (see Note 1)	N	18 V
	e 2)	
Input voltage range, V _I (any input)		0.3 V to V _{DD}
Input current, I ₁		±5 mA
Output current, IO (each output)		±30 mA
Total current out of GND		45 mA
Duration of short-circuit current at	(or below) 25°C (see Note 3)	Unlimited
Continuous total dissipation		See Dissipation Rating Table
Operating free-air temperature, TA	: C suffix	0°C to 70°C
	I suffix	
	M suffix	–55°C to 125°C
Storage temperature range		65°C to 150°C
Case temperature for 60 seconds:	FK package	260°C
	ch) from case for 10 seconds: D or P packa	
Lead temperature 1,6 mm (1/16 in	ch) from case for 60 seconds: JG package	300°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
 - 2. Differential voltages are at IN+ with respect to IN-.
 - 3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded (see application section).

DISSIPATION RATING TABLE

PACKAGE	T _A ≤ 25°C POWER RATING	DERATING FACTOR ABOVE T _A = 25°C	T _A = 70°C POWER RATING	T _A = 85°C POWER RATING	T _A = 125°C POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	In -
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
Р	1000 mW	8.0 mW/°C	640 mW	520 mW	W. I.

recommended operating conditions

	WWW. OOX.CO. TW	C SU	FFIX	I SUI	FFIX	M SU	FFIX	LINUT
		MIN	MAX	MIN	MAX	MIN	MAX	UNIT
Supply voltage, V _{DD}	M. Too r. COW. I.	3	16	4	16	4	16	V
Common mode input voltage V	V _{DD} = 5 V	-0.2	3.5	-0.2	3.5	0	3.5	ı V
Common-mode input voltage, V _{IC}	V _{DD} = 10 V	-0.2	8.5	-0.2	8.5	0	8.5	V
Operating free-air temperature, $T_{\mbox{\scriptsize A}}$	M.In. COM.	0	70	-40	85	-55	125	√ °C



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electrical characteristics at specified free-air temperature, $V_{DD} = 5 \text{ V}$ (unless otherwise noted)

N	PARAMETER	M.TW M.TW	TEST CONI	DITIONS	T _A †	TL TL	C27L2C C27L2A C27L2B C27L7C	C	UNIT
	M.100	OM:	WW.100	COM		MIN	TYP	MAX	O_{Mr}
	WW. 1001.	TLC27L2C	V _O = 1.4 V,	$V_{IC} = 0$,	25°C	1	1.1	10	OM.
		TEGZTEZC	$R_S = 50 \Omega$,	$R_L = 1 M\Omega$	Full range	W.	- 41	12	mV
		TLC27L2AC	V _O = 1.4 V,	$V_{IC} = 0$,	25°C	V	0.9	5	Tilly
11/10	Input offset voltage	TEOZTEZAC	$R_S = 50 \Omega$,	$R_L = 1 M\Omega$	Full range	<	MW	6.5	4 . 6 CO 1
VIO	input onset voltage	TLC27L2BC	V _O = 1.4 V,	V _{IC} = 0,	25°C		204	2000	-1 CC
Ī		TLC27L2BC	$R_S = 50 \Omega$,	$R_L = 1 M\Omega$	Full range		M	3000	
		TI C071 7C	V _O = 1.4 V,	V _{IC} = 0,	25°C		170	500	μV
		TLC27L7C	$R_S = 50 \Omega$,	$R_L = 1 M\Omega$	Full range	1	4 N	1500	
ανιο	Average temperature co	pefficient of input	TW	M. 100	25°C to 70°C	W	1.1	WW	μV/°C
	WALLS IN	V. Jun Z. COL		XXVVI.	25°C		0.1	60	4
ΙO	Input offset current (see	Note 4)	$V_0 = 2.5 V$,	$V_{IC} = 2.5 V$	70°C	- 1	7	300	pΑ
	MA	100 Y. C.	30.77	W ** 10	25°C	TV	0.6	60	T.W.10
IB	Input bias current (see I	Note 4)	$V_0 = 2.5 V$,	$V_{IC} = 2.5 V$	70°C	WILL	50	600	pΑ
.,	Common-mode input vo	oltage range	COWLIN	MMM.	25°C	-0.2 to 4	-0.3 to 4.2	V	V
VICR	(see Note 5)	MMM.100	COM.TW		Full range	-0.2 to 3.5	TW		V
		TWW.Io	COM	-31	25°C	3.2	4.1		W
Vон	High-level output voltag	e 1	$V_{ID} = 100 \text{ mV},$	$R_L = 1 M\Omega$	0°C	3	4.1	- T	٧
			100Y.COMITY		70°C	3	4.2	1	1
		MAN	COM.	W	25°C	U.Y.C.	0	50	4
VOL	Low-level output voltage	e VVV	$V_{ID} = -100 \text{ mV},$	I _{OL} = 0	0°C	. N.C	0	50	mV
			N.100 Y.	1.41	70°C	UU .	0	50	
		MA	1007.0	TW	25°C	50	700	V.I.A.	
AVD	Large-signal differential	voltage	$V_0 = 0.25 \text{ V to 2 V},$	$R_L = 1 M\Omega$	0°C	50	700	TI	V/mV
- 	amplification		NW.100 TO	M-2	70°C	50	380	M	W.
			100	Mil	25°C	65	94	$O_{M_{1}}$	-41
CMRR	Common-mode rejectio	n ratio	V _{IC} = V _{ICR} min		0°C	60	95	Mo	dB
	•		NWW.		70°C	60	95		WI
			TWW.10	COMP	25°C	70	97	COD	TIN
ksvr	Supply-voltage rejection	n ratio	$V_{DD} = 5 \text{ V to } 10 \text{ V},$	V _O = 1.4 V	0°C	60	97	1 CO	dB
	$(\Delta V_{DD}/\Delta V_{IO})$		WW 100	Y.V.	70°C	60	98	7.	
			MMA	V.CO.	25°C	MW.	20	34	
I_{DD}	Supply current (two am	olifiers)	$V_0 = 2.5 \text{ V},$	$V_{IC} = 2.5 V,$	0°C		24	42	μΑ
 		•	No load		70°C		16	28	

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

5. This range also applies to each input individually.



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TLC27L2, TLC27L2A, TLC27L2B, TLC27L7 LinCMOS™ PRECISION DUAL OPERATIONAL AMPLIFIERS

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electrical characteristics at specified free-air temperature, $V_{\mbox{\scriptsize DD}}$ = 10 V (unless otherwise noted)

MM	PARAMETER	LM A	TEST CON	DITIONS	T _A †	TL TL	C27L2C C27L2A C27L2B C27L7C	C C	UNIT
	NW.1001. COM		WWW.100	COM	***	MIN	TYP	MAX	W
1//	1001.	TLC27L2C	V _O = 1.4 V,	$V_{IC} = 0$,	25°C	NIX.	1.1	10	7.1
		TLOZILZO	$R_S = 50 \Omega$,	$R_L = 1 M\Omega$	Full range		₁ 1007	12	mV
		TLC27L2AC	$V_0 = 1.4 \text{ V},$	$V_{IC} = 0$,	25°C		0.9	5	1110
V:0	Input offset voltage	TLCZTLZAC	$R_S = 50 \Omega$,	$R_L = 1 M\Omega$	Full range	WIN	W.r.	6.5	Diar.
VIO	input onset voltage	TLC27L2BC	V _O = 1.4 V,	$V_{IC} = 0$,	25°C	-75	235	2000	OM
		TEGZTEZBC	$R_S = 50 \Omega$,	$R_L = 1 M\Omega$	Full range		- xx 1	3000	μV
		TLC27L7C	$V_0 = 1.4 V$,	$V_{IC} = 0$,	25°C	V	190	800	
	W.100	TEGZTETO	$R_S = 50 \Omega$,	$R_L = 1 M\Omega$	Full range	V	WWW	1900	1 CO 1
ανιο	Average temperature conffset voltage	oefficient of input	N WW	N.100 Y.C.C	25°C to 70°C		1	N.100	μV/°C
		" COMP.	30 - v 30V	W. Para C	25°C		0.1	60	N.C
ΙΟ	Input offset current (see	e Note 4)	$V_0 = 5 V$,	$V_{IC} = 5 V$	70°C	1	8	300	pΑ
	- III WW.	1007.	In M	1007	25°C		0.7	60	100 -
lΒ	Input bias current (see	Note 4)	$V_0 = 5 V$,	$V_{IC} = 5 V$	70°C	N	50	600	pΑ
	Common-mode input v	oltage range	MTW	MMM.100	25°C	-0.2 to 9	-0.3 to 9.2	MM	V.V
VICR	(see Note 5)	WW.100Y.C	OM.TW		Full range	-0.2 to 8.5	V	N	V .1
		TANN Too	COMP	WW	25°C	8	8.9	4	JAMAN
Vон	High-level output voltage	ge	$V_{ID} = 100 \text{ mV},$	$R_L = 1 M\Omega$	0°C	7.8	8.9		V
			I.CO. TW		70°C	7.8	8.9		W.
		MAN	V.Com	WW	25°C		0	50	MA
VOL	Low-level output voltag	e	$V_{ID} = -100 \text{ mV},$	$I_{OL} = 0$	0°C	$C_{O_{D_0}}$	0	50	mV
			0.01. $COW.I.A.$		70°C	-1 CO	0	50	- 1
		MM.	100 Y. OM.T		25°C	50	860		111
A_{VD}	Large-signal differentia amplification	l voltage	$V_0 = 1 \text{ V to 6 V},$	$R_L = 1 M\Omega$	0°C	50	1025		V/mV
	ampimodion	TAN V	The COM.		70°C	50	660	TIN	
		_<1	N.100 P. COM	. 1	25°C	65	97	. 1	
CMRR	Common-mode rejection	on ratio	V _{IC} = V _{ICR} min		0°C	60	97	1.1	dB
		W	LAL. OUN COL	WT	70°C	60	97	TI	
	O	-1	WW. PO CO	NI.	25°C	70	97	TAS.	N
ksvr	Supply-voltage rejectio (ΔV _{DD} /ΔV _{IO})	n ratio	$V_{DD} = 5 \text{ V to } 10 \text{ V},$	$V_0 = 1.4 \text{ V}$	0°C	60	97	0_{Mr}	dB
	(A V DD / A V IO/		MAL 1007.	WIL	70°C	60	98		
			V- EV 400Y.	V- 1 50.	25°C		29	46	
I_{DD}	Supply current (two am	plifiers)	V _O = 5 V, No load	$V_{IC} = 5 V$	0°C		36	66	μΑ
			4/22/1007		70°C		22	40	

[†]Full range is 0°C to 70°C.

NOTES: 4 The typical values of input bias current and input offset current below 5 pA were determined mathematically.

5 This range also applies to each input individually.



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electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

N	PARAMETER	M.TW	TEST CON	DITIONS	τ _A †	TL TL	C27L2I C27L2A C27L2B C27L7I		UNIT
	W.100	OMI	1. W.10	COM.		MIN	TYP	MAX	O_{Mr} .
		TLC27L2I	V _O = 1.4 V,	$V_{IC} = 0$,	25°C	111	1.1	10	OM
		TEOZTEZI	$R_S = 50 \Omega$,	$R_L = 1 M\Omega$	Full range		-41	13	mV
		TLC27L2AI	$V_0 = 1.4 V$,	$V_{IC} = 0$,	25°C	V	0.9	5	UIIV
VIO	Input offset voltage	1202/22/11	$R_S = 50 \Omega$,	$R_L = 1 M\Omega$	Full range		WW	7	V.CO
VIO	input onset voltage	TLC27L2BI	V _O = 1.4 V,	$V_{IC} = 0$,	25°C		240	2000	<1 C
		0 1.60212281	$R_S = 50 \Omega$,	$R_L = 1 M\Omega$	Full range		M	3500	μV
		TLC27L7I	V _O = 1.4 V,	$V_{IC} = 0$,	25°C		170	500	002.7
	WW.	J.CO	$R_S = 50 \Omega$,	$R_L = 1 M\Omega$	Full range		N.	2000	Voc
αΛΙΟ	Average temperature of input offset voltage	coefficient of	TW T	NAM. 100	25°C to 85°C	N	1.1	WW	μV/°C
l. a	Innut offeet ourment (co	o Note 4) V.CC	V- 25V	V.5 2.5.V	25°C	TW	0.1	60	- m/A
liO	Input offset current (se	e Note 4)	$V_0 = 2.5 V$,	$V_{IC} = 2.5 V$	85°C	-XXI	24	1000	pΑ
1	Innut high ourrent (occ	Note 100 Y.	Vo 25V	V:- 25V	25°C		0.6	60	
İΙΒ	Input bias current (see	Note 4)	$V_0 = 2.5 V$,	$V_{IC} = 2.5 V$	85°C	TW	200	2000	pΑ
.,	Common-mode input v	roltage range	COM.TW	MMM	25°C	-0.2 to 4	-0.3 to 4.2	V	V
VICR	(see Note 5)	MAMA-10	OY.COM.TW		Full range	-0.2 to 3.5	TW		٧
		WW.	COM	i ai	25°C	3.2	4.1		N.
Vон	High-level output volta	ge	$V_{ID} = 100 \text{ mV},$	$R_L = 1 M\Omega$	-40°C	3	4.1	T	V
			100Y.Co. T. T.		85°C	3	4.2	W	
		WW	A. CO.	TW.	25°C	U.Y.C.	0	50	
V_{OL}	Low-level output voltage	je	$V_{ID} = -100 \text{ mV},$	$I_{OL} = 0$	-40°C	. V.C	0	50	mV
			W.1001. COM		85°C	00	00	50	
		1/1	1007.	V.T.M	25°C	50	480	1.11	
AVD	Large-signal differentia voltage amplification	ıl	$V_0 = 0.25 \text{ V to 2 V},$	$R_L = 1 M\Omega$	-40°C	50	900	TI	V/mV
	voltage amplification		MM. Inc. CO)NI.	85°C	50	330	- 11	N
			M.100	OM.	25°C	65	94	0_{Mr} ,	-XXI
CMRR	Common-mode rejection	on ratio	$V_{IC} = V_{ICR}min$		-40°C	60	95	Mor	dB
			MAN TOUX	CU	85°C	60	95		TW
			WWW.IO	COM	25°C	70	97	COR	TV
ksvr	Supply-voltage rejection (ΔV _{DD} /ΔV _{IO})	n ratio	$V_{DD} = 5 \text{ V to } 10 \text{ V},$	V _O = 1.4 V	-40°C	60	97	CO	dB
	\\UD'_\\		WW 100	Y. OM.T	85°C	60	98	7.	
			V 05.V	01/ 251/	25°C	MAA	20	34	
I_{DD}	Supply current (two an	nplifiers)	$V_O = 2.5 \text{ V},$ No load	$V_{IC} = 2.5 V,$	-40°C		31	54	μΑ
			TAN A		85°C		15	26	

[†] Full range is -40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.



^{5.} This range also applies to each input individually.

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electrical characteristics at specified free-air temperature, $V_{\mbox{\scriptsize DD}}$ = 10 V (unless otherwise noted)

WW	PARAMETER		TEST CON	DITIONS	T _A †	TL TL	C27L2I C27L2A C27L2B C27L7I		UNIT
	M.1001. COM.	11	TWW.100	OM	· .	MIN	TYP	MAX	W
111	100 Y. CON	TLC27L2I	V _O = 1.4 V,	$V_{IC} = 0$,	25°C	Wix	1.1	10	7.1
		TLOZ/LZI	$R_S = 50 \Omega$,	$R_L = 1 M\Omega$	Full range		₁ 100?	13	mV
		TLC27L2AI	$V_0 = 1.4 V,$	$V_{IC} = 0$,	√ 25°C		0.9	5	
۷ıO	Input offset voltage	TEGZTEZAI	$R_S = 50 \Omega$,	$R_L = 1 M\Omega$	Full range	WIN	W.r.	7.7	Div.
٧IO	input onset voltage	TLC27L2BI	V _O = 1.4 V,	V _{IC} = 0,	25°C		235	2000	O_{M^*}
		TEOZITEZBI	$R_S = 50 \Omega$,	$R_L = 1 M\Omega$	Full range	7/1 1	`	3500	μV
		TLC27L7I	$V_0 = 1.4 V$,	$V_{IC} = 0$,	25°C	W	190	800	μν
	WW.Ino	TEGZIEN	$R_S = 50 \Omega$,	$R_L = 1 M\Omega$	Full range		VWW	2900	1 CO 5
αVIO	Average temperature co offset voltage	efficient of input	MMA		25°C to 85°C		1	1 10 N . Too	μV/°C
		" COMP.	W J. W	W. Sant C	25°C		0.1	60	ny.C
ΙO	Input offset current (see	Note 4)	$V_0 = 5 V$,	$V_{IC} = 5 V$	85°C	ſ	26	1000	pΑ
		1007	144	WX 100 1.	25°C		0.7	60	100
IВ	Input bias current (see N	Note 4)	$V_0 = 5 V$,	$V_{IC} = 5 V$	85°C	7	220	2000	pA
	Common-mode input vo	ltage range	T.TW	NAM.100	25°C	-0.2 to 9	-0.3 to 9.2	MM	V-V
VICR	(see Note 5)	MW-100Y.C	OW.TW		Full range	-0.2 to 8.5		N	V
	**	M. Ing	COMP	WWW	25°C	8	8.9	*	MW.
VOH	High-level output voltage	6 . 100x	$V_{ID} = 100 \text{ mV},$	$R_L = 1 M\Omega$	−40°C	7.8	8.9		V
			I.V. TW		85°C	7.8	8.9		W.
		MWW.	I.Com	WW	25°C		0	50	MAA
VOL	Low-level output voltage	, 1111/1.10	$V_{ID} = -100 \text{ mV},$	I _{OL} = 0	-40°C	$C_{O_{2a}}$	0	50	mV
			$00^{1.5}$		85°C	-1 CO	0	50	
		MAN	1007. OM.TV	4	25°C	50	860	4	44
A _{VD}	Large-signal differential amplification	voltage	$V_0 = 1 \text{ V to 6 V},$	$R_L = 1 M\Omega$	-40°C	50	1550		V/mV
	amplification		Too COMP.		85°C	50	585	TV	
		-31	1.100 . COM.	1	25°C	65	97		
CMRR	Common-mode rejection	n ratio	$V_{IC} = V_{ICR}min$		-40°C	60	97	T.I.A.	dB
			M. COL		85°C	60	98	177	
			M. T. CO	VI.	25°C	70	97	TA-	N
ksvr	Supply-voltage rejection	ratio	$V_{DD} = 5 \text{ V to } 10 \text{ V},$	V _O = 1.4 V	-40°C	60	97	0_{Mr} ,	dB
	$(\Delta V_{DD}/\Delta V_{IO})$		100 Y.C.	MTW	85°C	60	98		
		-	WWW.CONY.C	TW	25°C	V 11	29	46	
I_{DD}	Supply current (two amp	olifiers)	V _O = 5 V, No load	$V_{IC} = 5 V$	-40°C		49	86	μΑ
			THO IOUG		85°C		20	36	

[†]Full range is -40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.



^{5.} This range also applies to each input individually.

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electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

W	PARAMETER TLC27L2	M.TW	TEST CON	DITIONS	T _A †	- 17	.C27L2N .C27L7N		UNIT
	TLC27L		W.10			MIN	TYP	MAX	Mr
	11001	TI COZI OM	V _O = 1.4 V,	V _{IC} = 0,	25°C	NA .	1.1	10	mV
V. 0	Input offact voltage	TLC2/L2M	$R_S = 50 \Omega$,	$R_L = 1 M\Omega$	Full range	MAN	-110	12	IIIV
VIO	input onset voitage	TLC27L7M	$V_0 = 1.4 \text{ V},$	$V_{IC} = 0$,	25°C	TAN N	170	500	
	11007	TLC27L7W	$R_S = 50 \Omega$,	$R_L = 1 M\Omega$	Full range	4	- N IX	3750	μV
αΛΙΟ	Average temperature input offset voltage	coefficient of	W WW	W.100Y.CC	25°C to 125°C		1.4	100,	μV/°C
	777 10	OF.	V 0.5.V	100	25°C		0.1	60	pА
lio	Input offset current (s	ee Note 4)	$V_0 = 2.5 V$,	$V_{IC} = 2.5 V$	125°C		1.4	15	nA
		V.CON	WOWN SW	VV 0.50V	25°C		0.6	60	pA
lВ	Input bias current (se	e Note 4)	$V_0 = 2.5 V$,	$V_{IC} = 2.5 V$	125°C	1	9	35	nA
V	Common-mode input	voltage range	OM.TW	MAN.100	25°C	0 N to 4	-0.3 to 4.2	WW	170
VICR	(see Note 5)		OM.TW		Full range	0 to 3.5		WW	V
	V	1005	TIN	MAI	25°C	3.2	4.1	A.	- 1
Vон	High-level output volta	age	$V_{ID} = 100 \text{ mV},$	$R_L = 1 M\Omega$	−55°C	3	4.1	V	V
			COMIT		125°C	3	4.2		UNN
		WWW	OY.	1	25°C	αM^{T}	0	50	-11
V_{OL}	Low-level output volta	ige	$V_{ID} = -100 \text{ mV},$	$I_{OL} = 0$	−55°C		0	50	mV
			COM		125°C	CO_{Mr}	0	50	WIN
		N. T.	100 1. ON'I	4.	25°C	50	500		
A_{VD}	Large-signal differenti amplification	ial voltage	$V_0 = 0.25 \text{ V to 2 V},$	$R_L = 1 M\Omega$	−55°C	25	1000		V/mV
	amplification		V.Inc. COMP.		125°C	25	200	N	V
		44	W.100 . COM.	1.	25°C	65	94	-1	
CMRR	Common-mode reject	tion ratio	V _{IC} = V _{ICR} min		−55°C	60	95	. 44	dB
			M. To OA COM		125°C	60	85	TI	1
	0 1 11 11		MW.100	M	25°C	70	97	-XXI	
KSVR	Supply-voltage rejecti (ΔV _{DD} /ΔV _{IO})	on ratio	$V_{DD} = 5 \text{ V to } 10 \text{ V},$	$V_0 = 1.4 \text{ V}$	−55°C	60	97	CLA	dB
	(7 A DD 17 A IO)	4	WW. COV.CO	WT	125°C	60	98	TI	
			V2 - 2 E V	OV OF V	25°C	N. 3	20	34	N .
IDD	Supply current (two a	mplifiers)	V _O = 2.5 V, No load	$V_{IC} = 2.5 V,$	−55°C	W.100	35	60	μΑ
					125°C	40	14	24	

[†] Full range is -55°C to 125°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.



^{5.} This range also applies to each input individually.

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electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

WW	PARAMETER	N V	TEST CON	DITIONS	TAT		.C27L2I .C27L7I		UNIT
			W.100			MIN	TYP	MAX	
MA	11007.	TI COZI OM	V _O = 1.4 V,	V _{IC} = 0,	25°C	-TVV.1	1.1	10	
, «N	WW. COM	TLC27L2M	$R_S = 50 \Omega$,	$R_L = 1 M\Omega$	Full range	MA	100X	12	mV
VIO	Input offset voltage	TI 0071 7M	V _O = 1.4 V,	V _{IC} = 0,	25°C	JWW.	190	800	
		TLC27L7M	$R_S = 50 \Omega$,	$R_L = 1 M\Omega$	Full range	- NV	Too	4300	μV
αΛΙΟ	Average temperature of input offset voltage	coefficient of	MM.	ON COM	25°C to 125°C	MW.	1.4	V.C	μV/°C
	lanut effect summet (se	- NI-t- 4)	V 5V	V - 5 VON	25°C	-181	0.1	60	pA
liO	Input offset current (se	e Note 4)	$V_0 = 5 V$,	$V_{IC} = 5 V$	125°C	14.	1.8	15	nA
	1	COM	1 v 5 v 1	V ONE CO	25°C	W	0.7	60	pA
ΙΒ	Input bias current (see	Note 4)	$V_O = 5 V$,	$V_{IC} = 5 V$	125°C		10	35	₇ nA
V	Common-mode input v	oltage range	LM MA	M.100X.C	25°C	0 to 9	-0.3 to 9.2	W.100	
VICR	(see Note 5)		TAN M		Full range	0 to 8.5	W	NW.1	10 VY.
	MM	- 100 Y.	WILL	100	25°C	8	8.9	-47	100
V_{OH}	High-level output voltage	ge	$V_{ID} = 100 \text{ mV},$	$R_L = 1 M\Omega$	−55°C	7.8	8.8	NW	V
			OM.1		125°C	7.8	9		W.To.
		100Y.	TITI	W.	25°C	1.4	0	50	W.10
V_{OL}	Low-level output voltag	je .	$V_{ID} = -100 \text{ mV},$	$I_{OL} = 0$	−55°C	WIL	0	50	mV
			COM		125°C		J 0	50	M.M.
	l anno simpol differentia	1	L'OW'I'	-517	25°C	50	860		Wixe
A_{VD}	Large-signal differentia amplification	ii voitage	$V_0 = 1 \text{ V to 6 V},$	$R_L = 1 M\Omega$	−55°C	25	1750		V/mV
	amplification	W.IO.	COM.	VVV	125°C	25	380		
		10.10	COM	7	25°C	65	97		
CMRR	Common-mode rejection	on ratio	V _{IC} = V _{ICR} min		−55°C	60	97		dB
			LOV.COM	N v	125°C	60	91		
	Commissional main atio		Too	- 1	25°C	70	97	NI.	**
ksvr	Supply-voltage rejection (ΔV _{DD} /ΔV _{IO})	ni ratio	$V_{DD} = 5 \text{ V to } 10 \text{ V},$	$V_0 = 1.4 \text{ V}$	−55°C	60	97	4.7	dB
	(¬ , DD , ¬ , IO)	WW	J. WY.CO.	TW	125°C	60	98		*
		TXN	V _O = 5 V,	V _{IC} = 5 V,	25°C	av C	29	46	
I_{DD}	Supply current (two an	nplifiers)	VO = 5 V, No load	VIC = 2V	−55°C	00 -	56	96	μΑ
			J. J. J. Co.		125°C	100%	18	30	

[†] Full range is –55 °C to 125°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

5. This range also applies to each input individually.



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operating characteristics, V_{DD} = 5 V

7	PARAMETER	TEST CO	ONDITIONS	тд	TL TL	C27L2C C27L2A(C27L2B(C27L7C		UNIT
	W.100 COM.	- WW.1	TONI.	~~~	MIN	TYP	MAX	O_{MT} .
	W. TOOX. COMITW	W.	100 r. COM	25°C	1	0.03	0 -	OM
		MM	V _{I(PP)} = 1 V	0°C	111.	0.04	00x.	COM
CD	Class sate at units mainly CO	$R_L = 1 M\Omega$,	TOON.CO	70°C	W	0.03	1005	\//va
SR	Slew rate at unity gain	C _L = 20 pF, See Figure 1	W. Too	25°C		0.03		V/μs
			$V_{I(PP)} = 2.5 V$	0°C		0.03	1.700	-7 CC
		MA	1001.0	70°C		0.02	W 10	01.0
v _n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	$R_S = 20 \Omega$,	25°C		68	VW.	nV/√ Hz
	WW. 11007.0M.		100 1	25°C		5	WIN	100 -
Вом	Maximum output-swing bandwidth	$V_O = V_{OH}$, $R_L = 1 M\Omega$,	C _L = 20 pF, See Figure 1	0°C		6	1	kHz
		1 1 10152,	See rigule r	70°C	W	4.5	MM	V - 2 00
	W.100 CO	VI.	TWW.In	25°C	- 1	85	Wire	11.10
B ₁	Unity-gain bandwidth	V _I = 10 mV, See Figure 3	$C_L = 20 pF,$	0°C	1.1.	100	4	kHz
		occ riguic s	MM	70°C	WILL	65	1/1	-511
	WWW. W.C	ON	, WWW.	25°C	VT	34°	V	MA.
φm	Phase margin	$V_{I} = 10 \text{ mV},$ $C_{L} = 20 \text{ pF},$	f = B ₁ , See Figure 3	0°C	OM	36°		UWW
		Joe - 20 pr.,	Seeguie o	70°C	OMI	30°		- 11

operating characteristics, V_{DD} = 10 V

	PARAMETER	TEST CO	ONDITIONS	TA 10	V.CTL	.C27L20 .C27L2 <i>A</i> .C27L2E .C27L70	AC BC	UNIT
	W. W.	100Y.	IN	N ''	MIN	TYP	MAX	
		JOON CO.	WT	25°C	1007.	0.05	TW	
		V. COL	V _{I(PP)} = 1 V	0°C	oov.	0.05	TW	
SR	Clause rate at units main	$R_L = 1 M\Omega$,	M.1	70°C	Too	0.04	1	1 1//10
)K	Slew rate at unity gain	C _L = 20 pF, See Figure 1	MITW	25°C	0.100	0.04	$M_{I,I}$	V/μs
		VVV.	V _{I(PP)} = 5.5 V	0°C	100	0.05	- N.T.	N
		M. Too	do _M .	70°C	111.5	0.04	$O_{N_{s}}$	CV
1	Equivalent input noise voltage	f = 1 kHz, See Figure 2	$R_S = 20 \Omega$,	25°C	WW.I	68		nV/√ Hz
		VIVI	V.CO.	25°C	N. T.	10019		WIT
MC	Maximum output-swing bandwidth	$V_O = V_{OH}$, $R_L = 1 M\Omega$,	C _L = 20 pF, See Figure 1	∫ 0°C	NWI	1.3	V.CO	kHz
			Gee rigule r	70°C		0.9		
		MAN .	007.	25°C	M.	110		
1	Unity-gain bandwidth	V _I = 10 mV, See Figure 3	$C_L = 20 pF$,	0°C		125		kHz
		See Figure 3	Jun COM	70°C		90		
		N T	V.100 3	25°C	İ	38°		
m	Phase margin	$V_{l} = 10 \text{ mV},$ $C_{L} = 20 \text{ pF},$	f = B ₁ , See Figure 3	0°C		40°		
	-	C _L = 20 μr,	See Figure 5	70°C		34°		



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operating characteristics, $V_{DD} = 5 \text{ V}$

PARAMETER		TEST CONDITIONS		TA	TLC27L2I TLC27L2AI TLC27L2BI TLC27L7I			UNIT
		WW.100	COM		MIN TYP		MAX	W.
V	100 Y. COM.TW	W. 100	COMIT	25°C	XXIVI.	0.03	COL	7.1
		1/1/1/100	V _{I(PP)} = 1 V	−40°C	1	0.04		WIN
CD	CONN. IV. CONT.	$R_L = 1 M\Omega$,	Y.CON.	√ 85°C	MM.	0.03	V.C	NA T
SR	Slew rate at unity gain	C _L = 20 pF, See Figure 1	J. COM.	25°C		0.03	N.C	V/μs
		Joseph Inguist I	$V_{I(PP)} = 2.5 V$	−40°C		0.04	-1 (OM.
		MM	100 Y.Co	85°C	Ma	0.02	00 x.	Mon
٧n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	$R_S = 20 \Omega$,	25°C	W	68	700Å	nV/√ Hz
	MA TIOOTO MITH	No.	1001.	25°C	1	5	V.100	- c0
ВОМ	Maximum output-swing bandwidth	$V_O = V_{OH}$, $R_L = 1 M\Omega$,	C _L = 20 pF, See Figure 1	-40°C		7	×1 10	kHz
		KL = 1 10152,	See Figure 1	85°C		4	A4	NY.C'
	A. 100, COM: 1.	7	11 W. 100	25°C	1	85	MN.	~1 C
В1	Unity-gain bandwidth	V _I = 10 mV, See Figure 3	$C_L = 20 pF$,	-40°C		130	W	kHz
		See Figure 3	WW 1007	85°C	N	55	A.	100X
	ZIMM. IN COM	-XXI	MMM	25°C		34° <	MWA	4007
φm	Phase margin	$V_{I} = 10 \text{ mV},$ $C_{L} = 20 \text{ pF},$	f = B ₁ , See Figure 3	-40°C	-XX	38°	Wire	W.In
		OL = 20 pr,	occ rigule 3	85°C	1.7.	29°	44	W.10

operating characteristics, V_{DD} = 10 V

	PARAMETER NYW 100 Y	TEST CONDITIONS		TA Y	TLC27L2I TLC27L2AI TLC27L2BI TLC27L7I	UNIT
	WW. 1003	MIM		100 x	MIN TYP N	IAX
	MAL	ON COST		25°C	0.05	
		COM.	V _{I(PP)} = 1 V	-40°C	0.06	17
SR	Class rate at switz ratio	$R_L = 1 M\Omega$,		85°C	0.03	Mus
	Slew rate at unity gain	C _L = 20 pF, See Figure 1	1	25°C	0.04	V/μs
		OOY GOOD	$V_{I(PP)} = 5.5 V$	-40°C	0.05	N
		A. LOU		85°C	0.03	W
v _n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	$R_S = 20 \Omega$,	25°C	68	nV/√Hz
ВОМ	VVV	VIV.	C _L = 20 pF, See Figure 1	25°C	1001.01	
	Maximum output-swing bandwidth	VO = VOH,		-40°C	1.4	kHz
		$R_L = 1 M\Omega$,		85°C	0.8	
B ₁	Unity-gain bandwidth $ \begin{array}{c} V_I = 10 \text{ mV}, & C_L = 20 \text{ pF}, \\ See \text{ Figure 3} & -40^{\circ}\text{C} \\ \hline \end{array} $	1003	WI.M.	25°C	110	
		155	kHz			
		See Figure 3	COM.	85°C	80	
		W 10	U 3	25°C	38°	
φm	Phase margin	$V_{I} = 10 \text{ mV},$ $C_{L} = 20 \text{ pF},$	f = B ₁ , See Figure 3	-40°C	42°	
		JE = 20 pi,	2301 19410 0	85°C_	32°	



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operating characteristics, $V_{DD} = 5 \text{ V}$

PARAMETER		TEST CO	TEST CONDITIONS		TLC27L2M TLC27L7M			UNIT
		W.10	M. TOO TOWN			TYP	MAX	M·
	WW TIOOY.	War and I	V _{I(PP)} = 1 V	25°C	NA .	0.03) } .	OM_{T}
	$R_L = 1 M\Omega$,	MMM		−55°C	MA	0.04	10 X .	M
0.0		No.CON	125°C	W	0.02	on Y.	White	
SR	Slew rate at unity gain	C _L = 20 pF, See Figure 1	ATON TOOM	25°C	-31	0.03	To-	V/μs
			$V_{I(PP)} = 2.5 V$	−55°C		0.04	700.	- 001
		N MAN	100X.CO	125°C		0.02	x1 100	1.00
v _n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	$R_S = 20 \Omega$,	25°C	T	68	W.10	nV/√ Hz
ВОМ	WWW. 100Y.Co. II T	IN N	C _L = 20 pF, See Figure 1	25°C		5	-TXV .1	kHz
	Maximum output-swing bandwidth	$V_O = V_{OH}$, $R_L = 1 M\Omega$,		−55°C		8	MA	
		RL = 1 IVIS 2		125°C	N	3	MA	. 007
	M. 100	11:1	1. 100	25°C	- 41	85		1.100
B ₁	Unity-gain bandwidth	V _I = 10 mV, See Figure 3	$C_L = 20 \text{ pF},$	−55°C	T.A.	140	W	kHz
		See Figure 3	WWW	125°C	WT	45	MA	10
	TINN. To	Opposition	· MW.	25°C	TV	34°	W	144.
φm	Phase margin	$V_{I} = 10 \text{ mV},$ $C_{L} = 20 \text{ pF},$	f = B ₁ , See Figure 3	−55°C	Mr.	39°		WW.
		or zobi,	occi igaic o	125°C	MIL	25°	N.	TIN

operating characteristics, V_{DD} = 10 V

	PARAMETER	TEST CONDITIONS		TAOOY	TLC27L2M TLC27L7M			UNIT
		M.Com	N N	N 11 100	MIN	TYP	MAX	
	MM.i.	V.COM	D W	25°C	V.Co	0.05	N	V
		OM.	V _{I(PP)} = 1 V	−55°C	ST CC	0.06		
CD	Clausesta at units anim	$R_L = 1 M\Omega$,		MIN TYP MA	1) //ws		
SR	Slew rate at unity gain	C _L = 20 pF, See Figure 1	WI	25°C	100 X.C	0.04	IM	V/μs
		GCC 1 iguic 1	V _{I(PP)} = 5.5 V	−55°C	You.	0.06	TW	İ
		M.100 T. C.C.		125°C	1.10	0.03	1.	J
Vn	Equivalent input noise voltage	f = 1 kHz, See Figure 2	Rs = 20Ω ,	25°C	W.100	68	M.I	nV/√Hz
	-117	$V_O = V_{OH}$, $R_L = 1 M\Omega$,	COMP.	25°C	M.	1	Oh	TW
Вом	Maximum output-swing bandwidth		C _L = 20 pF,	−55°C	M.M.T.	1.5	$^{\prime}O_{M_I}$	kHz
		$K_{L} = 1 \text{ IVIS2},$	See Figure 1	125°C	0.05 0.06 0.03 0.04 0.06 0.03 68 1 1.5 0.7 110 165 70 38° 43°	TIM		
B ₁		$V_{I} = 10 \text{ mV}, \qquad C_{L} = 20 \text{ pF}, \qquad -55^{\circ}\text{C}$ 165 See Figure 3	C _L = 20 pF,	25°C	NA.	110		TW
	Unity-gain bandwidth			√ -55°C	WWW	165	V.CO	kHz
			70		1			
φm		V _I = 10 mV, C _L = 20 pF,	001.	25°C	44.	38°		
	Phase margin		f = B ₁ , See Figure 3	−55°C		43°		1
		OL = 20 pi,	Joe rigule 3	125°C		29°		1



PARAMETER MEASUREMENT INFORMATION

single-supply versus split-supply test circuits

Because the TLC27L2 and TLC27L7 are optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The use of either circuit gives the same result.

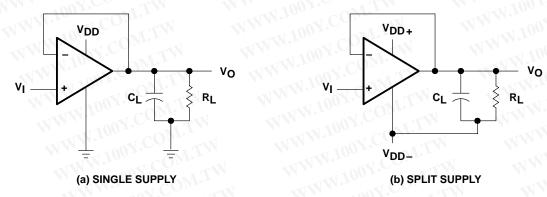


Figure 1. Unity-Gain Amplifier

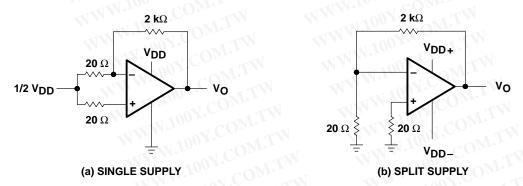


Figure 2. Noise-Test Circuit

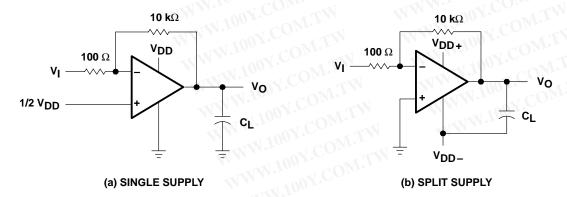


Figure 3. Gain-of-100 Inverting Amplifier

PARAMETER MEASUREMENT INFORMATION

input bias current

Because of the high input impedance of the TLC27L2 and TLC27L7 operational amplifiers, attempts to measure the input bias current can result in erroneous readings. The bias current at normal room ambient temperature is typically less than 1 pA, a value that is easily exceeded by leakages on the test socket. Two suggestions are offered to avoid erroneous measurements:

- Isolate the device from other potential leakage sources. Use a grounded shield around and between the device inputs (see Figure 4). Leakages that would otherwise flow to the inputs are shunted away.
- Compensate for the leakage of the test socket by actually performing an input bias current test (using a picoammeter) with no device in the test socket. The actual input bias current can then be calculated by subtracting the open-socket leakage readings from the readings obtained with a device in the test socket.

One word of caution: many automatic testers as well as some bench-top operational amplifier testers use the servo-loop technique with a resistor in series with the device input to measure the input bias current (the voltage drop across the series resistor is measured and the bias current is calculated). This method requires that a device be inserted into the test socket to obtain a correct reading; therefore, an open-socket reading is not feasible using this method.

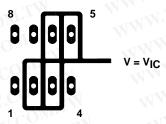


Figure 4. Isolation Metal Around Device Inputs (JG and P packages)

low-level output voltage

To obtain low-supply-voltage operation, some compromise was necessary in the input stage. This compromise results in the device low-level output being dependent on both the common-mode input voltage level as well as the differential input voltage level. When attempting to correlate low-level output readings with those quoted in the electrical specifications, these two conditions should be observed. If conditions other than these are to be used, please refer to Figures 14 through 19 in the Typical Characteristics of this data sheet.

input offset voltage temperature coefficient

Erroneous readings often result from attempts to measure temperature coefficient of input offset voltage. This parameter is actually a calculation using input offset voltage measurements obtained at two different temperatures. When one (or both) of the temperatures is below freezing, moisture can collect on both the device and the test socket. This moisture results in leakage and contact resistance, which can cause erroneous input offset voltage readings. The isolation techniques previously mentioned have no effect on the leakage since the moisture also covers the isolation metal itself, thereby rendering it useless. It is suggested that these measurements be performed at temperatures above freezing to minimize error.



PARAMETER MEASUREMENT INFORMATION

full-power response

Full-power response, the frequency above which the operational amplifier slew rate limits the output voltage swing, is often specified two ways: full-linear response and full-peak response. The full-linear response is generally measured by monitoring the distortion level of the output while increasing the frequency of a sinusoidal input signal until the maximum frequency is found above which the output contains significant distortion. The full-peak response is defined as the maximum output frequency, without regard to distortion, above which full peak-to-peak output swing cannot be maintained.

Because there is no industry-wide accepted value for significant distortion, the full-peak response is specified in this data sheet and is measured using the circuit of Figure 1. The initial setup involves the use of a sinusoidal input to determine the maximum peak-to-peak output of the device (the amplitude of the sinusoidal wave is increased until clipping occurs). The sinusoidal wave is then replaced with a square wave of the same amplitude. The frequency is then increased until the maximum peak-to-peak output can no longer be maintained (Figure 5). A square wave is used to allow a more accurate determination of the point at which the maximum peak-to-peak output is reached.

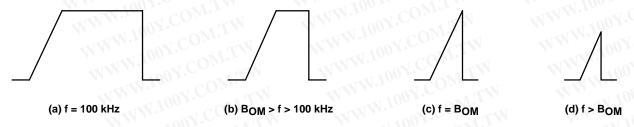


Figure 5. Full-Power-Response Output Signal

test time

Inadequate test time is a frequent problem, especially when testing CMOS high-volume, short-test-time environment. Internal capacitances are inherently higher in CMOS devices and require longer test times than their bipolar and BiFET counterparts. The problem becomes more pronounced with reduced supply levels and lower temperatures.



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TYPICAL CHARACTERISTICS

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Table of Graphs

N.100	COM.I	COM.	FIGURE	
V _{IO}	Input offset voltage	Distribution	6, 7	
ανιο	Temperature coefficient of input offset voltage	Distribution	8, 9	
Vон	High-level output voltage	vs High-level output current vs Supply voltage vs Free-air temperature	10, 11 12 13	
V _{OL}	Low-level output voltage	vs Differential input voltage vs Free-air temperature vs Low-level output current	14,16 15,17 18, 19	
AVD	Large-signal differential voltage amplification	vs Supply voltage vs Free-air temperature vs Frequency	20 21 32, 33	
I _{IB}	Input bias current	vs Free-air temperature	22 C	
lio	Input offset current	vs Free-air temperature	22	
VIС	Common-mode input voltage	vs Supply voltage	23	
lDD	Supply current	vs Supply voltage vs Free-air temperature	24 25	
SR	Slew rate	vs Supply voltage vs Free-air temperature	26 27	
	Normalized slew rate	vs Free-air temperature	28	
V _{O(PP)}	Maximum peak-to-peak output voltage	vs Frequency	29	
B ₁	Unity-gain bandwidth	vs Free-air temperature vs Supply voltage	30 31	
φm	Phase margin	vs Supply voltage vs Free-air temperature vs Capacitive Load	34 35 36	
٧ _n	Equivalent input noise voltage	vs Frequency	37	
	Phase shift	vs Frequency	32, 33	

TYPICAL CHARACTERISTICS

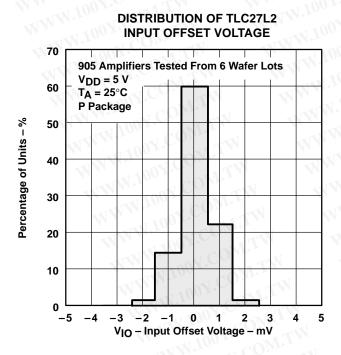


Figure 6

DISTRIBUTION OF TLC27LC AND TLC27L7 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT

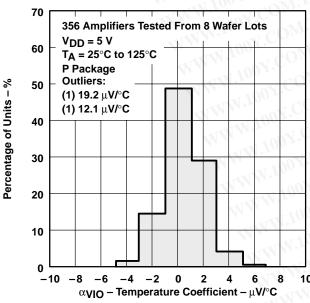


Figure 8

DISTRIBUTION OF TLC27L2 INPUT OFFSET VOLTAGE

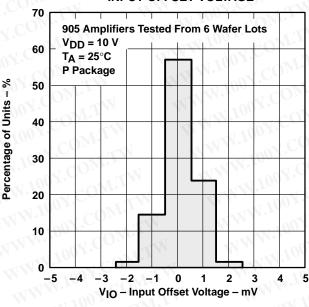


Figure 7

DISTRIBUTION OF TLC27LC AND TLC27L7 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT

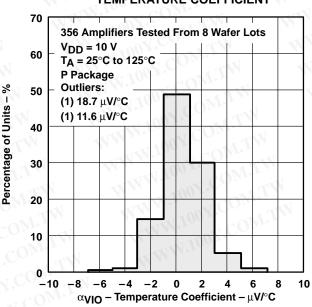


Figure 9

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TYPICAL CHARACTERISTICS[†]

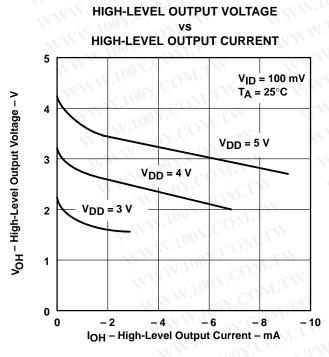


Figure 10

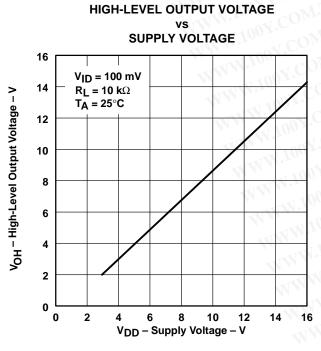


Figure 12

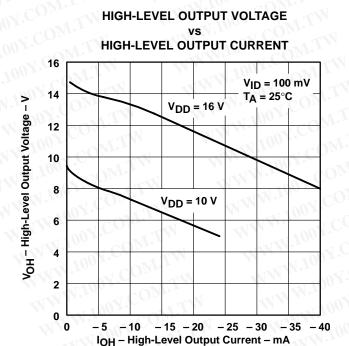


Figure 11

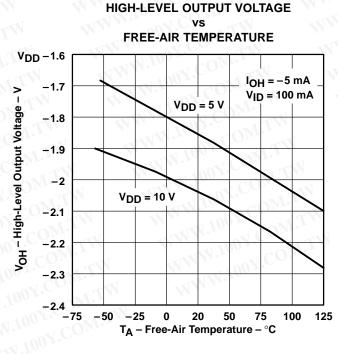
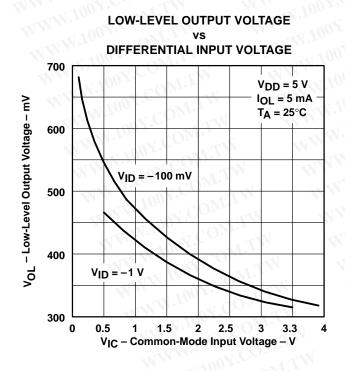


Figure 13

[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.



TYPICAL CHARACTERISTICS†





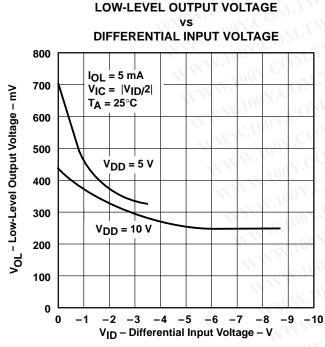


Figure 16

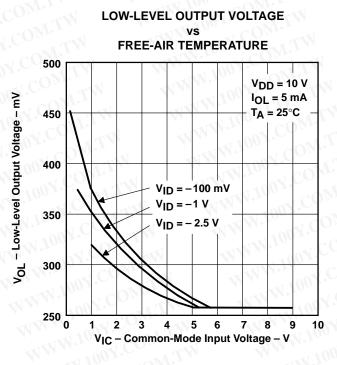


Figure 15

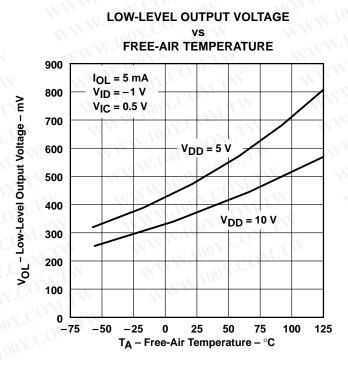


Figure 17

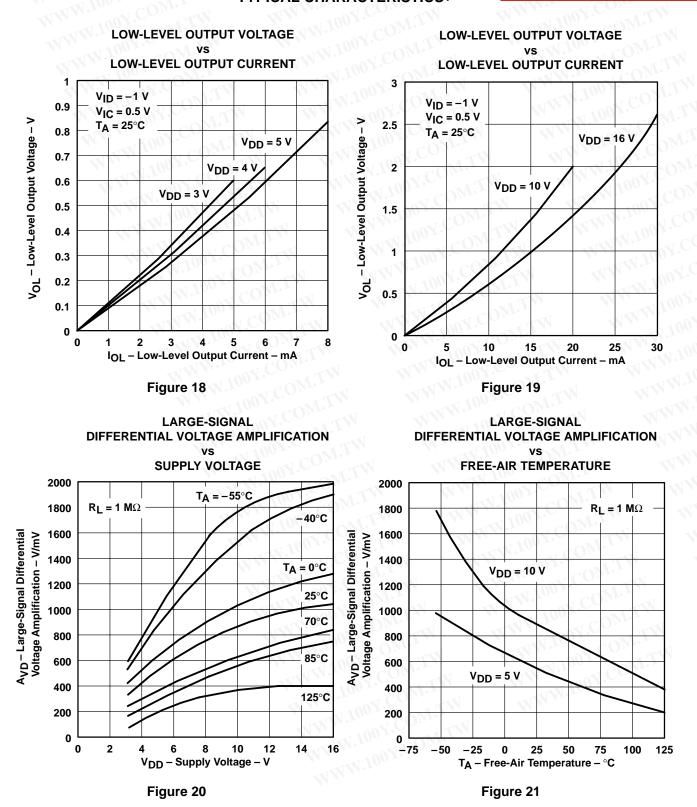
[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.



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TYPICAL CHARACTERISTICS[†]



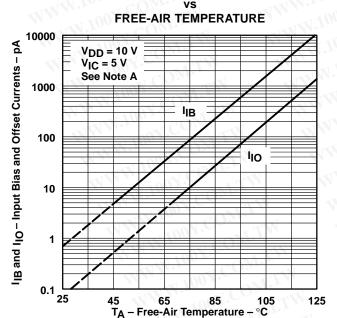
[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.



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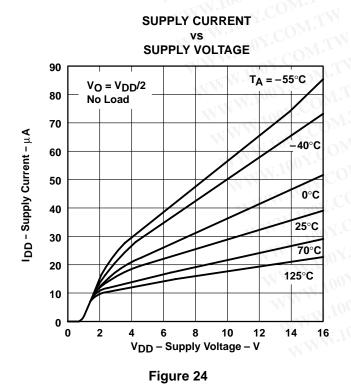
TYPICAL CHARACTERISTICS[†]

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT



NOTE A: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

Figure 22



COMMON-MODE INPUT VOLTAGE POSITIVE LIMIT

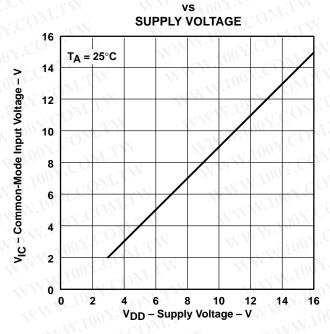


Figure 23



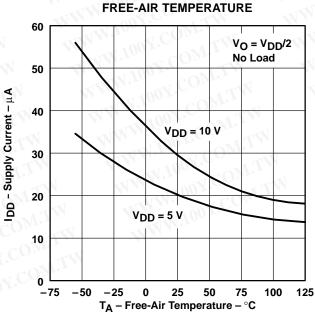


Figure 25

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

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 $R_L = 1 M\Omega$

 $C_L = 20 pF$

See Figure 1

 $V_{DD} = 10 V$ $V_{I(PP)} = 1 V_{\perp}$

> 100 125

 $A_V = 1$

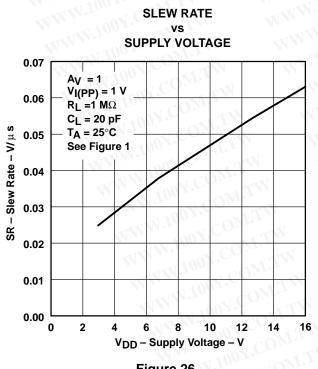
TYPICAL CHARACTERISTICS[†]

0.07

0.06

0.05

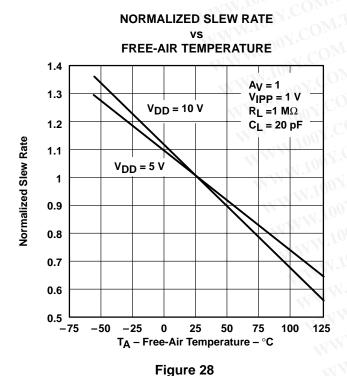
0.04



Slew Rate - V/ µ s 0.03 $V_{DD} = 5 V$ 0.02 V_{I(PP)} = 1 V $V_{DD} = 5 V$ 0.01 $V_{I(PP)} = 2.5 V$ 0.00 -50-250 25 50 75

Figure 26

Figure 27



MAXIMUM-PEAK-TO-PEAK OUTPUT VOLTAGE

TA - Free-Air Temperature - °C

SLEW RATE

vs FREE-AIR TEMPERATURE

 $V_{DD} = 10 \text{ V}$

 $V_{I(PP)} = 5.5 V$

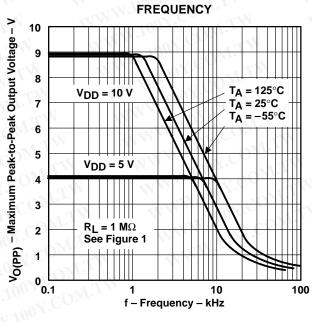


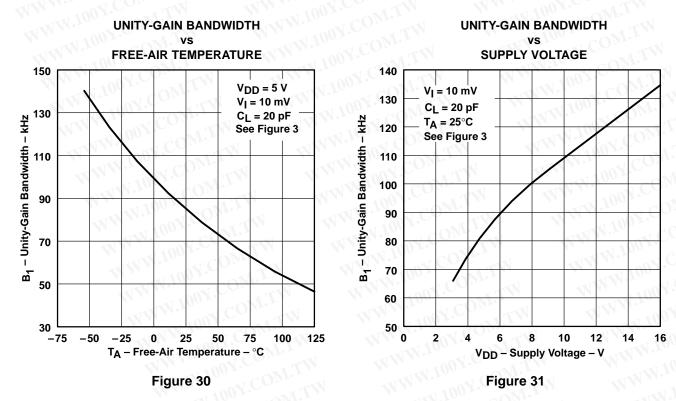
Figure 29

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

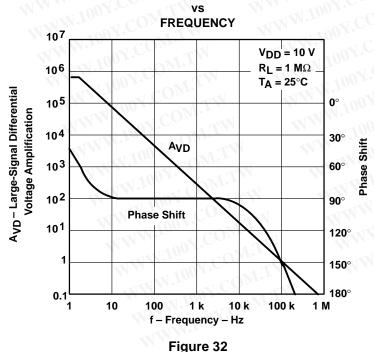


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TYPICAL CHARACTERISTICS[†]



LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT



† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

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TYPICAL CHARACTERISTICS[†]

LARGE-SIGNAL DIFFERENTIAL VOLTAGE **AMPLIFICATION AND PHASE SHIFT**

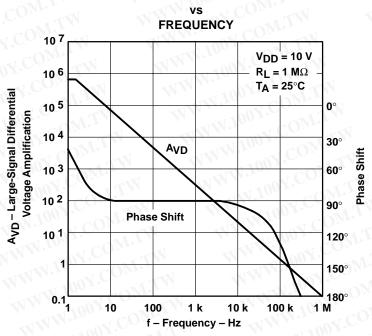
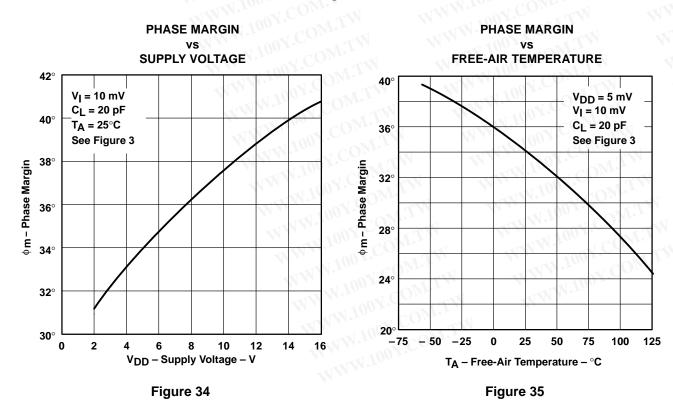


Figure 33



† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.



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TYPICAL CHARACTERISTICS

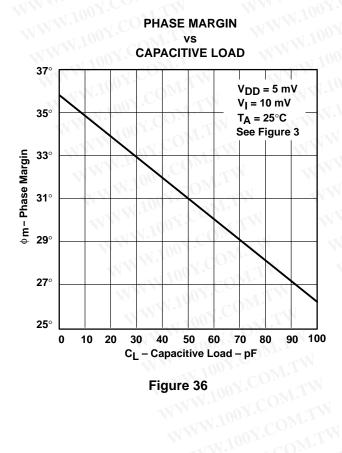


Figure 36

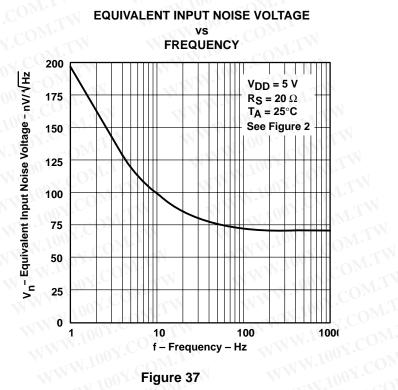


Figure 37

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APPLICATION INFORMATION

single-supply operation

While the TLC27L2 and TLC27L7 perform well using dual power supplies (also called balanced or split supplies), the design is optimized for single-supply operation. This design includes an input common-mode voltage range that encompasses ground as well as an output voltage range that pulls down to ground. The supply voltage range extends down to 3 V (C-suffix types), thus allowing operation with supply levels commonly available for TTL and HCMOS; however, for maximum dynamic range, 16-V single-supply operation is recommended.

Many single-supply applications require that a voltage be applied to one input to establish a reference level that is above ground. A resistive voltage divider is usually sufficient to establish this reference level (see Figure 38). The low input bias current of the TLC27L2 and TLC27L7 permits the use of very large resistive values to implement the voltage divider, thus minimizing power consumption.

The TLC27L2 and TLC27L7 work well in conjunction with digital logic; however, when powering both linear devices and digital logic from the same power supply, the following precautions are recommended:

- Power the linear devices from separate bypassed supply lines (see Figure 39); otherwise, the linear device supply rails can fluctuate due to voltage drops caused by high switching currents in the digital logic.
- 2. Use proper bypass techniques to reduce the probability of noise-induced errors. Single capacitive decoupling is often adequate; however, high-frequency applications may require RC decoupling.

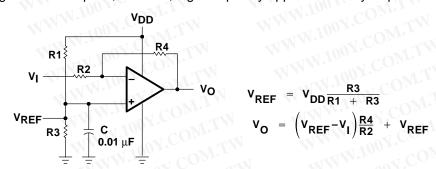


Figure 38. Inverting Amplifier With Voltage Reference

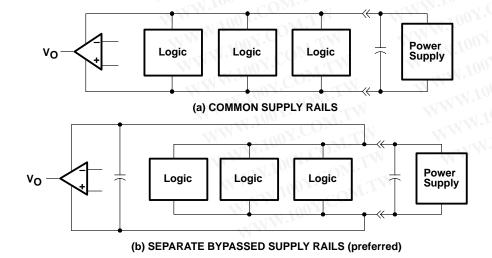


Figure 39. Common Versus Separate Supply Rails



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TLC27L2, TLC27L2A, TLC27L2B, TLC27L7 LinCMOS™ PRECISION DUAL OPERATIONAL AMPLIFIERS

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APPLICATION INFORMATION

input characteristics

The TLC27L2 and TLC27L7 are specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction. Exceeding this specified range is a common problem, especially in single-supply operation. Note that the lower range limit includes the negative rail, while the upper range limit is specified at V_{DD} –1 V at T_A = 25°C and at V_{DD} –1.5 V at all other temperatures.

The use of the polysilicon-gate process and the careful input circuit design gives the TLC27L2 and TLC27L7 very good input offset voltage drift characteristics relative to conventional metal-gate processes. Offset voltage drift in CMOS devices is highly influenced by threshold voltage shifts caused by polarization of the phosphorus dopant implanted in the oxide. Placing the phosphorus dopant in a conductor (such as a polysilicon gate) alleviates the polarization problem, thus reducing threshold voltage shifts by more than an order of magnitude. The offset voltage drift with time has been calculated to be typically 0.1 μ V/month, including the first month of operation.

Because of the extremely high input impedance and resulting low bias current requirements, the TLC27L2 and TLC27L7 are well suited for low-level signal processing; however, leakage currents on printed circuit boards and sockets can easily exceed bias current requirements and cause a degradation in device performance. It is good practice to include guard rings around inputs (similar to those of Figure 4 in the Parameter Measurement Information section). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input (see Figure 40).

Unused amplifiers should be connected as grounded unity-gain followers to avoid possible oscillation.

noise performance

The noise specifications in operational amplifier circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias current requirements of the TLC27L2 and TLC27L7 result in a very low noise current, which is insignificant in most applications. This feature makes the devices especially favorable over bipolar devices when using values of circuit impedance greater than $50 \text{ k}\Omega$, since bipolar devices exhibit greater noise currents.

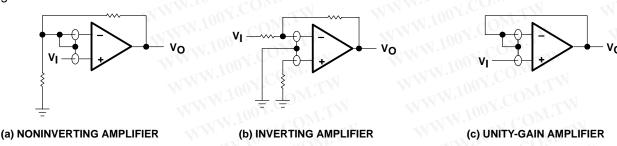


Figure 40. Guard-Ring Schemes

output characteristics

The output stage of the TLC27L2 and TLC27L7 is designed to sink and source relatively high amounts of current (see typical characteristics). If the output is subjected to a short-circuit condition, this high current capability can cause device damage under certain conditions. Output current capability increases with supply voltage.

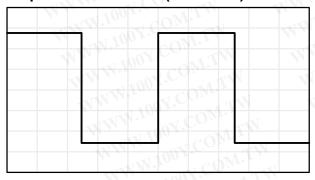
All operating characteristics of the TLC27L2 and TLC27L7 were measured using a 20-pF load. The devices drive higher capacitive loads; however, as output load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation (see Figure 41). In many cases, adding a small amount of resistance in series with the load capacitance alleviates the problem.



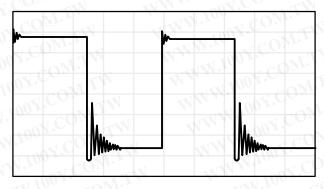
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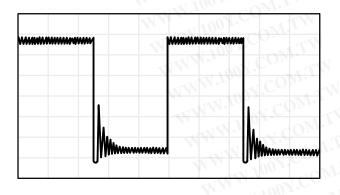
output characteristics (continued)



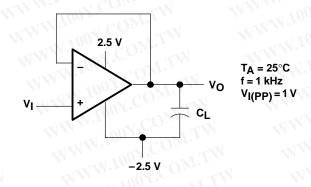
(a) C_L = 20 pF, R_L = NO LOAD



(b) $C_L = 260 \text{ pF}, R_L = NO \text{ LOAD}$



(c) $C_L = 310 \text{ pF}$, $R_L = NO \text{ LOAD}$



(d) TEST CIRCUIT

Figure 41. Effect of Capacitive Loads and Test Circuit

Although the TLC27L2 and TLC27L7 possess excellent high-level output voltage and current capability, methods for boosting this capability are available, if needed. The simplest method involves the use of a pullup resistor (R_P) connected from the output to the positive supply rail (see Figure 42). There are two disadvantages to the use of this circuit. First, the NMOS pulldown transistor N4 (see equivalent schematic) must sink a comparatively large amount of current. In this circuit, N4 behaves like a linear resistor with an on-resistance between approximately $60~\Omega$ and $180~\Omega$, depending on how hard the operational amplifier input is driven. With very low values of R_P, a voltage offset from 0 V at the output occurs. Second, pullup resistor R_P acts as a drain load to N4 and the gain of the operational amplifier is reduced at output voltage levels where N5 is not supplying the output current.

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APPLICATION INFORMATION

output characteristics (continued)

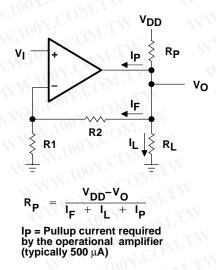


Figure 42. Resistive Pullup to Increase VOH

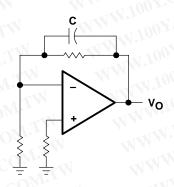


Figure 43. Compensation for Input Capacitance

feedback

Operational amplifier circuits nearly always employ feedback, and since feedback is the first prerequisite for oscillation, some caution is appropriate. Most oscillation problems result from driving capacitive loads (discussed previously) and ignoring stray input capacitance. A small-value capacitor connected in parallel with the feedback resistor is an effective remedy (see Figure 43). The value of this capacitor is optimized empirically.

electrostatic discharge protection

The TLC27L2 and TLC27L7 incorporate an internal electrostatic discharge (ESD) protection circuit that prevents functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2. Care should be exercised, however, when handling these devices, as exposure to ESD may result in the degradation of the device parametric performance. The protection circuit also causes the input bias currents to be temperature dependent and have the characteristics of a reverse-biased diode.

latch-up

Because CMOS devices are susceptible to latch-up due to their inherent parasitic thyristors, the TLC27L2 and TLC27L7 inputs and outputs were designed to withstand -100-mA surge currents without sustaining latch-up; however, techniques should be used to reduce the chance of latch-up whenever possible. Internal protection diodes should not, by design, be forward biased. Applied input and output voltage should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 μ F typical) located across the supply rails as close to the device as possible.

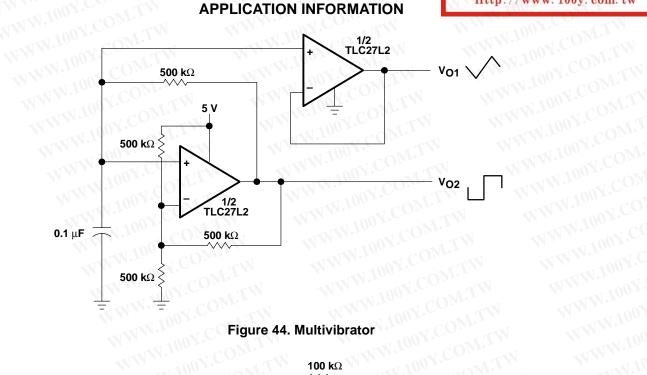
The current path established if latch-up occurs is usually between the positive supply rail and ground and can be triggered by surges on the supply lines and/or voltages on either the output or inputs that exceed the supply voltage. Once latch-up occurs, the current flow is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor and usually results in the destruction of the device. The chance of latch-up occurring increases with increasing temperature and supply voltages.



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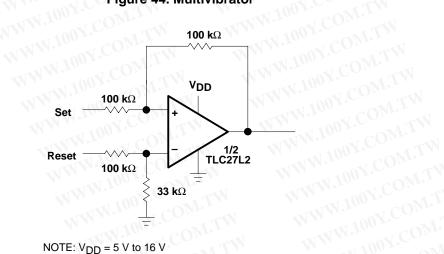


Figure 45. Set/Reset Flip-Flop

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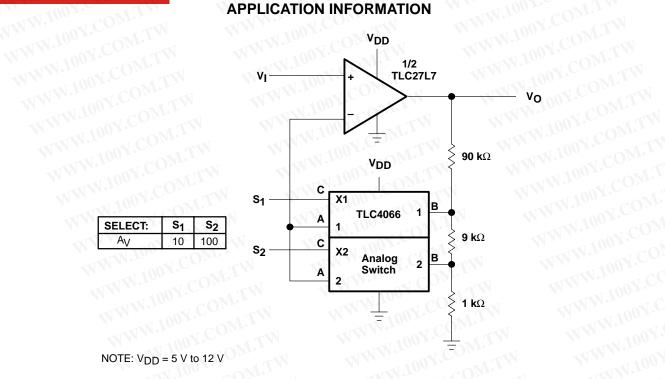
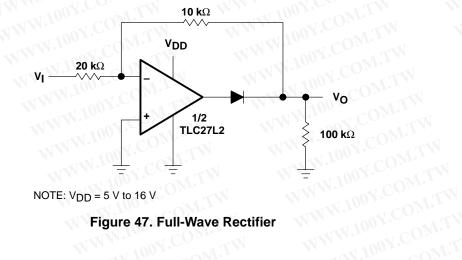


Figure 46. Amplifier With Digital Gain Selection

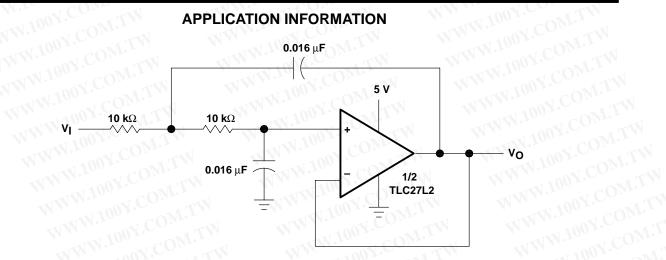


NOTE: VDD = 5 V to 16 V

Figure 47. Full-Wave Rectifier WWW.100Y.CC

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APPLICATION INFORMATION



NOTE: Normalized to $f_C = 1$ kHz and $R_L = 10$ k Ω

Figure 48. Two-Pole Low-Pass Butterworth Filter

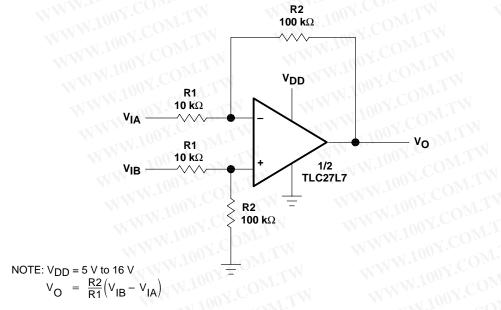


Figure 49. Difference Amplifier

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