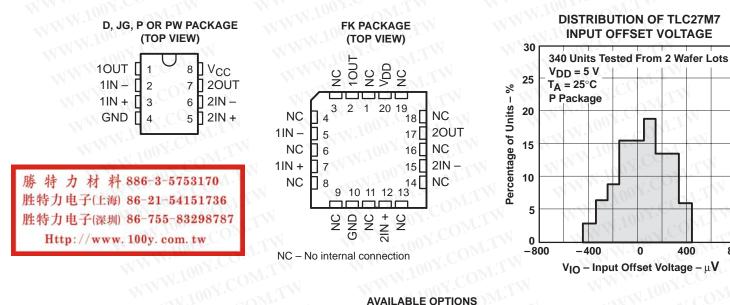
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- **Trimmed Offset Voltage:** TLC27M7 ... 500 μV Max at 25°C, $V_{DD} = 5 V$
- Input Offset Voltage Drift ... Typically 0.1 µV/Month, Including the First 30 Days
- Wide Range of Supply Voltages Over **Specified Temperature Ranges:** 0°C to 70°C . . . 3 V to 16 V -40°C to 85°C ... 4 V to 16 V -55°C to 125°C . . . 4 V to 16 V
- Single-Supply Operation
- **Common-Mode Input Voltage Range** Extends Below the Negative Rail (C-Suffix, I-Suffix Types)

- Low Noise . . . Typically 32 nV/ \sqrt{Hz} at f = 1 kHz
- Low Power . . . Typically 2.1 mW at 25°C, $V_{DD} = 5 V$
- **Output Voltage Range Includes Negative** Rail
- High Input impedance . . . $10^{12} \Omega$ Typ
- **ESD-Protection Circuitry**
- **Small-Outline Package Option Also** Available in Tape and Reel
- Designed-In Latch-Up Immunity



WW 100	M. M	V.M. W.	1001.00	PACKAGE	N.V.	00 CONT.
TA	V _{IO} max AT 25°C	SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)	TSSOP (PW)
W TINI	500 μV	TLC27M7CD		COM-	TLC27M7CP	1.10° = CO
0°C to 70°C	2 mV	TLC27M2BCD	WW = 100Y	The second	TLC27M2BCP	N.1001.C
0.0 10 10.0	5 mV	TLC27M2ACD	WW	VT - VO.	TLC27M2ACP	THOY.CC
	10 mV	TLC27M2CD	WWW.10	V.CON.	TLC27M2CP	TLC27M2CPW
VV ·	500 μV	TLC27M7ID	TW.10	COM-	TLC27M7IP	WW.Lo
-40°C to 85°C	2 mV	TLC27M2BID	N <u>N</u>	T.Mor. TOG	TLC27M2BIP	W-1001.
-40°C to 85°C	5 mV	TLC27M2AID	AT WWW	ON.COM	TLC27M2AIP	NN -100Y
	10 mV	TLC27M2ID	WWW	N-CONT	TLC27M2IP	TLC27M2IPW
-55°C to 125°C	500 μV	TLC27M7MD	TLC27M7MFK	TLC27M7MJG	TLC27M7MP	WT W
-55°C 10 125°C	10 mV	TLC27M2MD	TLC27M2MFK	TLC27M2MJG	TLC27M2MP	W.10

The D and PW package is available taped and reeled. Add R suffix to the device type (e.g., TLC27M7CDR

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0

400

800

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description

The TLC27M2 and TLC27M7 dual operational amplifiers combine a wide range of input offset voltage grades with low offset voltage drift, high input impedance, low noise, and speeds approaching that of general-purpose bipolar devices. These devices use Texas Instruments silicon-gate LinCMOS technology, which provides offset voltage stability far exceeding the stability available with conventional metal-gate processes.

The extremely high input impedance, low bias currents, and high slew rates make these cost-effective devices ideal for applications which have previously been reserved for general-purpose bipolar products, but with only a fraction of the power consumption. Four offset voltage grades are available (C-suffix and I-suffix types), ranging from the low-cost TLC27M2 (10 mV) to the high-precision TLC27M7 (500 μ V). These advantages, in combination with good common-mode rejection and supply voltage rejection, make these devices a good choice for new state-of-the-art designs as well as for upgrading existing designs.

In general, many features associated with bipolar technology are available on LinCMOS[™] operational amplifiers, without the power penalties of bipolar technology. General applications such as transducer interfacing, analog calculations, amplifier blocks, active filters, and signal buffering are easily designed with the TLC27M2 and TLC27M7. The devices also exhibit low voltage single-supply operation, making them ideally suited for remote and inaccessible battery-powered applications. The common-mode input voltage range includes the negative rail.

A wide range of packaging options is available, including small-outline and chip-carrier versions for high-density system applications.

The device inputs and outputs are designed to withstand -100-mA surge currents without sustaining latch-up.

The TLC27M2 and TLC27M7 incorporate internal ESD-protection circuits that prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parametric performance.

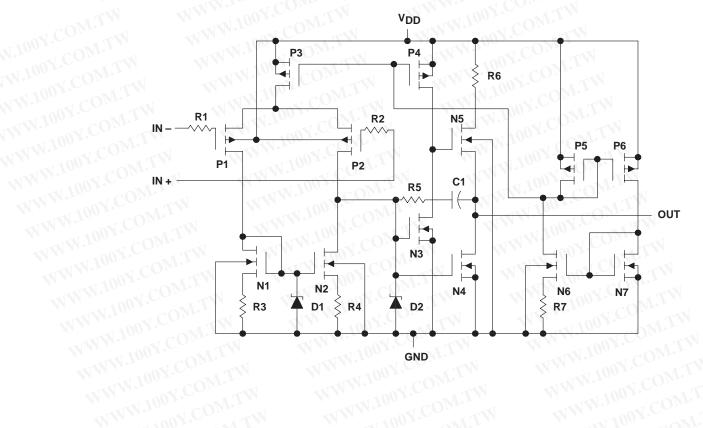
The C-suffix devices are characterized for operation from 0° C to 70° C. The I-suffix devices are characterized for operation from -40° C to 85° C. The M-suffix devices are characterized for operation over the full military temperature range of -55° C to 125° C.

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equivalent schematic (each amplifier) W.100Y.COM.TW

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WT.M

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V _{DD} (see Note 1)	
Differential input voltage, VID (see Note 2)	
Input voltage range, V _I (any input)	
Input current, I	±5 mĀ
Output current, I _O (each output)	±30 mA
Total current into V _{DD}	
Total current out of GND	
Duration of short-circuit current at (or below) 25°C (see Note 3)	Unlimited
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature, T _A : C suffix	0°C to 70°C
I suffix	–40°C to 85°C
M suffix	–55°C to 125°C
Storage temperature range	–65°C to 150°C
Case temperature for 60 seconds: FK package	
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D o	or P package 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG	package 300°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.

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2. Differential voltages are at IN+ with respect to IN-.

3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded (see application section).

		DISSIPATION F	RATING TABLE		
PACKAGE	T _A ≤ 25°C POWER RATING	DERATING FACTOR ABOVE $T_A = 25^{\circ}C$	T _A = 70°C POWER RATING	T _A = 85°C POWER RATING	T _A = 125°C POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	100Y.C
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
Р	1000 mW	8.0 mW/°C	640 mW	520 mW	

recommended operating conditions

	COMP.	C SU	FFIX	ISU	FIX	M SU	FFIX	LINUT
		MIN	MAX	MIN	MAX	MIN	MAX	UNIT
Supply voltage, V _{DD}	Dr. M.TW	3	16	4	16	4	16	V
	$V_{DD} = 5 V$	-0.2	3.5	-0.2	3.5	0	3.5	100 ² .
Common-mode input voltage, VIC	V _{DD} = 10 V	-0.2	8.5	-0.2	8.5	0	8.5	V
Operating free-air temperature, TA	The COM'r	0	70	-40	85	-55	125	°C

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electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

	PARAMETER	OY.COM.T	TEST CON	DITIONS	τ _A †	TL TL	.C27M2(.C27M2) .C27M2I .C27M2I	AC BC	UNIT
M.TV		.1001. COM		WW.100 1	TCOM.1	MIN	TYP	MAX	
TIM	W WW	TLC27M2C	V _O = 1.4 V,	V _{IC} = 0,	25°C		1.1	10	
		TLC27M2C	R _S = 50 Ω,	$R_{I} = 100 \text{ k}\Omega$	Full range	L.M.		12	mV
		TLC27M2AC	V _O = 1.4 V,	$V_{IC} = 0,$	25°C	W	0.9	5	IIIV
Vie	Input offset voltage	TLCZ/WIZAC	R _S = 50 Ω,	$R_{I} = 100 \text{ k}\Omega$	Full range	1. 1 		6.5	
VIO	input onset voltage	TLC27M2BC	V _O = 1.4 V,	$V_{IC} = 0,$	25°C	1.1	220	2000	
		TECZTWIZBC	R _S = 50 Ω,	$R_{I} = 100 \text{ k}\Omega$	Full range	TIM		3000	μV
		TLC27M7C	V _O = 1.4 V,	$V_{IC} = 0,$	25°C	Ju-	185	500	μν
J1	ONL'I'	TECZTIMITC	R _S = 50 Ω,	R _I = 100 kΩ	Full range	OM.,		1500	
αΛΙΟ	Average temperature c offset voltage	oefficient of input	V.COM.TW	WW	25°C to 70°C	COM.	1.7		μV/°C
100 -	Input offect ourrest (co.	Note ()	N- OFV		25°C	CON	0.1	(-
1000	Input offset current (see	e Note 4)	V _O = 2.5 V,	V _{IC} = 2.5 V	70°C	0	7	300	pА
100		Nata ()			25°C	N	0.6	14	- 4
IB	Input bias current (see	Note 4)	V _O = 2.5 V,	V _{IC} = 2.5 V	70°C	NY.CC	40	600	pА
V.V.10	Common-mode input v	oltage range	W.100Y.COM	TW	25°C	-0.2 to 4	-0.3 to 4.2	LM.	V
VICR	(see Note 5)	N N	WW.100 L.COM		Full range	-0.2 to 3.5	1.CON	M.TY	v
W.	N 1001. COM.	N N	.100 L.	OM.I.	25°C	3.2	3.9	0 _W .,	
Vон	High-level output voltage	ge V	V _{ID} = 100 mV,	$R_L = 100 \text{ k}\Omega$	0°C	3	3.9	Mo	V
			WWW.LOOY.		70°C	3	4		WT
N	WW.IUV CON	1.1	WW.IC.	COM	25°C	NN.	0	50	77
VOL	Low-level output voltag	e	$V_{ID} = -100 \text{ mV},$	$I_{OL} = 0$	0°C	WAR	0	50	mV
1	NW TOOX.CO	WILL	WW 100	Y.Com.T	70°C		0	50	L.M
	WWW.	WT	WWW	N.CO.	25°C	25	170	1.0	ant.
AVD	Large-signal differentia amplification	l voltage	$V_{O} = 0.25 V$ to 2 V,	$R_L = 100 \text{ k}\Omega$	0°C	15	200	N.Va	V/mV
	ampinioation	COM.TV	W.	LON T. COM	70°C	15	140	×1	co^{N}
	NAM TOOX	WI.W	N	1001.	25°C	65	91	100 r	c01
CMRR	Common-mode rejection	on ratio	$V_{IC} = V_{ICR}min$		0°C	60	91	1100	dB
	WW.100	COM.	With	N. W. CO	70°C	60	92	N•2	V.C
	N. 10	. COM.L		W.100 - C	25°C	70	93	1.70.	
ksvr	Supply-voltage rejectio (ΔVDD/ΔVIO)	n ratio	$V_{DD} = 5 V \text{ to } 10 V,$	V _O = 1.4 V	0°C	60	92	N.I	dB
		N.COm.	W WY	NY COOX	70°C	60	94	N N	00%
	WW.	TO COM	No EN		25°C	N	210	560	
IDD	Supply current (two am	plifiers)	$V_O = 2.5 V$, No load	V _{IC} = 2.5 V,	O°C	- 1	250	640	μA
					70°C		170	440	N.100

5. This range also applies to each input individually.



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electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

OM.T	PARAMETER	N.100Y.CO	TEST CON	DITIONS	TA		C27M2 C27M2 C27M2 C27M2	AC BC	UNIT
	I.TV W	NN.1001.	OM.IT	I.W.W.		MIN	TYP	MAX	
	W WILL	TLC27M2C	V _O = 1.4 V,	V _{IC} = 0,	25°C	M.T.Y	1.1	10	
		TECZTWZC	R _S = 50 Ω,	$R_L = 100 \text{ k}\Omega$	Full range	TI	N	12	mV
		TLC27M2AC	V _O = 1.4 V,	VIC = 0,	25°C	Jur	0.9	5	
VIO	Input offset voltage	TEGETWENO	R _S = 50 Ω,	R _L = 100 kΩ	Full range	OV.	-	6.5	
10	input onset voltage	TLC27M2BC	V _O = 1.4 V,	$V_{IC} = 0,$	25°C	Mon	224	2000	
		TEGETHIEBO	R _S = 50 Ω,	R _L = 100 kΩ	Full range		WT.	3000	μV
		TLC27M7C	V _O = 1.4 V,	V _{IC} = 0,	25°C	1.005	190	800	μ.
v.100	CONFIL	W.	R _S = 50 Ω,	R _L = 100 kΩ	Full range	-1 CO	Mr.	1900	
ανιο	Average temperature c offset voltage	oefficient of input	100X.COM.J		25°C to 70°C	N.C	2.1	W	μV/°C
1.1	Input offset current (see	n Noto ()	Vo - 5V COM		25°C		0.1	In	۳Å
10	input onset current (see	e Note 4)	$V_{O} = 5 V,$	$V_{IC} = 5 V$	70°C	100 -	7	300	pА
$\mathcal{N}_{\mathcal{M}}$	Innut high ourrest (and	Note ()	Ma EV		25°C	100%	0.7	V.L.A.	рА
IB	Input bias current (see	Note 4)	V _O = 5 V,	$V_{IC} = 5 V$	70°C	100	50	600	N PA
WW	Common-mode input v	oltage range	WW.100Y.CC	OM.TW	25°C	-0.2 to 9	-0.3 to 9.2	OW.]	v
VICR	(see Note 5)		WWW.1001.		Full range	-0.2 to 8.5	1001.	CO _{N1}	V
V	1001.	M.T.W	W 100	CON.T	25°C	8	8.7	. 00	W.r.
Vон	High-level output voltage	ge	V _{ID} = 100 mV,	$R_L = 100 \text{ k}\Omega$	0°C	7.8	8.7	1.0	V.
			WWW.L		70°C	7.8	8.7	N.C	
	W.100	-0 ^{M.1}	I.WW.I	COM.	25°C	Vice	0	50	Our
Vol	Low-level output voltag	le l.	$V_{ID} = -100 \text{ mV},$	$I_{OL} = 0$	0°C		0	50	mV
			WW		70°C	N	0	50	
	WWW.	V.COm mV	WWW	. on Y.CO.	25°C	25	275	1100	1.00
Avd	Large-signal differentia amplification	I voltage	$V_{O} = 1 V \text{ to } 6 V,$	$R_L = 100 \text{ k}\Omega$	0°C	15	320	N	V/mV
	ampinication				70°C	15	230	N.10	
	WWW	00Y.CO.	W WY	100%.0	25°C	65	94	1	70 x.
CMRR	Common-mode rejection	on ratio	VIC = VICRmin		0°C	60	94	N	dB
					70°C	60	94	MM.	100
	W	1.100 1.	1. T	W.100	25°C	70	93	VINT	100
^k svr	Supply-voltage rejectio $(\Delta V_{DD}/\Delta V_{IO})$	n ratio	$V_{DD} = 5 V \text{ to } 10 V,$	V _O = 1.4 V	0°C	60	92		dB
			WTS		70°C	60	94	MM	10
	-14	WW.100	ONL.	. March	25°C	Wm	285	600	141.2
IDD	Supply current (two am	plifiers)	$V_{O} = 5 V$, No load	V _{IC} = 5 V,	0°C	1.1	345	800	μA
			NO IORU		70°C	VT.IA	220	560	

[†] Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

5. This range also applies to each input individually.



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electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

NT.	PARAMETER	0Y.COM.T	TEST CON	DITIONS	T _A †	TL TL	.C27M2 .C27M2 .C27M2 .C27M2 .C27M7	AI BI	UNIT
M.TV	WIT WIT	100 1. COM	T.A. A.	W.100 1	1 COM.1	MIN	TYP	MAX	
The	W WW	TLC27M2I	V _O = 1.4 V,	$V_{IC} = 0,$	25°C		1.1	10	
		TLC27Wi2I	R _S = 50 Ω,	$R_L = 100 \text{ k}\Omega$	Full range	LW		13	
		TLC27M2AI	V _O = 1.4 V,	$V_{IC} = 0,$	25°C	Wn	0.9	5	mV
Vie	Input offset voltage	TLOZIWIZAI	R _S = 50 Ω,	$R_L = 100 \text{ k}\Omega$	Full range			7	
VIO	input onset voltage	TLC27M2BI	V _O = 1.4 V,	V _{IC} = 0,	25°C	1.1	220	2000	
		TECZTWIZDI	R _S = 50 Ω,	$R_L = 100 \text{ k}\Omega$	Full range	TIM		3500	μV
		TLC27M7I	V _O = 1.4 V,	$V_{IC} = 0,$	25°C	Ju-	185	500	μν
02	ONI.I Y		R _S = 50 Ω,	R _L = 100 kΩ	Full range	OVr.		2000	
αΛΙΟ	Average temperature co offset voltage	pefficient of input	V.COM.TW		25°C to 85°C		1.7		μV/°C
100 -	land affect summer (as	Nata AVV.1	NE OFN		25°C	CON	0.1	I	- 4
1000	Input offset current (see	Note 4)	V _O = 2.5 V,	V _{IC} = 2.5 V	85°C	- c0]	24	1000	pА
1		lata ()			25°C	Y	0.6	14	- 4
IB	Input bias current (see I	Note 4)	V _O = 2.5 V,	V _{IC} = 2.5 V	85°C	NY.CC	200	2000	pА
W.IC	Common-mode input vo	oltage range	N.100X.COM	TW	25°C	-0.2 to 4	-0.3 to 4.2	TW	V
VICR	(see Note 5)		W.100 L.COM		Full range	-0.2 to 3.5	1.CO ^N	M.TY	V V
M.	N1001. M.T	11 11	1001.	ON.T.	25°C	3.2	3.9	OV.	
Vон	High-level output voltag	e	V _{ID} = 100 mV,	$R_L = 100 \text{ k}\Omega$	-40°C	3	3.9	Mo	V
			WWW.LOOY.		85°C	3	4		WT
	WW.100 CON		WW.IO	COM	25°C	MW.	0	50	10
VOL	Low-level output voltage	e1.1	$V_{ID} = -100 \text{ mV},$	$I_{OL} = 0$	-40°C	WIN	0	50	mV
	WWWW.100Y.CO		WW 100		85°C		0	50	N.T
	WWW. SYCC	W	WWW	or.com	25°C	25	170	01.0	M
AVD	Large-signal differential amplification	voltage	$V_{O} = 0.25 V$ to 2 V,	$R_L = 100 \ k\Omega$	-40°C	15	270	N.V.	V/mV
		COM.T.V	L.W.W.	ON T. COM	85°C	15	130	V V - 1	CON
	WW 100Y.	WT.M	N Y	1001.	25°C	65	91	1001	
CMRR	Common-mode rejectio	n ratio	$V_{IC} = V_{ICR}min$		-40°C	60	90	1100	dB
	.100 M.100	COM.	WWW.	N.L. CO	85°C	60	90	1.5	V.C
	Cupply voltage and attend	T.MO Cont		W.IUV TC	25°C	70	93	M.I.	V.C
^k SVR	Supply-voltage rejectior (ΔVDD/ΔVIO)	Tallo	$V_{DD} = 5 V \text{ to } 10 V,$	V _O = 1.4 V	-40°C	60	91	TN.1	dB
		NY.CUT	W W	N TOOY!	85°C	60	94		001.
			V _O = 2.5 V,	V _{IC} = 2.5 V,	25°C	N	210	560	1005
IDD	Supply current (two amp	olifiers)	$V_0 = 2.5 V$, No load	viC − 2.5 v,	-40°C	-1	315	800	μA
			VT.		85°C		160	400	N.100

[†]Full range is –40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

5. This range also applies to each input individually.



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electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

ON.T	PARAMETER	V.100Y.COM	TEST CON	DITIONS			LC27M2 LC27M2 LC27M2 LC27M7	AI BI	UNIT
AM	TN NT.	TN.1001.	M.T.Y	N.W.10	CON	MIN	TYP	MAX	
.00	W WIN		V _O = 1.4 V,	V _{IC} = 0,	25°C	V.L.	1.1	10	
		TLC27M2I	$R_S = 50 \Omega$,	$R_L = 100 k\Omega$	Full range	T	N	13	
		TI 00714201	V _O = 1.4 V,	$V_{IC} = 0,$	25°C	DAT U	0.9	5	mV
01.0	MAT	TLC27M2AI	$R_{S} = 50 \Omega,$	$R_L = 100 k\Omega$	Full range	OM.	-1	7	
VIO	Input offset voltage	TI COZMODI	V _O = 1.4 V,	$V_{IC} = 0,$	25°C	Mon	224	2000	
		TLC27M2BI	R _S = 50 Ω,	$R_L = 100 k\Omega$	Full range		WT.	3500	
		TLCOTMT	V _O = 1.4 V,	V _{IC} = 0,	25°C		190	800	μV
a 100 x	CONLIN'	TLC27M7I	$R_{S} = 50 \Omega,$	$R_L = 100 k\Omega$	Full range	<1 CO	Mr	2900	1
αVIO	Average temperature co offset voltage	efficient of input	100Y.COM.T		25°C to 85°C	N.C	2.1	W	μV/°C
.W.10	lagut affact ourroot (pag	Note 4)	N- EVCON	NO EV	25°C	~1	0.1	In	~^
10	Input offset current (see	Note 4)	V _O = 5 V,	$V_{IC} = 5 V$	85°C	100 -	26	1000	рА
W.	MT. CONTRACTW	NW	1001.00	WE	25°C	1001	0.7	V.L.A.	
IB	Input bias current (see N	Note 4)	V _O = 5 V,	$V_{IC} = 5 V$	85°C	N.100	220	200 0	рА
	Common-mode input voltage range		WW.100X.C	WI.MO	25°C	-0.2 to 9	-0.3 to 9.2	O _M .	V
VICR	(see Note 5)	WT.	WWW.100Y.		Full range	-0.2 to 8.5	100X.	1.CO ^N	V
	NWW. CO	W	WWW. OO	Y.CO.T	25°C	8	8.7	1.00	TIM
Vон	High-level output voltage	e	V _{ID} = 100 mV,	$R_L = 100 \text{ k}\Omega$		7.8	8.7	N.C	v
			W.10	COM.	85°C	7.8	8.7	, s	·0 _W .,
	MM 100X.C	MIM	With and I	Mox.	25°C	NV .	0	50	COM
Vol	Low-level output voltage	WT NO	$V_{ID} = -100 \text{ mV},$	$I_{OL} = 0$	-40°C	N	0	50	mV
	WW.100	CONT	WWW.	NOJ.V.	85°C		0	50	I.CON
	100	COMIT	W Mart	1.100 -1 CO	25°C	25	275	1.100	V.CO
AVD	Large-signal differential amplification	voltage	$V_{O} = 1 V \text{ to } 6 V,$	$R_L = 100 \text{ k}\Omega$	-40°C	15	390	W.10	V/mV
	ampinioution	N.CUT	MW W	100Y.C	85°C	15	220	1	DOX.C
	WWW.P	N.COM.	VIA NO	W.L.	25°C	65	94	NA.	. NOY.C
CMRR	Common-mode rejection	n ratio	$V_{IC} = V_{ICR}min$		-40°C	60	93	WW.	dB
	WW	100Y.C-	In N	100x	85°C	60	94	-	100 1
	Cumple under state st	100Y.CO	V WT	100	25°C	70	93		x100
K SVR	Supply-voltage rejection $(\Delta V_{DD}/\Delta V_{IO})$	ratio	$V_{DD} = 5 V \text{ to } 10 V,$	V _O = 1.4 V	-40°C	60	91	NN	dB
	· · · · · · · · · · · · · · · · · · ·	W.100	N.I.	.WW.10	85°C	60	94	- NIN	W.10
		100x.		Vio – E.V.	25°C	1.1	285	600	V.W.Y
IDD	Supply current		$V_{O} = 5 V$, No load	V _{IC} = 5 V,	-40°C	TIM	450	900	μA
			CONT.		85°C	- 15	205	520	MAN

[†]Full range is –40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

5. This range also applies to each input individually.



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	PARAMETER	V.COM.T	TEST CON	DITIONS	TAT		_C27M2I _C27M7I		UNIT
				W.1001.	OMEN	MIN	TYP	MAX	_
VT1	A WWW	TLOOZMONA	V _O = 1.4 V,	$V_{IC} = 0,$	25°C		1.1	10	
N	N	TLC27M2M	R _S = 50 Ω,	$R_L = 100 \text{ k}\Omega$	Full range	N		12	
VIO	Input offset voltage		$V_{O} = 1.4 V_{,}$	$V_{IC} = 0,$	25°C	W	185	500	mV
		TLC27M7M	R _S = 50 Ω,	$R_L = 100 k\Omega$	Full range			3750	
ανιο	Average temperature co offset voltage	efficient of input	ONT.TW	WWW.10	25°C to 125°C	WT.	1.7		μV/°C
	Input offect ourrent (cos	Note ()	Va DEV	Via DEV	25°C	1.	0.1		pА
10	Input offset current (see	Note 4)	V _O = 2.5 V,	V _{IC} = 2.5 V	125°C	W.	1.4	15	nA
N.CC	Innut high ourrant (and h	loto ()	No DEV		25°C	T.M.	0.6		pА
IB	Input bias current (see N	NOIE 4)	V _O = 2.5 V,	V _{IC} = 2.5 V	125°C	U. C	9	35	nA
1007.	Common-mode input vo	Itage range	OX.COM.TW	WW	25°C	0 to 4	-0.3 to 4.2	[V
VICR	(see Note 5)	WWW.J	100Y.COM.TV		Full range	0 to 3.5	M.T	N	V
	OT. O. T.W	W	1001. OM.		25°C	3.2	3.9		
Vон	High-level output voltage	e WW	V _{ID} = 100 mV,	$R_L = 100 \text{ k}\Omega$	-55°C	3	3.9	IN	V
			N.10 N.COM		125°C	3	4	NT.	
War	.100 . COM. 1		W.100 CON	1.	25°C	. Y.	0	50	Ń
VOL	Low-level output voltage		$V_{ID} = -100 \text{ mV},$	$I_{OL} = 0$	−55°C	1.100	0	50	mV
WWY	MANNA T	N N	1001.00	WILL	125°C	x1 10	0	50	7
WW	N. L. COMP.	V IV	WW. OOY.C	WT	25°C	25	170		L.M.
AVD	Large-signal differential amplification	voltage	$V_{O} = 0.25 V \text{ to } 2 V,$	$R_L = 100 \text{ k}\Omega$	−55°C	15	290	20 M*	V/mV
	1001. ON	TW	W 100 1.	COM.IT	125°C	15	120	CON	
			WW 100Y		25°C	65	91		1.1
CMRR	Common-mode rejection	n ratio	$V_{IC} = V_{ICR}min$		−55°C	60	89	1.00	dB
	CO NUN. 100	M.	WWW.100	V CONT.	125°C	60	91	V.C) N A
	Committee and the second section	oM.1	WW.10		25°C	70	93	-1 (OM.
^K SVR	Supply-voltage rejection $(\Delta V_{DD}/\Delta V_{IO})$	Tallo	$V_{DD} = 5 V \text{ to } 10 V,$	V _O = 1.4 V	-55°C	60	91	007.	dB
		WILLIAM	WW	100Y.CO.	125°C	60	94	1001	
			V _O = 2.5 V,	V _{IC} = 2.5 V,	25°C	-	210	560	1.00
IDD	Supply current (two amp	olifiers)	No load	10 - 2.0 V,	-55°C		340	880	μA
	WW 100	Y.U. TY	N.		125°C		140	360	

electrical characteristics at specified free-air temperature. V = 5 V (unless otherwise noted)

5. This range also applies to each input individually.



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electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER		TEST CONI	DITIONS	TAT	TL	UNIT				
			1.1	W.100	COM	MIN	TYP	MAX	onn	
	UM WH.	400	V _O = 1.4 V,	$V_{IC} = 0,$	25°C	T.M.	1.1	10		
CON	WW.	TLC27M2M	R _S = 50 Ω,	$R_L = 100 k\Omega$	Full range	WTN		12		
10	Input offset voltage	TI 00714714	V _O = 1.4 V,	VIC = 0,	25°C	17	190	800	mV	
		TLC27M7M	R _S = 50 Ω,	$R_L = 100 \text{ k}\Omega$	Full range	N_{1}	-	4300		
	Average temperature coeff	cient of input		W. T.	25°C to	M.	2.1		μV/°C	
VIO	offset voltage	WW.	NT NUS	WW	125°C	Ur A	2.1		μν/Ο	
10	Input offset current (see No	ote 4)	V _O = 5 V,	VIC = 5 V	25°C	COM	0.1		pА	
		N.10			125°C	CON	1.8	15	P/ 1	
IB 00	Input bias current (see Not	e 4)	V _O = 5 V,	VIC = 5 V	25°C		0.7		pА	
UQ .	N.CO. TV				125°C	N.C	10	35	P	
	CON.1		ON CONL		0500	0	-0.3	W	V	
	Common mode input volta		100 CON.		25°C	to 9	to 9.2	I	V	
VICR	Common-mode input voltage range (see Note 5)		N.1001. OM			0	<u></u>			
			1004.001		Full range	to		ΛTN	V	
VIN	The CONT	Vite	W.L. CON	Win	WWW	8.5	1.CO		Ń	
	N.100 COM.1		WW.100 CO	M.	25°C	8	8.7	Nr.	N	
√он	High-level output voltage		V _{ID} = 100 mV,	RL = 100 kΩ	−55°C	7.8	8.6	ON.	V	
WW	W. A ONY.COM T	V V	A LOOX.C	WTN	125°C	7.8	8.8	In		
			WWW.LOOV.		25°C	11	0	50	WT	
/OL	Low-level output voltage		$V_{ID} = -100 \text{ mV},$	IOT = 0	−55°C	WW.	0	50	mV	
V	1100Y.COM	TN	W " 1001	M.T.V	125°C	ALC: N	0	50	M.1.	
		WEA	WW 100		25°C	25	275	N.0-	M.T	
AVD	Large-signal differential vol amplification	tage	$V_{O} = 1 V \text{ to } 6 V,$	$R_L = 100 \text{ k}\Omega$	55°C	15	420	N.C	V/mV	
	ampinioadon	M.I.	WW.10	CONT.	125°C	15	190	~1(ON.	
			W T		25°C	65	94	00 *	co^{M}	
CMRR	Common-mode rejection ra	itio	$V_{IC} = V_{ICR}min$		−55°C	60	93	1001	dB	
	WWW.Io.	N/m	WWW.	LON.COM	125°C	60	93		1.001	
	0	.co ^{M.1}	WW		25°C	70	93	1.10	V.CC	
ksvr	Supply-voltage rejection ra (ΔVDD/ΔVIO)	tio	$V_{DD} = 5 V \text{ to } 10 V,$	V _O = 1.4 V	-55°C	60	91	W.10	dB	
		Y.COM	WW WW	1001.0	125°C	60	94	1	10X.C	
	WWW.IC	V.COM.		V. S.	25°C		285	600	NON!	
DD	Supply current (two amplifi	ers)	$V_{O} = 5 V,$ No load	V _{IC} = 5 V,	-55°C	N	490	1000	μA	
					125°C		180	480	1.100	



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	PARAMETER	TEST C	ONDITIONS	TA	TLC27M2C TLC27M2AC TLC27M2BC TLC27M7C	UNIT
M.T.Y	W.100	V.1	.100 -	COM.	MIN TYP MAX	
		M.I.M.	N 1001	25°C	0.43	
		WTD	$V_{I(PP)} = 1 V$	0°C	0.46	
SR :	Clow rote at unity rain	$R_L = 100 k\Omega$	WWW.L	70°C	0.36	
SK .	Slew rate at unity gain	C _L = 20 pF, See Figure 1	N.W.IV	25°C	0.40	V/μs
			V _{I(PP)} = 2.5 V	0°C	0.43	1
		I.COM TW	WW	70°C	0.34	1
vn C9	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R _S = 20 Ω,	25°C	32	nV/√H
N.C	WWW WT	NT N. V.	W.	25°C	55	
BOM I	Maximum output-swing bandwidth	$V_{O} = V_{OH},$ $R_{L} = 100 \text{ k}\Omega,$	C _L = 20 pF, See Figure 1	0°C	60	kHz
		KL = 100 KS2,	See Figure 1	70°C	50	1
11007	WIM WI	100	11 - N1 -	25°C	525	
B ₁	Unity-gain bandwidth	$V_{I} = 10 \text{ mV},$ See Figure 3	C _L = 20 pF,	0°C	600	kHz
		See Figure 5		70°C	400	1
W.10	COM.1	W. The COM		25°C	40°	
¢m l	Phase margin	V _I = 10 mV, C _L = 20 pF,	f = B ₁ , See Figure 3	0°C	41°	1
		0L = 20 pr,	oce rigule 5	70°C	39°	1

operating characteristics at specified free-air temperature, V_{DD} = 5 V

operating characteristics at specified free-air temperature, V_{DD} = 10 V

	PARAMETER	TEST C	TEST CONDITIONS		TLO TLO TLO TLO	UNIT		
	NWW. LONY.COMP. TW	WWW.	Y.COMMENTW	V	MIN	TYP MAX	VTA	
	COM.	WWW.10	CONT.	25°C	WWW	0.62		
		W.10	$V_{I(PP)} = 1 V$	O°C	- TANK	0.67	0_{M^*}	
२	Slew rate at unity gain	R _L = 100 kΩ, C _L = 20 pF,	T.M.	70°C	N	0.51	V/μs	
`	WWW.100Y.COM.TW WWW.100Y.COM.TW	See Figure 1	INV.CO.	25°C	NN	0.56		
		WWW	VI(PP) = 5.5 V	0°C	W	0.61		
			100 L. COM	70°C		0.46		
		f = 1 kHz, See Figure 2	R _S = 20 Ω,	25°C	N N	32	nV/√Hz	
	W.100 . COM. 1		W.IO CC	25°C		35	J.V	
DM	Maximum output-swing bandwidth	$V_{O} = V_{OH},$ $R_{I} = 100 \text{ k}\Omega,$	C _L = 20 pF, See Figure 1	0°C		40	kHz	
			occ rigure r	70°C	30		1001.	
	WWW.L. OX.COM	A Start	NWW.	25°C	N	635	Yoor	
1	Unity-gain bandwidth	V _I = 10 mV, See Figure 3	C _L = 20 pF,	O°C		710	kHz	
	WW 1007.0	occ rigure o	W 1,100 1	70°C		510	N.100	
	WWW. ODY.CO		WW 100	25°C	IN	43°	-xi 10	
۱	Phase margin	$V_{I} = 10 \text{ mV},$ $C_{L} = 20 \text{ pF},$	f = B ₁ , See Figure 3	O°C	WT.	44°		
		0L-20 pi,	eee rigare e	70°C	1.	42°	$_{\rm V}{\rm W}{}^{\rm Y}$	

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operating characteristics at specified free-air temperature, V_{DD} = 5 V

ON.	PARAMETER	TEST C	ONDITIONS	ТА	TLC27M2I TLC27M2AI TLC27M2BI TLC27M7I	UNIT
	N.1. 1001. CC	N.I.	WW.10	1001	MIN TYP MA	X
		MT.Mo	W T	25°C	0.43	
V.C		WT	VI(PP) = 1 V	-40°C	0.51	
CD C	Clour rate at unity gain	$R_L = 100 k\Omega$	WWW.	85°C	0.35)/////
SR	Slew rate at unity gain	C _L = 20 pF, See Figure 1	VI(PP) = 2.5 V	25°C	0.40	V/μs
				-40°C	0.48	
		V.COM TW		85°C	0.32	
Vn	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R _S = 20 Ω,	25°C	32	nV/√Hz
Вом	Maximum output-swing bandwidth	V _O = V _{OH} , R _I = 100 kΩ,	W W	25°C	55	
			C _L = 20 pF, See Figure 1	-40°C	75	kHz
		$R_{L} = 100 R_{Z},$	See Figure 1	85°C	45	N
B ₁	Unity-gain bandwidth	AL 100	1.I.V.	25°C	525	
		$V_{I} = 10 \text{ mV},$	C _L = 20 pF,	-40°C	770	MHz
		See Figure 3		85°C	370	NT
[¢] m	Phase margin	N.100 - C	ONL	25°C	40°	- N
		$V_{I} = 10 \text{ mV},$ $C_{L} = 20 \text{ pF},$	f = B ₁ , See Figure 3	-40°C	43°	
		0L = 20 pr,	occ rigule 5	85°C	38°	NTN.

operating characteristics at specified free-air temperature, V_{DD} = 10 V

	PARAMETER	TEST C	ONDITIONS	ТА	TL TL	.C27M2 .C27M2 .C27M2 .C27M2 .C27M7	Al Bl	UNIT	
	WWW.LCOMM	WWW	LOOY.COM	W	MIN	TYP	MAX		
		NWW	COMP.	25°C	-	0.62	Van	COM	
		VIII	VI(PP) = 1 V	-40°C		0.77	100		
SR	Slew rate at unity gain	R _L = 100 kΩ, C _L = 20 pF,	a 100Y.	85°C		0.47	N.100	V/µs	
	Ciew rate at unity gain	See Figure 1	1004.00	25°C		0.56	110	Viµs	
		V IV	VI(PP) = 5.5 V	-40°C		0.70	M.	N.C	
	W. 1001. COM. I		W.100 1	85°C		0.44	NW.		
'n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R _S = 20 Ω,	25°C	N	32	WW	nV/√Hz	
	N. 100 COM		WW.Ioo	25°C		35	VWI	1.10	
вом	Maximum output-swing bandwidth	$V_{O} = V_{OH},$ $R_{L} = 100 \text{ k}\Omega,$	C _L = 20 pF, See Figure 1	-40°C		45		kHz	
		KL = 100 K32,	See l'igure i	85°C	TW	25	M.	10	
	WWW.IC	N/m	WWW.	25°C	Wr.	635	W		
³ 1	Unity-gain bandwidth	V _I = 10 mV, See Figure 3	C _L = 20 pF,	-40°C	1	880	-	MHz	
		See Figure 5		85°C	M.L	480	1.1	I.	
	WWW COY.	WT	A.M.	25°C	The	43°			
m	Phase margin	$V_{I} = 10 \text{ mV},$ $C_{L} = 20 \text{ pF},$	f = B ₁ , See Figure 3	-40°C	U.S.	46°		NNN N	
		CL=20 pr,	eee rigure e	85°C	-ON-	41°		- N	

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TW	PARAMETER	TEST CO	ONDITIONS	TA	TLC27M2M TLC27M7M	UNIT
T.L	WILLIODY.COM.TW		NN.1001.	0 ^{M.1}	MIN TYP MA	X
11	WWW. 100Y. CONTR	4	1007.0	25°C	0.43	
DNT.		17 17	VI(PP) = 1 V	–55°C	0.54	
SR	Slew rate at unity gain	R _L = 100 kΩ, C _L = 20 pF,	WWW.IC	125°C	0.29	V/μs
JK	Siew rate at unity gain	See Figure 1	WW.100	25°C	0.40	v/μs
COr		1	V _{I(PP)} = 2.5 V	−55°C	0.49	
100	WWW. COM	WT	WWW	125°C	0.28	
v _n C	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R _S = 20 Ω,	25°C	32	nV/√H
N.C	WWWWWWWWWWW	WTD	MM.	25°C	55	
Вом	Maximum output-swing bandwidth	$V_{O} = V_{OH},$ R _L = 100 k Ω ,	C _L = 20 pF, See Figure 1	−55°C	80	kHz
001	COM.1		occ rigare r	125°C	40	
100	NITH WI 100X.	AN THE		25°C	525	
B1 00	Unity-gain bandwidth	V _I = 10 mV, See Figure 3	C _L = 20 pF,	−55°C	850	kHz
		occ riguie o	N N	125°C	330	
W.1	ONT. COM. I.	14 40		25°C	40°	
[¢] m	Phase margin	$V_{I} = 10 \text{ mV},$ $C_{L} = 20 \text{ pF},$	f = B ₁ , See Figure 3	−55°C	44°	1
N.M.		JL Copri,		125°C	36°	

operating characteristics at specified free-air temperature, V_{DD} = 5 V

operating characteristics at specified free-air temperature, $V_{DD} = 10 V$

	PARAMETER	TEST CO	ONDITIONS	TA		.C27M2 .C27M7		UNIT
	NW.10° COM. WW	VI.L.	W	WW	MIN	TYP	MAX	W
		NW.100 V	ONL.	25°C	NN.L	0.62	COM	W
		R _L = 100 kΩ,	VI(PP) = 1 V	−55°C	. WIT	0.81	.co1	
SR (Slew rate at unity gain	$R_{L} = 100 \text{ ksz},$ $C_{L} = 20 \text{ pF},$	TW	125°C		0.38		V/µs
	WWW. SOLCON	See Figure 1	VT NOS	25°C	NW	0.56	Y.CO	TIM
	WWW.100Y.COM.IW	WWW.100	V _{I(PP)} = 5.5 V	−55°C	WW	0.73	V.C	OM.I
				125°C		0.35		
/ _n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R _S = 20 Ω,	25°C		32	001.	nV/√Hz
	W	N.	100	25°C		35	700.	
OM	Maximum output-swing bandwidth	$V_{O} = V_{OH},$ R _I = 100 k Ω ,	$C_L = 20 \text{ pF},$	−55°C	N	50	N.100	kHz
	WWW.LCOW.TW	TKL = 100 K32,	Occ r igure r	125°C	-	20	-110	N.CO
	WW.Ino COM.	Witten a	W. P	25°C		635	M.	V.C
B ₁	Unity gain bandwidth	V _I = 10 mV, See Figure 3	C _L = 20 pF,	-55°C		960	NW.	kHz
				125°C		440		
[¢] m	Phase margin	V _I = 10 mV, C _L = 20 pF,	f = B ₁ , See Figure 3	25°C	N	43°		.100%
				–55°C	-N	47°	NWV	
		0L = 20 pr ,	Occ riguie 5	125°C		39°		N.100

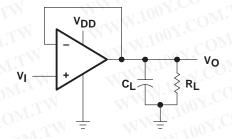


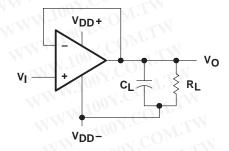
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PARAMETER MEASUREMENT INFORMATION

single-supply versus split-supply test circuits

Because the TLC27M2 and TLC27M7 are optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The use of either circuit gives the same result.

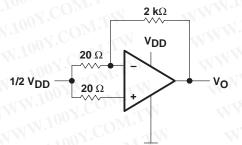


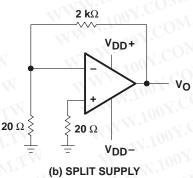


(b) SPLIT SUPPLY

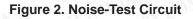
(a) SINGLE SUPPLY

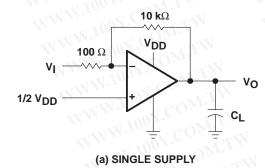


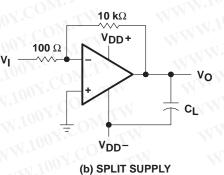
















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PARAMETER MEASUREMENT INFORMATION

input bias current

Because of the high input impedance of the TLC27M2 and TLC27M7 operational amplifiers, attempts to measure the input bias current can result in erroneous readings. The bias current at normal room ambient temperature is typically less than 1 pA, a value that is easily exceeded by leakages on the test socket. Two suggestions are offered to avoid erroneous measurements:

- 1. Isolate the device from other potential leakage sources. Use a grounded shield around and between the device inputs (see Figure 4). Leakages that would otherwise flow to the inputs are shunted away.
- 2. Compensate for the leakage of the test socket by actually performing an input bias current test (using a picoammeter) with no device in the test socket. The actual input bias current can then be calculated by subtracting the open-socket leakage readings from the readings obtained with a device in the test socket.

One word of caution—many automatic testers as well as some bench-top operational amplifier testers use the servo-loop technique with a resistor in series with the device input to measure the input bias current (the voltage drop across the series resistor is measured and the bias current is calculated). This method requires that a device be inserted into the test socket to obtain a correct reading; therefore, an open-socket reading is not feasible using this method.

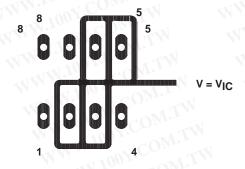


Figure 4. Isolation Metal Around Device Inputs (JG and P packages)

low-level output voltage

To obtain low-supply-voltage operation, some compromise was necessary in the input stage. This compromise results in the device low-level output being dependent on both the common-mode input voltage level as well as the differential input voltage level. When attempting to correlate low-level output readings with those quoted in the electrical specifications, these two conditions should be observed. If conditions other than these are to be used, please refer to Figures 14 through 19 in the Typical Characteristics of this data sheet.



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PARAMETER MEASUREMENT INFORMATION

input offset voltage temperature coefficient

Erroneous readings often result from attempts to measure temperature coefficient of input offset voltage. This parameter is actually a calculation using input offset voltage measurements obtained at two different temperatures. When one (or both) of the temperatures is below freezing, moisture can collect on both the device and the test socket. This moisture results in leakage and contact resistance, which can cause erroneous input offset voltage readings. The isolation techniques previously mentioned have no effect on the leakage, since the moisture also covers the isolation metal itself, thereby rendering it useless. It is suggested that these measurements be performed at temperatures above freezing to minimize error.

full-power response

Full-power response, the frequency above which the operational amplifier slew rate limits the output voltage swing, is often specified two ways: full-linear response and full-peak response. The full-linear response is generally measured by monitoring the distortion level of the output while increasing the frequency of a sinusoidal input signal until the maximum frequency is found above which the output contains significant distortion. The full-peak response is defined as the maximum output frequency, without regard to distortion, above which full peak-to-peak output swing cannot be maintained.

Because there is no industry-wide accepted value for significant distortion, the full-peak response is specified in this data sheet and is measured using the circuit of Figure 1. The initial setup involves the use of a sinusoidal input to determine the maximum peak-to-peak output of the device (the amplitude of the sinusoidal wave is increased until clipping occurs). The sinusoidal wave is then replaced with a square wave of the same amplitude. The frequency is then increased until the maximum peak-to-peak output can no longer be maintained (Figure 5). A square wave is used to allow a more accurate determination of the point at which the maximum peak-to-peak output is reached.





(a) f = 1 kHz

(b) B_{OM} > f > 1 kHz

(c) f = B_{OM}

(d) f > BOM

Figure 5. Full-Power-Response Output Signal

test time

Inadequate test time is a frequent problem, especially when testing CMOS devices in a high-volume, short-test-time environment. Internal capacitances are inherently higher in CMOS than in bipolar and BiFET devices and require longer test times than their bipolar and BiFET counterparts. The problem becomes more pronounced with reduced supply levels and lower temperatures.



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TYPICAL CHARACTERISTICS

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			FIGUR
Vio	Input offset voltage	Distribution	6, 7
αVIO	Temperature coefficient	Distribution	8, 9
VOH	High-level output voltage	vs High-level output current vs Supply voltage vs Free-air temperature	10, 11 12 13
VOL	Low-level output voltage	vs Common-mode input voltage vs Differential input voltage vs Free-air temperature vs Low-level output current	14, 15 16 17 18, 19
AVD	Differential voltage amplification	vs Supply voltage vs Free-air temperature vs Frequency	20 21 32, 33
IIB/IIO	Input bias and input offset current	vs Free-air temperature	22
VIC	Common-mode input voltage	vs Supply voltage	23
IDD	Supply current	vs Supply voltage vs Free-air temperature	24 25
SR	Slew rate	vs Supply voltage vs Free-air temperature	26 27
- CON	Normalized slew rate	vs Free-air temperature	28
VO(PP)	Maximum peak-to-peak output voltage	vs Frequency	29
B ₁	Unity-gain bandwidth	vs Free-air temperature vs Supply voltage	30 31
[¢] m	Phase margin	vs Supply voltage vs Free-air temperature vs Capacitive loads	34 35 36
Vn	Equivalent input noise voltage	vs Frequency	37
	Phase shift	vs Frequency	32, 33

Table of Graphs

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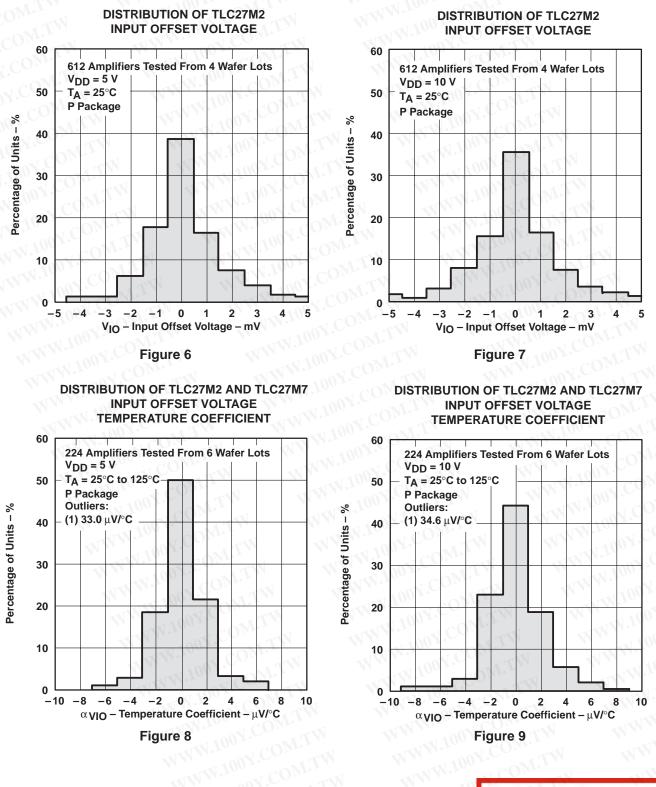


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TYPICAL CHARACTERISTICS

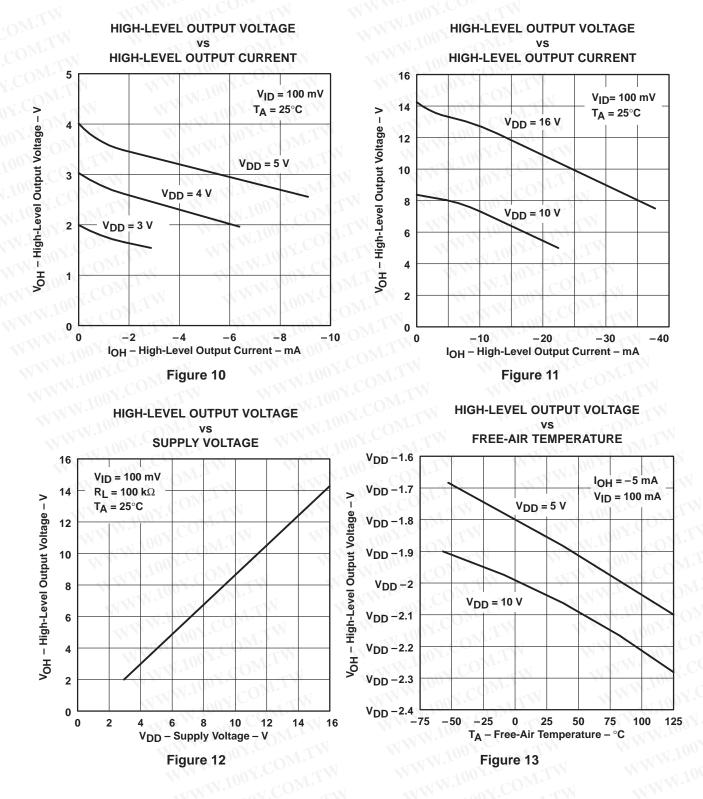


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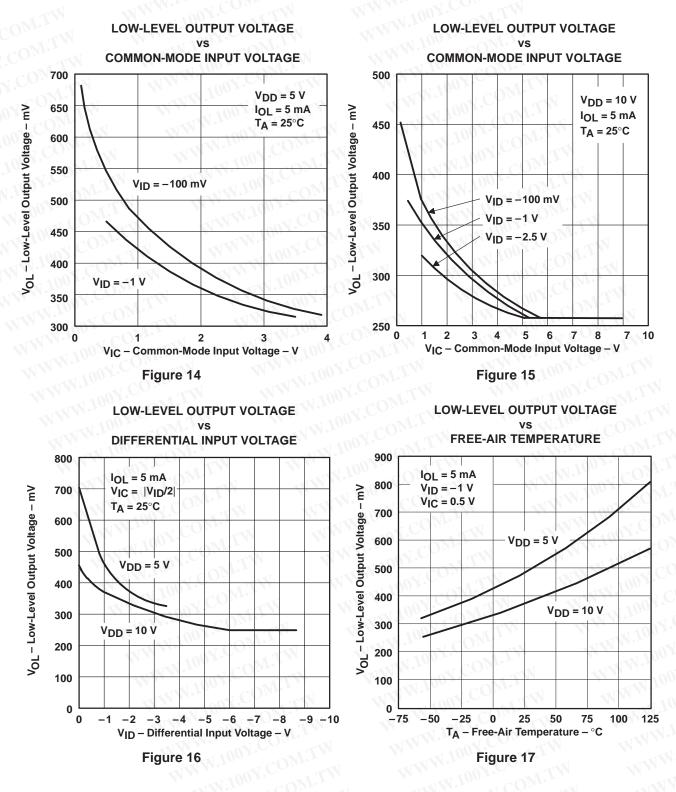
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TYPICAL CHARACTERISTICS[†]





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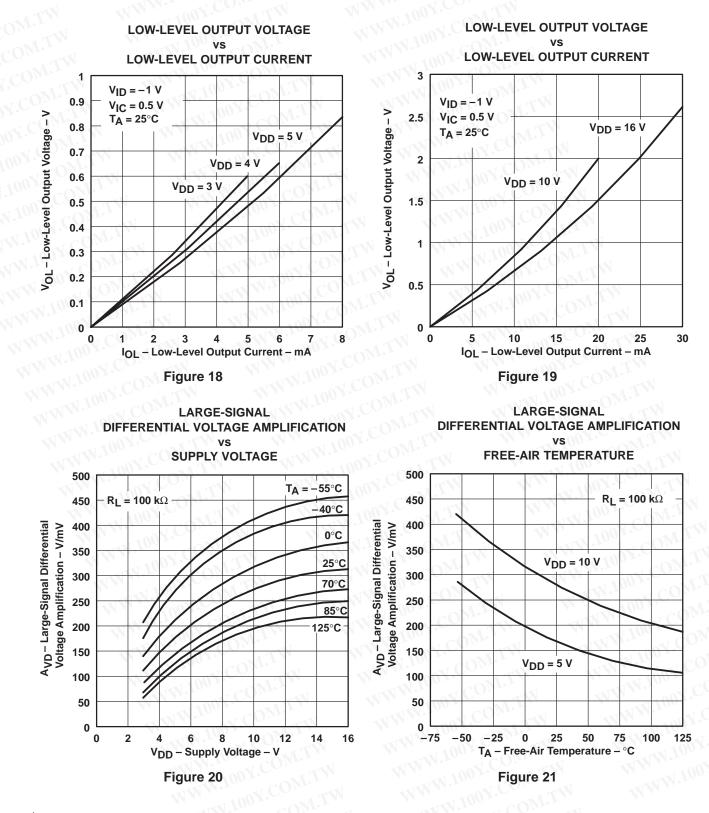
TYPICAL CHARACTERISTICS[†]

[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.



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TYPICAL CHARACTERISTICS[†]

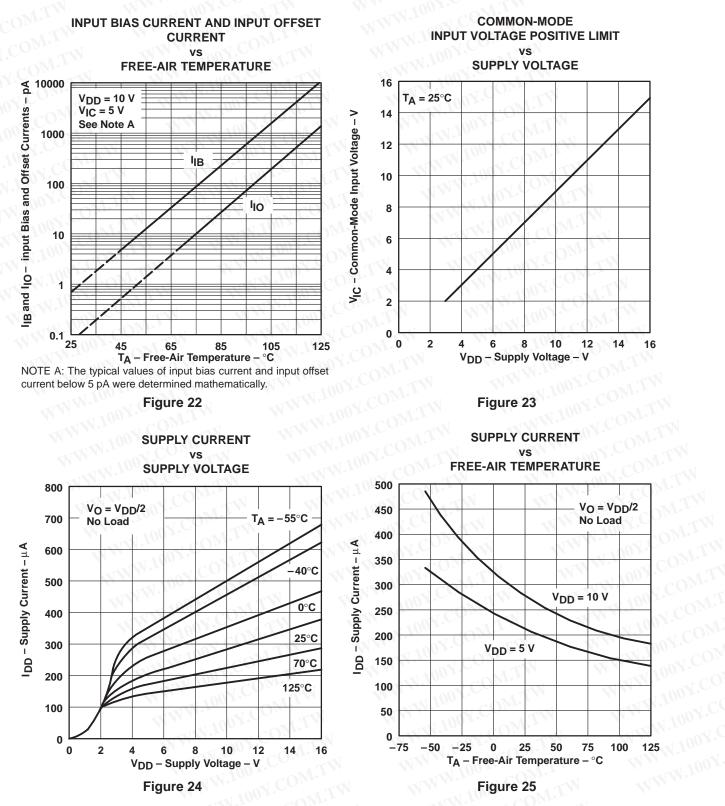




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TYPICAL CHARACTERISTICS[†]



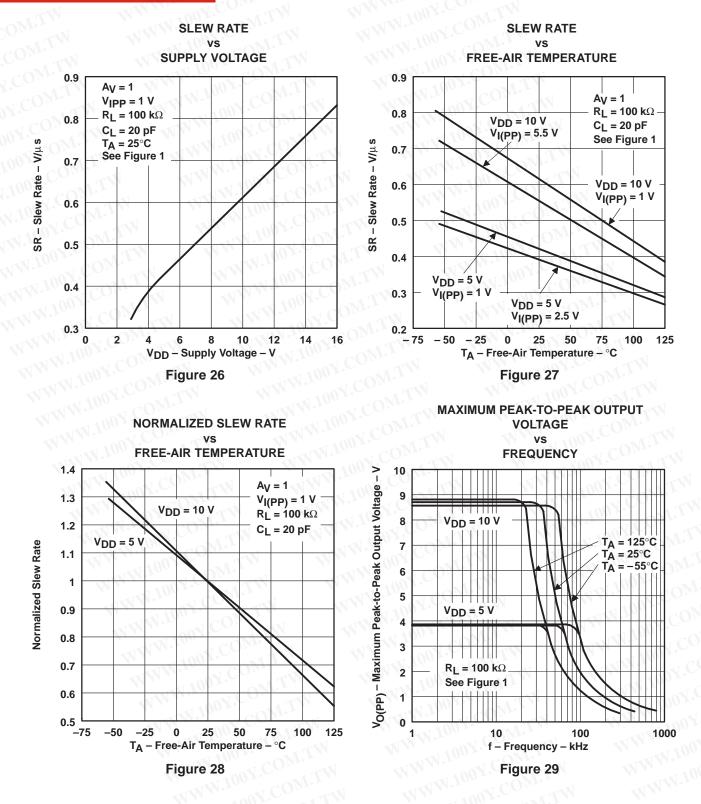


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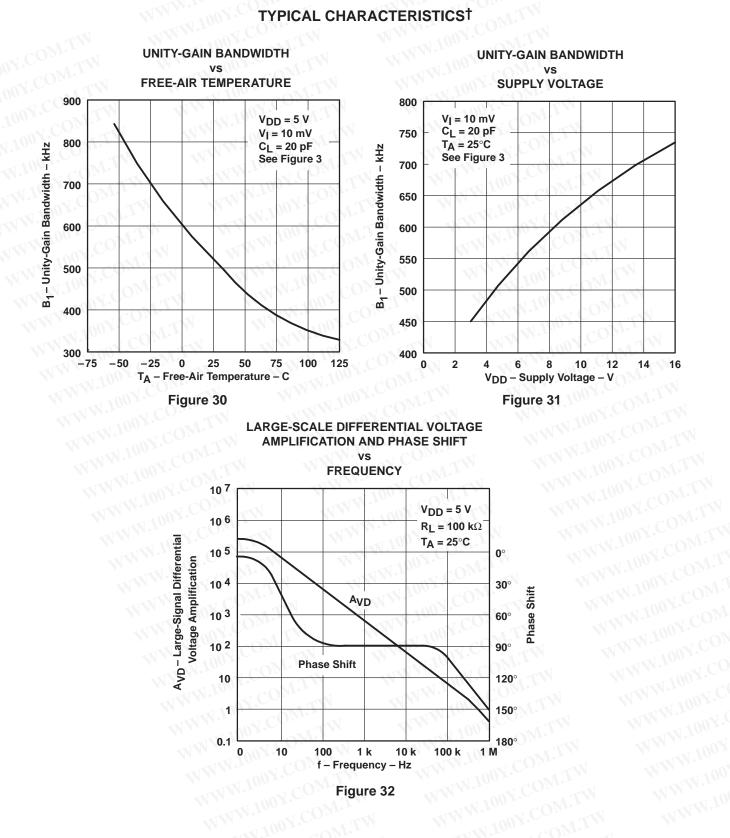
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TYPICAL CHARACTERISTICS[†]





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[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

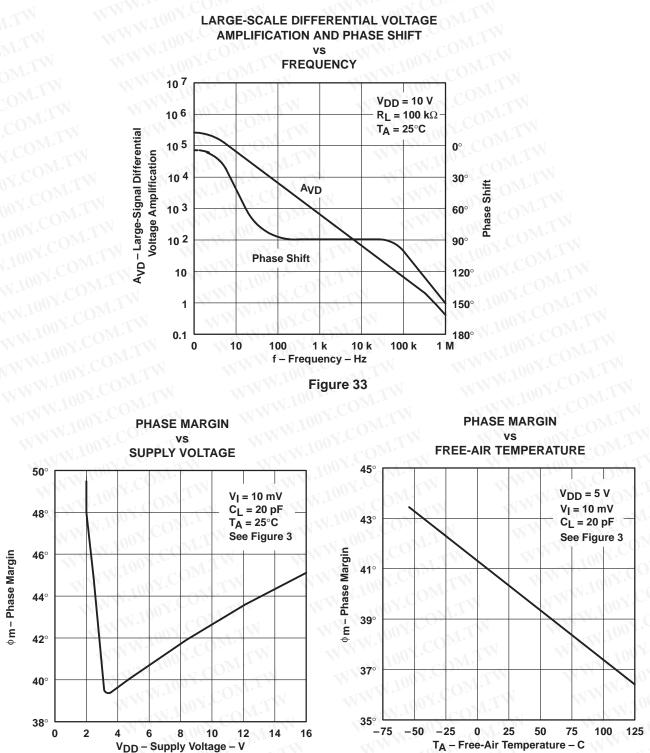


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TYPICAL CHARACTERISTICS[†]



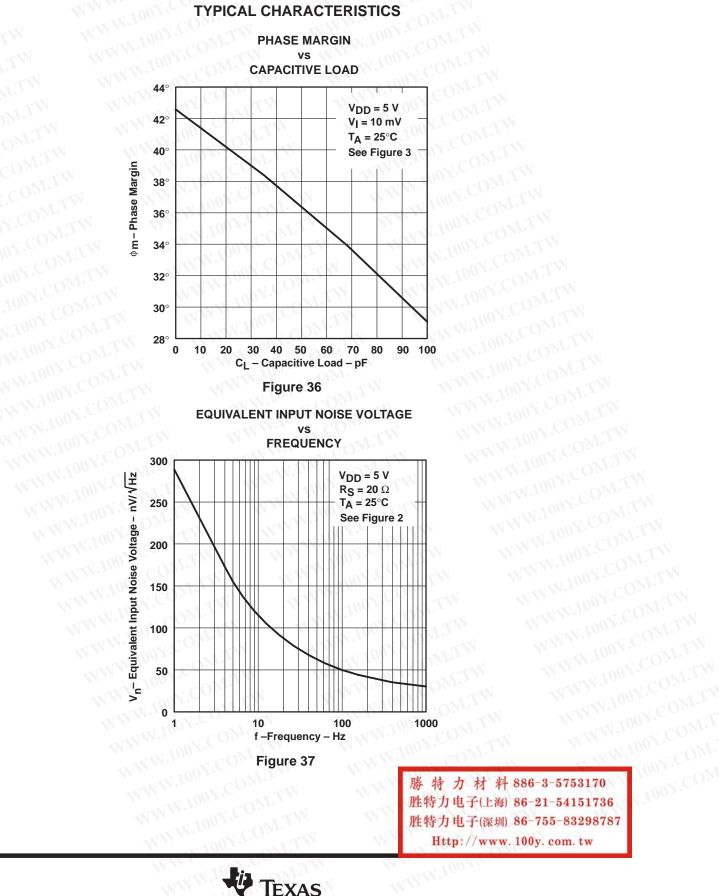
[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

Figure 34



Figure 35

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APPLICATION INFORMATION

single-supply operation

While the TLC27M2 and TLC27M7 perform well using dual power supplies (also called balanced or split supplies), the design is optimized for single-supply operation. This design includes an input common-mode voltage range that encompasses ground as well as an output voltage range that pulls down to ground. The supply voltage range extends down to 3 V (C-suffix types), thus allowing operation with supply levels commonly available for TTL and HCMOS; however, for maximum dynamic range, 16-V single-supply operation is recommended.

Many single-supply applications require that a voltage be applied to one input to establish a reference level that is above ground. A resistive voltage divider is usually sufficient to establish this reference level (see Figure 38). The low input bias current of the TLC27M2 and TLC27M7 permits the use of very large resistive values to implement the voltage divider, thus minimizing power consumption.

The TLC27M2 and TLC27M7 work well in conjunction with digital logic; however, when powering both linear devices and digital logic from the same power supply, the following precautions are recommended:

- Power the linear devices from separate bypassed supply lines (see Figure 39); otherwise, the linear device supply rails can fluctuate due to voltage drops caused by high switching currents in the digital logic.
- 2. Use proper bypass techniques to reduce the probability of noise-induced errors. Single capacitive decoupling is often adequate; however, high-frequency applications may require RC decoupling.

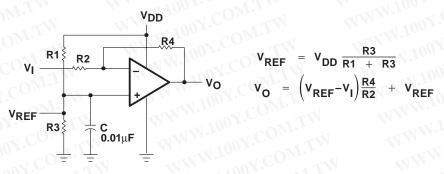
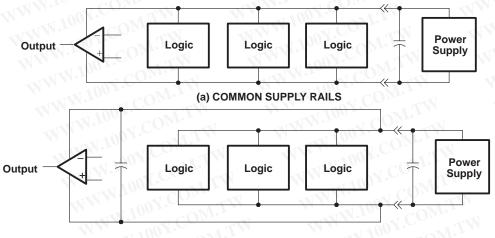


Figure 38. Inverting Amplifier With Voltage Reference



(b) SEPARATE BYPASSED SUPPLY RAILS (preferred)

Figure 39. Common Versus Separate Supply Rails



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APPLICATION INFORMATION

input characteristics

The TLC27M2 and TLC27M7 are specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction. Exceeding this specified range is a common problem, especially in single-supply operation. Note that the lower range limit includes the negative rail, while the upper range limit is specified at $V_{DD} - 1$ V at $T_A = 25^{\circ}$ C and at $V_{DD} - 1.5$ V at all other temperatures.

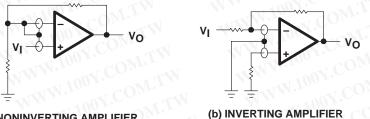
The use of the polysilicon-gate process and the careful input circuit design gives the TLC27M2 and TLC27M7 very good input offset voltage drift characteristics relative to conventional metal-gate processes. Offset voltage drift in CMOS devices is highly influenced by threshold voltage shifts caused by polarization of the phosphorus dopant implanted in the oxide. Placing the phosphorus dopant in a conductor (such as a polysilicon gate) alleviates the polarization problem, thus reducing threshold voltage shifts by more than an order of magnitude. The offset voltage drift with time has been calculated to be typically 0.1µV/month, including the first month of operation.

Because of the extremely high input impedance and resulting low bias current requirements, the TLC27M2 and TLC27M7 are well suited for low-level signal processing; however, leakage currents on printed-circuit boards and sockets can easily exceed bias current requirements and cause a degradation in device performance. It is good practice to include guard rings around inputs (similar to those of Figure 4 in the Parameter Measurement Information section). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input (see Figure 40).

The inputs of any unused amplifiers should be tied to ground to avoid possible oscillation.

noise performance

The noise specifications in operational amplifier circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias current requirements of the TLC27M2 and TLC27M7 result in a very low noise current, which is insignificant in most applications. This feature makes the devices especially favorable over bipolar devices when using values of circuit impedance greater than 50 k Ω , since bipolar devices exhibit greater noise currents.



(a) NONINVERTING AMPLIFIER

Figure 40. Guard-Ring Schemes

output characteristics

The output stage of the TLC27M2 and TLC27M7 is designed to sink and source relatively high amounts of current (see typical characteristics). If the output is subjected to a short-circuit condition, this high current capability can cause device damage under certain conditions. Output current capability increases with supply voltage.

All operating characteristics of the TLC27M2 and TLC27M7 were measured using a 20-pF load. The devices drive higher capacitive loads; however, as output load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation (see Figure 41). In many cases, adding a small amount of resistance in series with the load capacitance alleviates the problem.



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(c) UNITY-GAIN AMPLIFIER

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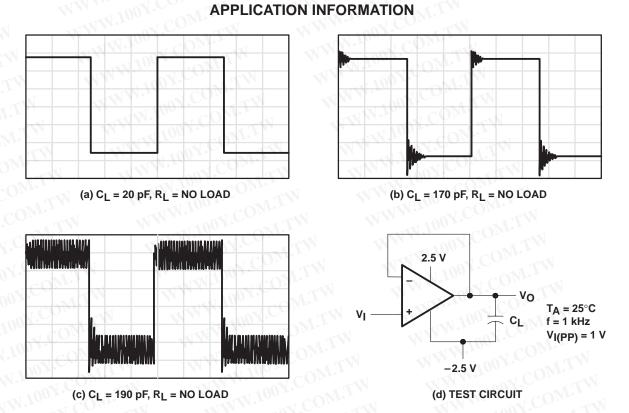


Figure 41. Effect of Capacitive Loads and Test Circuit

output characteristics (continued)

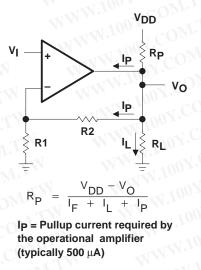
Although the TLC27M2 and TLC27M7 possess excellent high-level output voltage and current capability, methods for boosting this capability are available, if needed. The simplest method involves the use of a pullup resistor (R_P) connected from the output to the positive supply rail (see Figure 42). There are two disadvantages to the use of this circuit. First, the NMOS pulldown transistor N4 (see equivalent schematic) must sink a comparatively large amount of current. In this circuit, N4 behaves like a linear resistor with an on-resistance between approximately 60Ω and 180Ω , depending on how hard the op amp input is driven. With very low values of R_P , a voltage offset from 0 V at the output occurs. Second, pullup resistor R_P acts as a drain load to N4 and the gain of the operational amplifier is reduced at output voltage levels where N5 is not supplying the output current.



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APPLICATION INFORMATION

output characteristics (continued)





vo

Figure 42. Resistive Pullup to Increase VOH



feedback

Operational amplifier circuits nearly always employ feedback, and since feedback is the first prerequisite for oscillation, some caution is appropriate. Most oscillation problems result from driving capacitive loads (discussed previously) and ignoring stray input capacitance. A small-value capacitor connected in parallel with the feedback resistor is an effective remedy (see Figure 43). The value of this capacitor is optimized empirically.

electrostatic-discharge protection

The TLC27M2 and TLC27M7 incorporate an internal electrostatic-discharge (ESD) protection circuit that prevents functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2. Care should be exercised, however, when handling these devices as exposure to ESD may result in the degradation of the device parametric performance. The protection circuit also causes the input bias currents to be temperature dependent and have the characteristics of a reverse-biased diode.

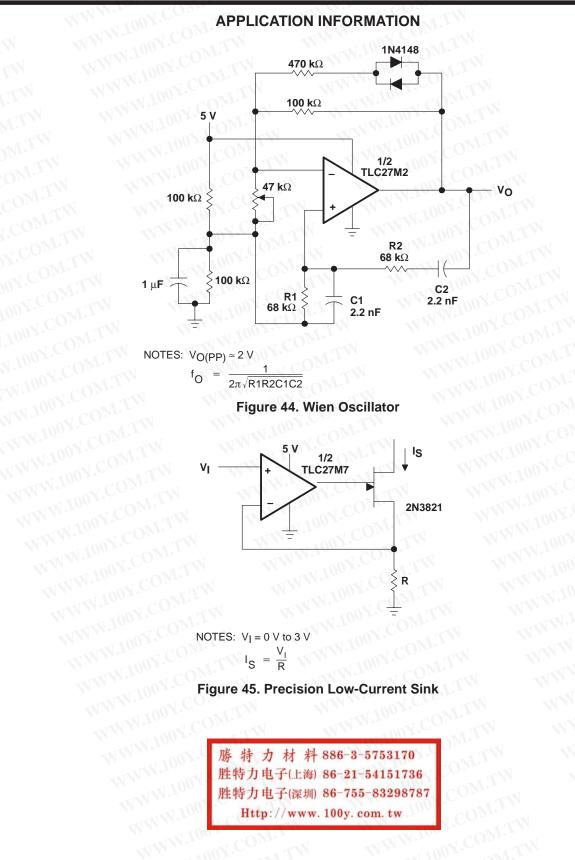
latch-up

Because CMOS devices are susceptible to latch-up due to their inherent parasitic thyristors, the TLC27M2 and TLC27M7 inputs and outputs were designed to withstand –100-mA surge currents without sustaining latch-up; however, techniques should be used to reduce the chance of latch-up whenever possible. Internal protection diodes should not, by design, be forward biased. Applied input and output voltage should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 μ F typical) located across the supply rails as close to the device as possible.

The current path established if latch-up occurs is usually between the positive supply rail and ground and can be triggered by surges on the supply lines and/or voltages on either the output or inputs that exceed the supply voltage. Once latch-up occurs, the current flow is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor and usually results in the destruction of the device. The chance of latch-up occurring increases with increasing temperature and supply voltages.

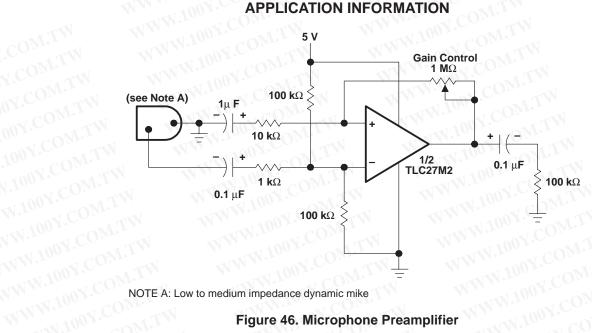


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NOTE A: Low to medium impedance dynamic mike

Figure 46. Microphone Preamplifier

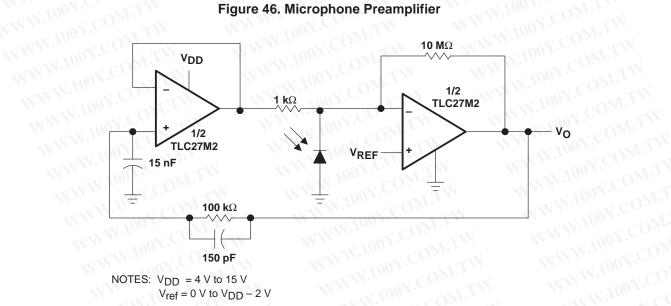


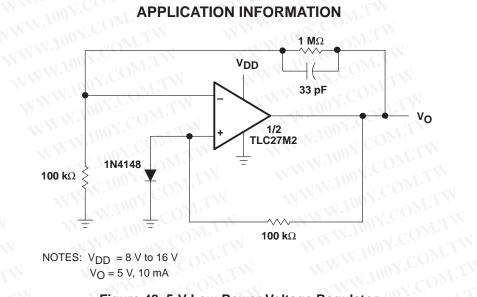
Figure 47. Photo-Diode Amplifier With Ambient Light Rejection

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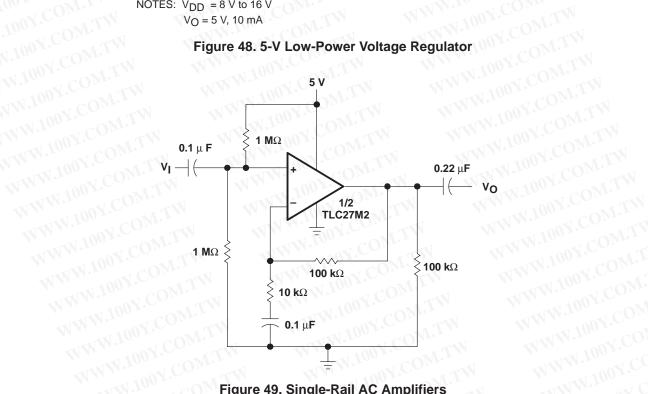
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Vo = 5 V, 10 mA

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