- Trimmed Offset Voltage: TLC27M9 . . . 900 μ V Max at T_A = 25°C, V_{DD} = 5 V
- Input Offset Voltage Drift ... Typically 0.1 μV/Month, Including the First 30 Days
- Wide Range of Supply Voltages Over Specified Temperature Range: 0°C to 70°C...3 V to 16 V -40°C to 85°C...4 V to 16 V -55°C to 125°C...4 V to 16 V
- Single-Supply Operation
- Common-Mode Input Voltage Range Extends Below the Negative Rail (C-Suffix, I-Suffix Types)
- Low Noise . . . Typically 32 nV/\/Hz at f = 1 kHz
- Low Power . . . Typically 2.1 mW at T_A = 25°C, V_{DD} = 5 V
- Output Voltage Range Includes Negative Rail
- High Input Impedance . . . 10¹² Ω Typ
- ESD-Protection Circuitry
- Small-Outline Package Option Also Available in Tape and Reel
- Designed-In Latch-Up Immunity

description

The TLC27M4 and TLC27M9 quad operational amplifiers combine a wide range of input offset voltage grades with low offset voltage drift, high input impedance, low noise, and speeds comparable to that of general-purpose bipolar devices. These devices use Texas Instruments silicon-gate LinCMOS[™] technology, which provides offset voltage stability far exceeding the stability available with conventional metal-gate processes.

The extremely high input impedance, low bias currents, make these cost-effective devices ideal for applications that have previously been reserved for general-purpose bipolar products, but with only a fraction of the power consumption.



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NC - No internal connection

DISTRIBUTION OF TLC27M9 INPUT OFFSET VOLTAGE





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description (continued)

Four offset voltage grades are available (C-suffix and I-suffix types), ranging from the low-cost TLC27M4 (10 mV) to the high-precision TLC27M9 (900 μ V). These advantages, in combination with good common-mode rejection and supply voltage rejection, make these devices a good choice for new state-of-the-art designs as well as for upgrading existing designs.

In general, many features associated with bipolar technology are available on LinCMOS[™] operational amplifiers, without the power penalties of bipolar technology. General applications such as transducer interfacing, analog calculations, amplifier blocks, active filters, and signal buffering are easily designed with the TLC27M4 and TLC27M9. The devices also exhibit low voltage single-supply operation, and low power consumption, making them ideally suited for remote and inaccessible battery-powered applications. The common-mode input voltage range includes the negative rail.

A wide range of packaging options is available, including small-outline and chip-carrier versions for high-density system applications.

The device inputs and outputs are designed to withstand -100-mA surge currents without sustaining latch-up.

The TLC27M4 and TLC27M9 incorporate internal ESD-protection circuits that prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015; however, care should be exercised in handling these devices, as exposure to ESD may result in the degradation of the device parametric performance.

The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from -40°C to 85°C. The M-suffix devices are characterized for operation over the full military temperature range of -55°C to 125°C.

			AVAILABL	E OPTIONS			
NW.10			WW.IV	PACKAGE	i IIa	NWW.	COM TV
TA	V _{IO} max AT 25°C	SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)	TSSOP (PW)	FORM (Y)
W	900 μV	TLC27M9CD	<u> </u>	1.100 × cO	TLC27M9CN	I.W.T	- EOM.
000 to 7000	2 mV	TLC27M4BCD	- NN	N 1002.00	TLC27M4BCN	<u> </u>	Mont - 100
0°C to 70°C	5 mV	TLC27M4ACD	WW-	N.C.	TLC27M4ACN	At W	1005-00-
	10 mV	TLC27M4CD		W.100	TLC27M4CN	 	TLC27M4Y
A.	900 μV	TLC27M9ID		M. HOV	TLC27M9IN	-	4.100 <u>-</u> CC
40%C to 95%C	2 mV	TLC27M4BID	1 - 1	100Y	TLC27M4BIN		W.1001.C
-40°C 10 85°C	5 mV	TLC27M4AID	$\sim - \infty$	WW - 001	TLC27M4AIN	$-\sqrt{N}$	1707.0
	10 mV	TLC27M4ID		WWW.100	TLC27M4IN	TLC27M41PW	NN.
55°C to 125°C	900 μV	TLC27M9MD	TLC27M9MFK	TLC27M9MJ	TLC27M9MN		WW-100
-55°C 10 125°C	10 mV	TLC27M4MD	TLC27M4MFK	TLC27M4MJ	TLC27M4MN	v _ v	NN.1007

The D and PW package is available taped and reeled. Add R suffix to the device type (e.g., TLC279CDR).



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TLC27M4Y chip information

This chip, when properly assembled, displays characteristics similar to the TLC27M4C. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V _{DD} (see Note 1)	18 V
Differential input voltage, VID (see Note 2)	±Vחס
Input voltage range, V _I (any input)	-0.3 V to V
	±5 mA
Output current. In (each output)	+30 mA
Total current into V	45 mA
Total current out of GND	45 mA
Duration of short-circuit current at (or below) 25°C (see Note 3)	unlimited
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature T_A : C suffix	0°C to 70°C
	-40°C to 85°C
M suffix	-55°C to 125°C
Storage temperature range	-65°C to 150°C
Case temperature for 60 seconds: FK package	
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, N, or PW	backage 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package .	300°C

WWW [†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.

2. Differential voltages are at IN+ with respect to IN-.

3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded (see application section).

DISSIPATION RATING TABLE

PACKAGE	T _A ≤ 25°C POWER RATING	DERATING FACTOR ABOVE T _A = 25°C	T _A = 70°C POWER RATING	T _A = 85°C POWER RATING	T _A = 125°C POWER RATING
Dool	950 mW	7.6 mW/°C	608 mW	494 mW	10010M.
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
J.100	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
N	1575 mW	12.6 mW/°C	1008 mW	819 mW	N.100 - CON
PW	700 mW	5.6 mW/°C	448 mW	<u> </u>	$100\underline{1}$

recommended operating conditions

WW.100 - C	ON	C SU	FFIX	I SUF	FIX	M SU	FFIX	
		MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, V _{DD}	WITH WWW.	3	16	4	16	4	16	V
Common mode input veltage Vie	$V_{DD} = 5 V$	-0.2	3.5	-0.2	3.5	0	3.5	
Common-mode input voltage, vIC	V _{DD} = 10 V	-0.2	8.5	-0.2	8.5	0	8.5	VC
Operating free-air temperature, TA	N. T. W. T. W.	0	70	-40	85	-55	125	°C

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electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

OM.	PARAMETER	N.100Y.CON	TEST CONI	DITIONS			.C27M4 .C27M4 .C27M4 .C27M4 .C27M9	C AC BC C	UNIT
			M.TV		T CON	MIN	TYP	MAX	1
	W WILL	TI 0071440	V _O = 1.4 V,	$V_{IC} = 0,$	25°C	1.1	1.1	10	
		TLC27M4C	R _S = 50 Ω,	$R_L = 100 \text{ k}\Omega$	Full range	TIM	N	12	
		TI COZNALAC	$V_{O} = 1.4 V_{,}$	$V_{IC} = 0,$	25°C	. T	0.9	5	mv
	land affect wells as	TLC27M4AC	$R_{S} = 50 \Omega,$	$R_L = 100 k\Omega$	Full range	OM.	M	6.5	1
VIO	input onset voltage	TI COZADO	V _O = 1.4 V,	$V_{IC} = 0,$	25°C	COM	250	2000	
		TLC274BC	R _S = 50 Ω,	$R_L = 100 \text{ k}\Omega$	Full range		U.L.M.	3000	
		TI C270C	V _O = 1.4 V,	V _{IC} = 0,	25°C	1.005	210	900	μν
1.100	COMPT	TLC279C	R _S = 50 Ω,	RL = 100 kΩ	Full range	A CO	Mre	1500	
×VIO	Average temperature co offset voltage	efficient of input	IOUX.COM.T		25°C to 70°C	NY.C	1.7	W1	μV/°C
.W.)	Insuit offent summer /	Note 4)	No. 25V		25°C	N.V.	0.1	Wm	~ ^
10	input onset current (see	NU(e 4)	vO = 2.5 V,	vIC = 2.5 v	70°C	The state	07	300	рА
14 T.		lata ()			25°C	1001	0.6	1.1	
IB	Input bias current (see h	input bias current (see Note 4)		VIC = 2.5 V	70°C		40	600	рА
WW	Common-mode input vo		WW.100Y.CO	DN.TW	25°C	-0.2 to 4	-0.3 to 4.2	OM.	V
VICR	(see Note 5)		WWW.1001.		Full range	-0.2 to 3.5	1001.	COM	V
	1001.00	W.FW	W.1003	COM.	25°C	3.2	3.9	-1 C O	N
′он	High-level output voltage	WTT 6	V _{ID} = 100 mV,	R _L = 100 kΩ	0°C	3	3.9	1	V
	WWW.LOOV.C		WWW.	N.COM	√ 70°C	3	4	01.0	- 11
	WW.IOU	-0N1	WW.10	N COM	25°C	VI	0	50	O.
/OL	Low-level output voltage	COMTY	$V_{ID} = -100 \text{ mV},$	$I_{OL} = 0$	0°C		0	50	mV
	WW 100Y		NW.	1001.00	70°C	A.	0	50	CON
	WWW	V.COM TW	Man	100Y.CO.	25°C	25	170	1100	1.0
AVD	Large-signal differential		$V_{O} = 0.25 V \text{ to } 2 V,$	$R_L = 100 \text{ k}\Omega$	0°C	15	200	N.S.	V/mV
	voitage amplification				70°C	15	140	W.10	
	WW	T.M. 1.100	A AN	W.1001.	25°C	65	91	W.1	10
MRR	Common-mode rejection	n ratio	VIC = VICRmin		0°C	60	91		dB
			Va No		70°C	60	92	WW.	Ynor
		V.100 COM		WW.Iou	25°C	70	93	VW1z	
SVR	Supply-voltage rejection	ratio	$V_{DD} = 5 V \text{ to } 10 V,$	V _O = 1.4 V	0°C	60	92	N	dB
		VI ONY.CO	WTD	WW TIO	70°C	60	94	AL.	10
	AL	VW. POSTOC	No.	NWW.	25°C	Wr.	420	1120	
DD	Supply current (four amp	olifiers)	$V_{O} = 2.5 V$,	V _{IC} = 2.5 V,	0°C	1	500	1280	μA
	N	V 100Y.C	i to load	W T	70°C	M	340	880	W.

[†] Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

5. This range also applies to each input individually.



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electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

	PARAMETER		TEST CON	DITIONS	T _A †		.C27M4 .C27M4 .C27M4 .C27M4	C AC BC C	UNIT
		100 L. COM			CONT	MIN	TYP	MAX	
I.Mo	W W.	TLC27MAC	V _O = 1.4 V,	$V_{IC} = 0,$	25°C	-1	1.1	10	
		TEC271014C	R _S = 50 Ω,	$R_L = 100 \text{ k}\Omega$	Full range	LM.		12	m\/
		TI C27MAAC	V _O = 1.4 V,	$V_{IC} = 0,$	25°C	WT	0.9	5	IIIV
Vio	Input offset voltage	TEO2/INITAO	R _S = 50 Ω,	$R_L = 100 \ k\Omega$	Full range	-		6.5	
VIO	input onset voltage	TI C27M4BC	V _O = 1.4 V,	$V_{IC} = 0,$	25°C	1.1	260	2000	
		TEGETIMITEG	R _S = 50 Ω,	$R_L = 100 \text{ k}\Omega$	Full range	T.I.	N	3000	иV
		TI C27M9C	V _O = 1.4 V,	$V_{IC} = 0,$	25°C	T	220	1200	μν
	'0 ^{N.1}	TEGETINGG	R _S = 50 Ω,	R _L = 100 kΩ	Full range	Òù.	M	1900	
αΛΙΟ	Average temperature coe offset voltage	efficient of input	K.COM.TW		25°C to 70°C		2.1		μV/°C
700		Nata A			25°C	COP	0.1		- 0
10	input onset current (see	Note 4)	$v_0 = 5 v$,	vIC = p v	70°C	-1 CO	7	300	рА
	Innut biog ourrent (oog N	lata ()			25°C	1.	0.7		~ ^
IΒ	input bias current (see N	lote 4)	$v_{O} = 5 v,$	vIC = 2 v	70°C	01.0	50	600	рА
NW.L	Common-mode input vol	tage range	V.100Y.COM	TW.	25°C	-0.2 to 9	-0.3 to 9.2	TW	V
VICR	(see Note 5)	WW 1	W.100 ² .CON		Full range	-0.2 to 8.5	N.CO	M.TY	v
W	W1001. ONL	11 - VI	W.100 - C(DW. F	25°C	8	8.7	0_{Nr}	
Vон	High-level output voltage	V WI	V _{ID} = 100 mV,	$R_L = 100 \text{ k}\Omega$	0°C	7.8	8.7	Mor	V
			WWW. IODY.C		70°C	7.8	8.7		WT.
	WW.IV CON	W.	WWW.LOOV	COM	25°C	MA.	0	50	WT.
VOL	Low-level output voltage		$V_{ID} = -100 \text{ mV},$	$I_{OL} = 0$	0°C	WW	0	50	mV
-	WW TIOOX.CO	WT.M.	W 100	T.Mon.T	70°C		0	50	M.L
	M.M.M. OOX.CC	WTI	WW 100	Y.Com	25°C	25	275	01.0	M
A _{VD}	Large-signal differential		$V_{O} = 1 V \text{ to } 6 V,$	$R_L = 100 \text{ k}\Omega$	0°C	15	320	any.	V/mV
	volage amplification	COM.1	L.W.W.	T COM	70°C	15	230		COM
	W V 100Y.	M.TW	N. T.	1001.00	25°C	65	94	700,	CON
CMRR	Common-mode rejection	ratio	$V_{IC} = V_{ICR}min$		0°C	60	94	1100	dB
	WW.Ioc	V.CONI.	WWW	vov.CO	70°C	60	94	10	N.CO
	10°	COM.1	With the second	W.Ino. CO	25°C	70	93	4.10	J.V.
k SVR	Supply-voltage rejection $(\Delta V \rho \sigma / \Delta V \rho)$	ratio	$V_{DD} = 5 V \text{ to } 10 V,$	V _O = 1.4 V	0°C	60	92	1.W.	dB
		MY.COM	WW WW	1004.6	70°C	60	94		001.
	WWW.	ON.COM		You - only	25°C	N	570	1200	1001
IDD	Supply current (four amp	lifiers)	$V_{O} = 5 V$,	$V_{IC} = 5 V,$	O°C	X	690	1600	μA
	NN.	N 100Y.	1 to loud	100°	70°C		440	1120	N.100

5. This range also applies to each input individually.



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electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

	PARAMETER	W.100Y.CO	TEST CONI	DITIONS	TAT		.C27M4 .C27M4 .C27M4 .C27M4 .C27M9	i Ai Bi I	UNIT
(0)	V.7	W.100 F.C.	MA	WW.I	COV	MIN	TYP	MAX	
		TI C27M4I	V _O = 1.4 V,	V _{IC} = 0,	25°C	Nr.	1.1	10	
		TEOZYMA	R _S = 50 Ω,	R _L = 100 kΩ	Full range	TIM		13	m\/
		TI C27MAAL	V _O = 1.4 V,	$V_{IC} = 0,$	25°C		0.9	5	
10	Input offset voltage	TECZTWIAAT	R _S = 50 Ω,	RL = 100 kΩ	Full range	OM.		6.5	
10	input onset voltage	TI COZMARI	V _O = 1.4 V,	V _{IC} = 0,	25°C	COM	250	2000	
		TECZTWI4DI	R _S = 50 Ω,	$R_L = 100 \text{ k}\Omega$	Full range		I.T.W	3000	
		TI C27MQI	V _O = 1.4 V,	V _{IC} = 0,	25°C	1.001	210	900	μν
100	CONCIL	TECZTWIST	R _S = 50 Ω,	R _L = 100 kΩ	Full range	J CO	Mrez	2000	
vio	Average temperature co offset voltage	efficient of input	ONY.COMIT		25°C to 85°C	ov.C	1.7	W	μV/°C
N.	Input offent summer (Note ()	No OF	N- 05V	25°C	N.	0.1	Wm	- ^
)	input onset current (see	NUCE 4)	vO = 2.5 V,	vIC = 2.5 v	85°C	Too	24	1000	рА
	Input biog current (and b	loto (1)	Vo-25V		25°C	1001	0.6	1.1	r A
N	input bias current (see N	lote 4)	vo = 2.5 v,	VIC = 2.5 V	85°C	100	200	2000	рА
N W	Common-mode input vo	Itage range	WW.100Y.CO	DM.TW	25°C	-0.2 to 4	-0.3 to 4.2	OM.I	V
ICR	(see Note 5)	LTW	WWW.100Y.C		Full range	-0.2 to 3.5	1001.	^{1.} CO _M	V
	W.100 CO	M.	WW.IO	COM	25°C	3.2	3.9	1 CO	11.
н	High-level output voltage	WT.M	V _{ID} = 100 mV,	$R_L = 100 k\Omega$	-40°C	3	3.9	- 0	V
			WWW	N.T.	85°C	3	4	07.2	I.M.
	N.W.W.	OW.	WWW.	ov.com	25°C	VV	0	50	
)L	Low-level output voltage		$V_{ID} = -100 \text{ mV},$	$I_{OL} = 0$	-40°C	-	0	50	mV
			W T		85°C		0	50	100
	WW TOO	NTN	A.A.	100%.	25°C	25	170	N 100	1
VD	Large-signal differential		$V_{O} = 0.25 \text{ V to 2 V},$	$R_L = 100 \text{ k}\Omega$	-40°C	15	270	- 10	V/mV
	voltage amplification		A TAN		85°C	15	130	M.r.	V.C
	I I	NOT. ONIT		W.100 1	25°C	65	91	I.W.	00-10
MRR	Common-mode rejection	n ratio	VIC = VICRmin		-40°C	60	90		dB
			W W		85°C	60	90		Yoor
	VID	100 COM		WW.10	25°C	70	93	VIVIA	
VR	Supply-voltage rejection $(A)(a = (A)(a = b))$	ratio	$V_{DD} = 5 V \text{ to } 10 V,$	V _O = 1.4 V	-40°C	60	91		dB
-			WIL	101	85°C	60	94	VI.	×10
	VIA	W. M. CC	Wn	WWW.	25°C	WTS	420	1120	
DD	Supply current (four amp	olifiers)	$V_0 = 2.5 V_1$	V _{IC} = 2.5 V,	-40°C	1	630	1600	μA
-		100%.0	INO IOAD		85°C	M.ª	320	800	AV.

5. This range also applies to each input individually.



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electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

NT.W	PARAMETER	ov.com.T	TEST CON	DITIONS	TAT		.C27M4 .C27M4 .C27M4 .C27M4 .C27M9	I Al Bl	UNIT
M.T					COM.1	MIN	TYP	MAX	
CIM		TICOZNAL	$V_{O} = 1.4 V_{,}$	$V_{IC} = 0,$	25°C		1.1	10	
One		1202710141	R _S = 50 Ω,	$R_L = 100 \text{ k}\Omega$	Full range	L.M.		13	
COM		TI COZMANI	V _O = 1.4 V,	$V_{IC} = 0,$	25°C	WT	0.9	5	IIIV
Vie		TEG27IWI4AI	R _S = 50 Ω,	$R_L = 100 \text{ k}\Omega$	Full range	In		7	
VI0	input onset voltage	TI C27M/BI	V _O = 1.4 V,	V _{IC} = 0,	25°C	1.1	260	2000	
N.CO		TECZTWI4DI	R _S = 50 Ω,	$R_L = 100 \text{ k}\Omega$	Full range	T.M.		3500	
V.C		TI C27M9I	V _O = 1.4 V,	$V_{IC} = 0,$	25°C	T	220	1200	μν
	'0M.1'	TEGETIMOT	R _S = 50 Ω,	$R_L = 100 k\Omega$	Full range	Ò'n.	N/a	2900	
ανιο	Average temperature coel offset voltage	fficient of input	V.COM.TW	WW	25°C to 85°C	CON.	2.1		μV/°C
700	Input offect ourrest (acc.)	loto ()		Via – E.V	25°C		0.1		۳Å
1000	input onset current (see N	IOLE 4)	$v_0 = 5 v$,	vIC = 2 v	85°C	-1 CO	26	1000	рА
10	Input biog ourrapt (ago No	to (1)	Vo - EV		25°C	1	0.7		n A
чв	input bias current (see No	ne 4)	$v_{O} = 5 v,$	vIC = 2 v	85°C	04.0	220	2000	рА
MM.T	Common-mode input	WWW WWW	W.100Y.COM	TW	25°C	-0.2 to 9	-0.3 to 9.2	WT.	V
VICR	voltage range (see Note 5		W.100Y.CON		Full range	-0.2 to 8.5	V.COL	MT	v
	W.100 - COM.1		WW.Ioo C	OM.	25°C	8	8.7	ON.	W
VOH	High-level output voltage		V _{ID} = 100 mV,	$R_L = 100 \text{ k}\Omega$	-40°C	7.8	8.7	^{0}M	V
W	WW. 100Y.COM	WT	WW 100X.	WIM	85°C	7.8	8.7		T.
-	WW.LOW.COW	Wm	WWW.	CON TW	25°C 🔨		0	50	WTN
VOL	Low-level output voltage		$V_{ID} = -100 \text{ mV},$	$I_{OL} = 0$	-40°C	NWIX	0	50	mV
-	W 100X.	M.T.W	W 1.100	COM.	85°C	T	0	50	$M \cdot 1$
	WW 1001.00	WILIA	WW 10	T.M.	25°C	25	275	01.5	M.T
AVD	Large-signal differential		$V_{O} = 1 V \text{ to } 6 V,$	$R_L = 100 \text{ k}\Omega$	-40°C	15	390	00Y.	V/mV
	voltage amplification	OM.	L.WW.L	COM.	85°C	15	220	Van	COM
	W	COM.T.	WIG	100 1. CON	25°C	65	94	700	CON
CMRR	Common-mode rejection	ratio	$V_{IC} = V_{ICR}min$		-40°C	60	93	v100	dB
	WWW.L	V.COMPTY	N WWW		85°C	60	94	110	Y.C
		T COM.	WIN IN		25°C	70	93	N.	N.CC
^k SVR	Supply-voltage rejection r_{i}	atio	$V_{DD} = 5 V \text{ to } 10 V,$	V _O = 1.4 V	-40°C	60	91	VN.V	dB
		DOY.COM	W AN	1007.0	85°C	60	94	- NI	100x.
	WWW.	MY.COM		Vielevol	25°C	N	570	1200	1001.
IDD	Supply current (four ampli	fiers)	$v_{O} = 5 v$, No load	VIC = 5 V,	-40°C	N	900	1800	μA
	W				85°C		410	1040	N.100

[†] Full range is –40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

5. This range also applies to each input individually.



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electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

	PARAMETER		TEST CON	DITIONS	CTAT	TL	C27M4I C27M9I	VI VI	UNIT
			Λ . T	W.100	COM	MIN	TYP	MAX	
CO P	TH WW	TIOOTIAAA	$V_{0} = 1.4 V_{0}$	$V_{IC} = 0.$	25°C	T.V.	1.1	10	
COV		TLC27M4M	$R_S = 50 \Omega$,	$R_L = 100 \text{ k}\Omega$	Full range	WT		12	mv
VIO	Input offset voltage	TIOOTIANA	$V_{O} = 1.4 V_{0}$	$V_{IC} = 0$,	25°C	Nr.	210	900	
		TLC27M9M	$R_S = 50 \Omega$,	$R_L = 100 \text{ k}\Omega$	Full range	M.T		3750	μv
ανιο	Average temperature coefficient offset voltage	ent of input	COMITY	WW.	25°C to 125°C	OM.T	1.7		μV/°C
00Y.	hand the second free black	100	N. OFV	N 0.5.V	25°C	Mos	0.1		pА
10	Input offset current (see Note	4)	VO = 2.5 V,	VIC = 2.5 V	125°C		1.4	15	nA
100 -		N.W.N	N- 0.5 V		25°C	1 COM	0.6		pА
IB	input bias current (see Note 4	+)	vO = 2.5 v,	VIC = 2.5 V	125°C	0	9	35	nA
W.10	Common-mode input voltage	range	00Y.COM.TY		25°C	0 to 4	-0.3 to 4.2		V
VICR	(see Note 5)	WWW WWW	V.100Y.COM		Full range	0 to 3.5	COM	TW	V
	100x ONLY		W.100 L. CON	1 .	25°C	3.2	3.9		s1
√он	High-level output voltage		V _{ID} = 100 mV,	RL = 100 kΩ	−55°C	3	3.9	M.T	V
WIN	W.10 V.COM.		LAN. TODA'CO	WT	125°C	3	4	11	N
	W.Ine COM-	Ĩ.	WW.10 STC	DIVI	25°C	M.	0	50	W
/OL	Low-level output voltage		$V_{ID} = -100 \text{ mV},$	$I_{OL} = 0$	−55°C	1.1/1	0	50	mV
			NW TOOX.		125°C	- 1	000	50	MT.I
	COM.	N.	Van WWW.	COMM	25°C <	25	170		17
AVD	Large-signal differential		$V_{O} = 0.25 V \text{ to } 2 V,$	V, $R_L = 100 k\Omega$	−55°C	15	290	<1 CO	V/mV
	voltage amplification	M	WW 100	I.M.T	125°C	15	120		M.
	WWW. LOW.COM	Wn.	WWW	N.CO.	25°C	65	91	01.0	- 11
CMRR	Common-mode rejection ratio	0	$V_{IC} = V_{ICR}min$		−55°C	60	89		dB
	WW 1007.0	VT.M.	L Krong 1	Mor. COM	125°C	60	91	00 -	CON
	Cumply units as asis sting again	WT	WW.	100Y.CC.	25°C	70	93	1001	
K SVR	Supply-voltage rejection ratio		$V_{DD} = 5 V \text{ to } 10 V,$	V _O = 1.4 V	-55°C	60	91		dB
		M.T.V	N. A.	1.100 . 00	125°C	60	94	1.100	-100
	WW INOY.	VT1	Vo - 25 V	VID DEV	25°C		420	1120	J
DD	Supply current (four amplifie	rs)	$v_0 = 2.5 v$, No load	VIC = 2.5 V,	-55°C		680	1760	μA
	N 100 '	COM-1		W.Juv-	125°C		280	720	×7



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electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

	PARAMETER		TEST CON	NDITIONS	T⊿t	TL	C27M9	N	UNIT
T.T.W	W.I.	Mon		W.100 F	COM.	MIN	TYP	MAX	
TI	N WW.	TI C27MAM	V _O = 1.4 V,	V _{IC} = 0,	25°C		1.1	10	m\/
10	Input offset voltage	TECZ71014101	R _S = 50 Ω,	R _L = 100 kΩ	Full range			12	IIIV
VIO	input onset voltage	TI COZNADNA	V _O = 1.4 V,	V _{IC} = 0,	25°C	N .	220	1200	
Ma	IN N.	TECZTIVISIVI	R _S = 50 Ω,	$R_L = 100 \text{ k}\Omega$	Full range			4300	μv
αVIO	Average temperature coe offset voltage	fficient of input	OM.TW	I.WWW.I	25°C to 125°C	.TW	2.1		μV/°C
	Input offect ourrest (acc.)	late (1)		Via EV	25°C	1.	0.1		pА
10	input onset current (see r	Note 4)	$v_{O} = 5 v,$	vIC = 2 v	125°C	W.	1.8	15	nA
N.C.	In with the summer to an a N	100	No. EN		25°C	T.M.	0.7		pА
IB	input bias current (see No	ote 4)	vO = 5 v,	vIC = 2 v	125°C	Or al	10	35	nA
1001	Common-mode input volt	age range	OY.COM.TV	VW I	25°C	0 to 9	-0.3 to 9.2		V
VICR	(see Note 5)		100 1. 100X.COM.1		Full range	0 to 8.5	M.T	N N	V
	ON.T.		N.100 T. COM		25°C	8	8.7		
∕он	High-level output voltage		V _{ID} = 100 mV,	$R_L = 100 \text{ k}\Omega$	−55°C	7.8	8.6	T.	V
			W.LOOY.CO		125°C	7.8	8.8	NT.N	
VIII	.100 COM.		NN.1 SCC	N. T.	25°C		0	50	N N
/OL	Low-level output voltage		$V_{ID} = -100 \text{ mV},$	$I_{OL} = 0$	−55°C	1.100	0	50	mV
	100Y.COMIT		100Y.C	WT.ING	125°C	V.10	0	50	
WW	N. COM	W	NW 100Y.	WTN	25°C	25	275		LM
AVD	Large-signal differential		$V_{O} = 1 V \text{ to } 6 V,$	$R_L = 100 \text{ k}\Omega$	-55°C	15	420	COM	V/mV
	voltage amplification		WW.100	COM.1	125°C	15	190	CON	
V	1001.00	WT.N	W 100	Y. OM.TY	25°C	65	94	. ~0	V.L
CMRR	Common-mode rejection	ratio	VIC = VICRmin		√ –55°C	60	93	1.00	dB
			WWW.L		125°C	60	93	N.C	
	1001.	OW.L	.WW.	COM.	25°C	70	93		ON.
SVR	Supply-voltage rejection (atio	$V_{DD} = 5 V \text{ to } 10 V,$	V _O = 1.4 V	−55°C	60	91	00 r.	dB
		WT	WWW	1004.001	125°C	60	94	1001	
	WWW.IO	CONTRACT	WW	N. CO	25°C	1	570	1200	1.00.
DD	Supply current (four ampl	lifiers)	VO = 5 V,	VIC = 5 V,	−55°C		980	2000	μA
					125°C		360	960	



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electrical characteristics, V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

- 1	The same terms of the second second	TEAT OON		Т	.C27M4	Y	
OM.	PARAMETER	TEST CONI	DITIONS	MIN	TYP	MAX	UNIT
VIO	Input offset voltage	V _O = 1.4 V, R _S = 50 Ω,	$V_{IC} = 0,$ $R_L = 100 \text{ k}\Omega$	WT.	1.1	10	mV
ανιο	Temperature coefficient of input offset voltage	$T_{A} = 25^{\circ}C \text{ to } 70^{\circ}C$	1004.00	WIN	1.7		μV/°C
lio	Input offset current (see Note 4)	V _O = 2.5 V,	V _{IC} = 2.5 V	17.	0.1		pА
I _{IB}	Input bias current (see Note 4)	V _O = 2.5 V,	V _{IC} = 2.5 V	0.11.	0.6		pА
VICR	Common-mode input voltage range (see Note 5)	WILM M	WW.100Y.	-0.2 to 4	-0.3 to 4.2		V
VOH	High-level output voltage	V _{ID} = 100 mV,	$R_L = 100 \text{ k}\Omega$	3.2	3.9	4	V
VOL	Low-level output voltage	$V_{ID} = -100 \text{ mV},$	$I_{OL} = 0$	1.00	0	50	mV
AVD	Large-signal differential voltage amplification	$V_{O} = 0.25 V \text{ to } 2 V,$	RL= 100 kΩ	25	170	N	V/mV
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}min$	WW.IV	65	91		dB
k SVR	Supply-voltage rejection ratio (ΔVDD/ΔVIO)	V _{DD} = 5 V to 10 V,	V _O = 1.4 V	70	93		dB
IDD	Supply current (four amplifiers)	$V_{O} = 2.5 V,$ No load	V _{IC} = 2.5 V,	700X.	420	1120	μΑ

electrical characteristics, V_{DD} = 10 V, T_A = 25°C (unless otherwise noted)

	DADAMETER WITCH	TEAT CON	TEST CONDITIONS			Y	LINUT
	PARAMETER	TEST CON	MIN	TYP	MAX	UNIT	
VIO	Input offset voltage	$V_{O} = 1.4 V,$ R _S = 50 Ω ,	$V_{IC} = 0,$ $R_L = 100 \text{ k}\Omega$	NW.	1.1.	10	mV
ανιο	Temperature coefficient of input offset voltage	$T_A = 25^{\circ}C$ to $70^{\circ}C$	W N	1 M	2.1		μV/°C
IIO	Input offset current (see Note 4)	V _O = 5 V,	VIC = 5 V	NNY	0.1	Y.CO	pА
I _{IB}	Input bias current (see Note 4)	V _O = 5 V,	V _{IC} = 5 V	WIT	0.7	N.C	pА
VICR	Common-mode input voltage range (see Note 5)	W.100 1. CO	N.TW	-0.2 to 9	-0.3 to 9.2	00Y.	V
VOH	High-level output voltage	V _{ID} = 100 mV,	RL = 100 kΩ	8	8.7	100 .	V
VOL	Low-level output voltage	$V_{ID} = -100 \text{ mV},$	$I_{OL} = 0$		0	50	mV
A _{VD}	Large-signal differential voltage amplification	$V_{O} = 1 V \text{ to } 6 V,$	$R_{L} = 100 \text{ k}\Omega$	25	275		V/mV
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}min$	CONT.	65	94	W.L	dB
k SVR	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 5 V \text{ to } 10 V,$	V _O = 1.4 V	70	93	NN.1	dB
IDD	Supply current (four amplifiers)	$V_{O} = 5 V$, No load	V _{IC} = 5 V,	N	570	1200	μA



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.TV 1.TV	PARAMETER	TEST C	ONDITIONS	TA		.C27M4 .C27M4 .C27M4 .C27M4 .C27M9	C AC BC C	UNIT
M.1	W.100 P	OM.1	WW.100	J CONT.	MIN	TYP	MAX]
A.	LM M. 1001.	OM.TY	W.100	25°C	-1	0.43		
		WTN	VIPP = 1 V	0°C	UN	0.46]
	Classificate et units state	$R_L = 100 \Omega$,	WWW.	70°C	WT.	0.36		1//
SK	Siew rate at unity gain	CL = 20 pF, See Figure 1	·WW	25°C	- N	0.40		V/μs
		T.M.	VIPP = 2.5 V	0°C	1.1	0.43		1
		NTV YOUNTW	WW	70°C	M.T.Y	0.34		1
vn	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R _S = 20 Ω	25°C	OM.T	32		nV/√Hz
noV.	NTW WITH	1.001	M M	25°C	Mo	55		
Вом	Maximum output-swing bandwidth	$V_O = V_{OH}$	$C_L = 20 \text{ pF},$	0°C		60		kHz
		$K_{L} = 100 \text{ Ksz},$	See Figure 1	70°C	COM	50		1
1100	ON.I.	N.100 . CON	1.1.	25°C	-1 CO	525	* 1	
B ₁	Unity-gain bandwidth	$V_{I} = 10 \text{ mV},$	C _L = 20 pF,	0°C		610		kHz
		See Figure 5		70°C	07.0	400	N.	1
JW.	CONT.	NW. PO NC	DIVI.	25°C	N.V.C	40°	Wn	
φm 🔹	Phase margin	$V_{I} = 10 \text{ mV},$	$f = B_1$,	0°C	-100	41°		1
		$O_L = 20 \text{ pr},$	See Figure 5	70°C	1001.	39°	1.1	1

operating characteristics at specified free-air temperature, V_{DD} = 5 V

operating characteristics at specified free-air temperature, V_{DD} = 10 V

	PARAMETER	TEST	CONDITIONS	TA	TL TL TL TL	.C27M4 .C27M4 .C27M4 .C27M4	C AC BC C	UNIT
-	NAM TODY COM TA	WW	100Y. CONTY		MIN	TYP	MAX	I.T.Y
		WWW		25°C	NN	0.62	1.00	TIM
		WITT	VIPP = 1 V	0°C	WIR	0.67	V.C	Dist
P	Slew rate at unity gain	$R_{L} = 100 \Omega$,	W100 r. COM.	70°C		0.51		V/ue
	Siew rate at unity gain	See Figure 1	Vipp = 5.5 V	25°C		0.56	00x.	V/µS
		W W	V _{IPP} = 5.5 V	O°C	W	0.61	1001	
	W.100 L COM.		WW.100 CO	70°C	-	0.46	1.0	1.00
n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R _S = 20 Ω,	25°C	4	32	1.100	nV/√Hz
	NW.ION CON		J.V. WWW.L	25°C		35	V1	V.C
ОМ	Maximum output-swing bandwidth	$V_O = V_{OH}$	$C_L = 20 \text{ pF},$	0°C		40	NN'	kHz
		NL = 100 KS2,	See rigule r	70°C		30		100x.
	WWWWWWWWWW	WT	Van _ tool	25°C	N	635	NA .	1007
1	Unity-gain bandwidth	$V_{I} = 10 \text{ mV},$	C _L = 20 pF,	O°C	N	710	NWN	kHz
		See Figure 3		70°C		510	- N	N.100
	WWW 100X	WI.M.	NAME IO	25°C	IN	43°	At	N.10
m	Phase margin	$V_{I} = 10 \text{ mV},$	$f = B_1,$	-0°C	WT.	44°	AA.	
	- W.100	$C_{L} = 20 \text{ pr},$	See rigure 3	70°C		42°		NN

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EXAS

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operating characteristics at specified free-air temperature, V_{DD} = 5 V

ON. CON	PARAMETER	TEST CO	ONDITIONS	TAM	TLC27M TLC27M TLC27M TLC27M	41 4A1 4B1 91	UNIT
		COMPT		TCON	MIN TYP	MAX	1
	NITH WY 100	MIT	1.1	25°C	0.43		
V.C		OV.CONTW	VIPP = 1 V	-40°C	0.51]
en (Claur rate at unity gain	$R_L = 100 \Omega$	WWW.	85°C	0.35		1////
SK	Slew rate at unity gain	$C_L = 20 \text{ pr},$ See Figure 1	WW	25°C	0.40		V/μS
100%		1001. S. OM.T	VIPP = 2.5 V	-40°C	0.48	0.40 0.48 0.32 32 n]
100	WWW WR	Y.O.	N WW	85°C	0.32]
Vn	Equivalent input noise voltage	f = 1 kHz _, See Figure 2	R _S = 20 Ω,	25°C	32	N	nV/√Hz
- 10	OF.CONTRA NO	1002.	CIM W	25°C	55		
Вом	Maximum output-swing bandwidth	$V_O = V_{OH}$	$C_L = 20 \text{ pF},$	-40°C	75	TN	kHz
WIN.		KL = 100 KS2,	See Figure 1	85°C	45	Wm	1
	100 1. 011.1	W.100	MIT	25°C	525	1.1	
B ₁	Unity-gain bandwidth	$V_{l} = 10 \text{ mV},$	C _L = 20 pF,	-40°C	770	W.L.	kHz
WW		See rigure 5		85°C	370	The	
	W.IV CONL.	V. WW.IV	COM.	25°C	40°	UN	N
φm	Phase margin	$V_{I} = 10 \text{ mV},$	$f = B_1$, See Figure 3	-40°C	43°	-OM.	
W		0L - 20 pr,	oce rigule o	85°C	38°	M	J.V.

operating characteristics at specified free-air temperature, $V_{DD} = 10 V$

	PARAMETER	TEST	CONDITIONS	TA	TLC27M4I TLC27M4AI TLC27M4BI TLC27M9I	UNIT
	WWW. any.Com	WW W	-100Y.COM	M.C.	MIN TYP MAX	Mo
	WWW.PCONF.	WW IV	W ON.COM	25°C	0.62	
			VIPP = 1 V	-40°C	0.77	¹ CON
		$R_L = 100 \Omega$,	W.1001.	85°C	0.47	NGO
SR	Siew rate at unity gain	$C_L = 20 \text{ pF},$ See Figure 1	1001.0	25°C	0.56	v/μs
			V _{IPP} = 5.5 V	-40°C	0.70	Nov.Cu
		N	WW.100	85°C	0.44	O.V.C
Vn	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R _S = 20 Ω,	25°C	32	nV/√Hz
	WW.Ioo	ON.	WW.Lo	25°C	35	100
Вом	Maximum output-swing bandwidth	$V_O = V_{OH}$	$C_L = 20 \text{ pF},$	-40°C	45	kHz
		$K_{L} = 100 \text{ Ksz},$	See Figure 1	85°C	25	N.100
	WWW.	WT	WWW	25°C	635	-11
B ₁	Unity-gain bandwidth	$V_{I} = 10 \text{ mV},$	C _L = 20 pF,	-40°C	880	kHz
		See Figure 5		85°C	480	WW
	WW	MI.IN		25°C	43°	
φm	Phase margin	$V_{I} = 10 \text{ mV},$	$f = B_1$, Soo Figure 3	-40°C	46°	MN.
	WW	CL = 20 μr,	See Figure S	85°C	41°	WW



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PARAMETER	TEST	CONDITIONS	ТА	TLC27M4 TLC27M9	M	UNIT
	M.T.Y		OW.	MIN TYP	MAX	1
TW WW 100Y.C.	WT.W	N	25°C	0.43		
	WT	V _{IPP} = 1 V	−55°C	0.54		1
CD Clow rate at unity rain	$R_L = 100 \Omega$	WWW.Io.	125°C	0.29) //wa
SR Slew rate at unity gain	CL = 20 pF, See Figure 1	W.100	25°C	0.40		v/μs
		VIPP = 2.5 V	−55°C	0.50		1
	WT. OOM	WWW	125°C	0.28		1
V _n Equivalent input noise voltage	f = 1 kHz, See Figure 2	R _S = 20 Ω,	25°C	32		nV/√Hz
WWWWWWWWWWWWWWWWWWWWWWW	T I Store	N WW	25°C	55		1
BOM Maximum output-swing bandwidth	$V_O = V_{OH}$	$C_L = 20 \text{ pF},$	−55°C	80		kHz
	NL = 100 K32,	See Figure 1	125°C	40		1
100Y. M.T.W.	NICOL.	I. W.	25°C	525	1	
B1 Unity-gain bandwidth	$V_{I} = 10 \text{ mV},$	C _L = 20 pF,	−55°C	850	N	kHz
	See rigule 5		125°C	330	N	1
W.100 COM. 1	N. N. LOV	M.	25°C	40°	N/m	
φ _m Phase margin	$V_{I} = 10 \text{ mV},$	$f = B_1,$ See Figure 3	-55°C	44°]
	0 <u></u> = 20 pr,	occ rigule o	125°C	36°	TW]

operating characteristics at specified free-air temperature, V_{DD} = 5 V

operating characteristics at specified free-air temperature, V_{DD} = 10 V

WW	PARAMETER	TEST CO	ONDITIONS	TA	TLC27M4M TLC27M9M			UNIT
	NW.10° CONT.	WWW.Loo	V.COMMUN.	WW	MIN	ТҮР	MAX	W
		WW.Ioo	CONT.	25°C	NN.L	0.62	10 M	Wm
		W 10	$V_{IPP} = 1 V$	−55°C	.W.1	0.81	c01	
e D	Slow rate at unity goin	$R_L = 100 \Omega$,	DY.COMITY	125°C		0.38	Image Image Image	Mue
SK	Siew rate at unity gain	See Figure 1	NY.CUT	25°C	NN	0.56		v/µs
		WW.	VIPP = 5.5 V	-55°C	WW	0.73		DNr.
		W	100 r. OM.	125°C		0.35		OW.
Vn	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R _S = 20 Ω,	25°C	WW	32	00x.	nV/√Hz
	W. 1001. COM.		W.100 - COI	25°C	~1	35	Too	
Вом	Maximum output-swing bandwidth	$V_O = V_{OH}$	$C_L = 20 \text{ pF},$	-55°C	A.	50	1.100	kHz
		$K_{L} = 100 \text{ Ksz},$	See Figure 1	125°C	V	20	-110	Y.CO
	TWW.IOU CON		WW. LONG	25°C		635	V1	V.C
В ₁	Unity-gain bandwidth	$V_{I} = 10 \text{ mV},$	C _L = 20 pF,	-55°C		960	1.WV	kHz
		See Figure 5		125°C		440		100x.
	N.W.W. CON.C.	W	WWW AND	25°C	N	43°	VI.	1001
φm	Phase margin	$V_{I} = 10 \text{ mV},$	$f = B_1,$	55°C	N/	47°	NWV	
		$C_{L} = 20 \text{pr},$	See Figure 5	125°C		39°		N.100



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operating characteristics, V_{DD} = 5 V, T_A = 25°C

- 5	DADAMETED	ТЕСТ	CONDITIONS	TLC27M4Y	
OVr.	PARAMETER	IEST	CONDITIONS	MIN TYP MAX	
e D	Slow rote at upity opin	$R_L = 100 k\Omega$,	V _{IPP} = 1 V	0.43	\//uo
	Siew rate at unity gain	See Figure 1	V _{IPP} = 2.5 V	0.40	v/μs
Vn	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R _S = 20 Ω,	32	nV/√Hz
Вом	Maximum output-swing bandwidth	$V_{O} = V_{OH},$ $R_{L} = 100 \text{ k}\Omega,$	C _L = 20 pF, See Figure 1	55	kHz
B ₁	Unity-gain bandwidth	V _I = 10 mV, See Figure 3	C _L = 20 pF,	525	kHz
[¢] m	Phase margin	$V_{I} = 10 \text{ mV},$ $C_{I} = 20 \text{ pF},$	f = B ₁ , See Figure 3	40°	

operating characteristics, V_{DD} = 10 V, T_A = 25°C

WV.	DADAMETED	CONTERT	CONDITIONS	TL	_C27M4	Y	
	1001 TANAMETER	10	CONDITIONS	MIN	TYP	MAX	
CD	Slow sets at unity spin	$R_L = 100 k\Omega$	V _{IPP} = 1 V	V.1001	0.62	V.L.A	
SR	Siew rate at unity gain	CL = 20 pF, See Figure 1	VIPP = 5.5 V	N.100	0.56	M.T	v/μs
V _n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R _S = 20 Ω,	VW.10	32	ON.	nV/√Hz
Вом	Maximum output-swing bandwidth	$V_{O} = V_{OH},$ $R_{L} = 100 \text{ k}\Omega,$	C _L = 20 pF, See Figure 1	NWW.Y	35	COM	kHz
B ₁	Unity-gain bandwidth	V _I = 10 mV, See Figure 3	C _L = 20 pF,	ALW	635		kHz
[¢] m	Phase margin	V _I = 10 mV, C _L = 20 pF,	f = B ₁ , See Figure 3	WW	43°	N.C	DW.I

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PARAMETER MEASUREMENT INFORMATION

single-supply versus split-supply test circuits

Because the TLC27M4 and TLC27M9 are optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The use of either circuit gives the same result.







(b) SPLIT SUPPLY









Figure 2. Noise-Test Circuit











EXAS

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PARAMETER MEASUREMENT INFORMATION

input bias current

Because of the high input impedance of the TLC27M4 and TLC27M9 operational amplifiers, attempts to measure the input bias current can result in erroneous readings. The bias current at normal room ambient temperature is typically less than 1 pA, a value that is easily exceeded by leakages on the test socket. Two suggestions are offered to avoid erroneous measurements:

- 1. Isolate the device from other potential leakage sources. Use a grounded shield around and between the device inputs (see Figure 4). Leakages that would otherwise flow to the inputs are shunted away.
- 2. Compensate for the leakage of the test socket by actually performing an input bias current test (using a picoammeter) with no device in the test socket. The actual input bias current can then be calculated by subtracting the open-socket leakage readings from the readings obtained with a device in the test socket.

One word of caution—many automatic testers as well as some bench-top operational amplifier testers use the servo-loop technique with a resistor in series with the device input to measure the input bias current; the voltage drop across the series resistor is measured and the bias current is calculated. This method requires that a device be inserted into the test socket to obtain a correct reading; therefore, an open-socket reading is not feasible using this method.



Figure 4. Isolation Metal Around Device Inputs (J and N packages)

low-level output voltage

To obtain low-supply-voltage operation, some compromise was necessary in the input stage. This compromise results in the device low-level output being dependent on both the common-mode input voltage level as well as the differential input voltage level. When attempting to correlate low-level output readings with those quoted in the electrical specifications, these two conditions should be observed. If conditions other than these are to be used, please refer to Figures 14 through 19 in the *Typical Characteristics* of this data sheet.



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PARAMETER MEASUREMENT INFORMATION

input offset voltage temperature coefficient

Erroneous readings often result from attempts to measure temperature coefficient of input offset voltage. This parameter is actually a calculation using input offset voltage measurements obtained at two different temperatures. When one (or both) of the temperatures is below freezing, moisture can collect on both the device and the test socket. This moisture results in leakage and contact resistance, which can cause erroneous input offset voltage readings. The isolation techniques previously mentioned have no effect on the leakage since the moisture also covers the isolation metal itself, thereby rendering it useless. It is suggested that these measurements be performed at temperatures above freezing to minimize error.

full-power response

Full-power response, the frequency above which the operational amplifier slew rate limits the output voltage swing, is often specified two ways: full-linear response and full-peak response. The full-linear response is generally measured by monitoring the distortion level of the output, while increasing the frequency of a sinusoidal input signal until the maximum frequency is found above which the output contains significant distortion. The full-peak response is defined as the maximum output frequency, without regard to distortion, above which full peak-to-peak output swing cannot be maintained.

Because there is no industry-wide accepted value for significant distortion, the full-peak response is specified in this data sheet and is measured using the circuit of Figure 1. The initial setup involves the use of a sinusoidal input to determine the maximum peak-to-peak output of the device (the amplitude of the sinusoidal wave is increased until clipping occurs). The sinusoidal wave is then replaced with a square wave of the same amplitude. The frequency is then increased until the maximum peak-to-peak output can no longer be maintained (Figure 5). A square wave is used to allow a more accurate determination of the point at which the maximum peak-to-peak output is reached.



Figure 5. Full-Power-Response Output Signal

(d) f > B_{OM}

test time

Inadequate test time is a frequent problem, especially when testing CMOS devices in a high-volume, short-test-time environment. Internal capacitances are inherently higher in CMOS than in bipolar and BiFET devices and require longer test times than their bipolar and BiFET counterparts. The problem becomes more pronounced with reduced supply levels and lower temperatures.

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TYPICAL CHARACTERISTICS

[WWW.L. COMP.	TY ON YOUNG	FIGURE
VIO	Input offset voltage	Distribution	6, 7
ανιο	Temperature coefficient of input offset voltage	Distribution	8, 9
VOH	High-level output voltage	vs High-level output current vs Supply voltage vs Free-air temperature	10, 11 12 13
VOL	Low-level output voltage	vs Common-mode input voltage vs Differential input voltage vs Free-air temperature vs Low-level output current	14, 15 16 17 18, 19
AVD	Differential voltage amplification	vs Supply voltage vs Free-air temperature vs Frequency	20 21 32, 33
IB	Input bias current	vs Free-air temperature	22
IIO	Input offset current	vs Free-air temperature	22
VIC	Common-mode input voltage	vs Supply voltage	23
IDD CO	Supply current	vs Supply voltage vs Free-air temperature	24 25
SR	Slew rate	vs Supply voltage vs Free-air temperature	26 27
100 x.	Normalized slew rate	vs Free-air temperature	28
VO(PP)	Maximum peak-to-peak output voltage	vs Frequency	29
B ₁	Unity-gain bandwidth	vs Free-air temperature vs Supply voltage	30 31
N 10	Phase shift	vs Frequency	32, 33
φm	Phase margin	vs Supply voltage vs Free-air temperature vs Load capacitance	34 35 36
Vn	Equivalent input noise voltage	vs Frequency	37

Table of Graphs

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TYPICAL CHARACTERISTICS

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TYPICAL CHARACTERISTICS[†]

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[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.



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TYPICAL CHARACTERISTICS





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APPLICATION INFORMATION

single-supply operation

While the TLC27M4 and TLC27M9 perform well using dual power supplies (also called balanced or split supplies), the design is optimized for single-supply operation. This design includes an input common-mode voltage range that encompasses ground as well as an output voltage range that pulls down to ground. The supply voltage range extends down to 3 V (C-suffix types), thus allowing operation with supply levels commonly available for TTL and HCMOS; however, for maximum dynamic range, 16-V single-supply operation is recommended.

Many single-supply applications require that a voltage be applied to one input to establish a reference level that is above ground. A resistive voltage divider is usually sufficient to establish this reference level (see Figure 38). The low input bias current of the TLC27M4 and TLC27M9 permits the use of very large resistive values to implement the voltage divider, thus minimizing power consumption.

The TLC27M4 and TLC27M9 work well in conjunction with digital logic; however, when powering both linear devices and digital logic from the same power supply, the following precautions are recommended:

- 1. Power the linear devices from separate bypassed supply lines (see Figure 39); otherwise, the linear device supply rails can fluctuate due to voltage drops caused by high switching currents in the digital logic.
- 2. Use proper bypass techniques to reduce the probability of noise-induced errors. Single capacitive decoupling is often adequate; however, high-frequency applications may require RC decoupling.



 $V_{REF} = V_{DD} \frac{R3}{R1 + R3}$ $V_{O} = (V_{REF} - V_{I}) \frac{R4}{R2} + V_{REF}$

Figure 38. Inverting Amplifier With Voltage Reference



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(b) SEPARATE BYPASSED SUPPLY RAILS (preferred)

Figure 39. Common Versus Separate Supply Rails

input characteristics

The TLC27M4 and TLC27M9 are specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction. Exceeding this specified range is a common problem, especially in single-supply operation. Note that the lower range limit includes the negative rail, while the upper range limit is specified at $V_{DD} - 1$ V at $T_A = 25^{\circ}$ C and at $V_{DD} - 1.5$ V at all other temperatures.

The use of the polysilicon-gate process and the careful input circuit design gives the TLC27M4 and TLC27M9 very good input offset voltage drift characteristics relative to conventional metal-gate processes. Offset voltage drift in CMOS devices is highly influenced by threshold voltage shifts caused by polarization of the phosphorus dopant implanted in the oxide. Placing the phosphorus dopant in a conductor (such as a polysilicon gate) alleviates the polarization problem, thus reducing threshold voltage shifts by more than an order of magnitude. The offset voltage drift with time has been calculated to be typically 0.1 μ V/month, including the first month of operation.

Because of the extremely high input impedance and resulting low bias current requirements, the TLC27M4 and TLC27M9 are well suited for low-level signal processing; however, leakage currents on printed-circuit boards and sockets can easily exceed bias current requirements and cause a degradation in device performance. It is good practice to include guard rings around inputs (similar to those of Figure 4 in the *Parameter Measurement Information* section). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input (see Figure 40).

Unused amplifiers should be connected as unity-gain followers to avoid possible oscillation.

noise performance

The noise specifications in operational amplifier circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias current requirements of the TLC27M4 and TLC27M9 result in a very low noise current, which is insignificant in most applications. This feature makes the devices especially favorable over bipolar devices when using values of circuit impedance greater than 50 k Ω , since bipolar devices exhibit greater noise currents.





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APPLICATION INFORMATION







(a) NONINVERTING AMPLIFIER

(b) INVERTING AMPLIFIER Figure 40. Guard-Ring Schemes (c) UNITY-GAIN AMPLIFIER

output characteristics

The output stage of the TLC27M4 and TLC27M9 is designed to sink and source relatively high amounts of current (see *typical characteristics*). If the output is subjected to a short-circuit condition, this high current capability can cause device damage under certain conditions. Output current capability increases with supply voltage.

All operating characteristics of the TLC27M4 and TLC27M9 were measured using a 20-pF load. The devices drive higher capacitive loads; however, as output load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation (see Figure 41). In many cases, adding a small amount of resistance in series with the load capacitance alleviates the problem.



(a) $C_L = 20 \text{ pF}$, $R_L = \text{NO LOAD}$



(b) $C_L = 170 \text{ pF}$, $R_L = \text{NO LOAD}$



(c) $C_L = 190 \text{ pF}$, $R_L = \text{NO LOAD}$





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APPLICATION INFORMATION

output characteristics (continued)

Although the TLC27M4 and TLC27M9 possess excellent high-level output voltage and current capability, methods for boosting this capability are available, if needed. The simplest method involves the use of a pullup resistor (R_P) connected from the output to the positive supply rail (see Figure 42). There are two disadvantages to the use of this circuit. First, the NMOS pulldown transistor N4 (see equivalent schematic) must sink a comparatively large amount of current. In this circuit, N4 behaves like a linear resistor with an on-resistance between approximately 60 Ω and 180 Ω , depending on how hard the operational amplifier input is driven. With very low values of R_P , a voltage offset from 0 V at the output occurs. Second, pullup resistor R_P acts as a drain load to N4 and the gain of the operational amplifier is reduced at output voltage levels where N5 is not supplying the output current.



to Increase V_{OH}



feedback

Operational amplifier circuits nearly always employ feedback, and since feedback is the first prerequisite for oscillation, some caution is appropriate. Most oscillation problems result from driving capacitive loads (discussed previously) and ignoring stray input capacitance. A small-value capacitor connected in parallel with the feedback resistor is an effective remedy (see Figure 43). The value of this capacitor is optimized empirically.

electrostatic discharge protection

The TLC27M4 and TLC27M9 incorporate an internal electrostatic discharge (ESD) protection circuit that prevents functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2. Care should be exercised, however, when handling these devices, as exposure to ESD may result in the degradation of the device parametric performance. The protection circuit also causes the input bias currents to be temperature-dependent and have the characteristics of a reverse-biased diode.

latch-up

Because CMOS devices are susceptible to latch-up due to their inherent parasitic thyristors, the TLC27M4 and TLC27M9 inputs and outputs were designed to withstand –100-mA surge currents without sustaining latch-up; however, techniques should be used to reduce the chance of latch-up whenever possible. Internal protection diodes should not, by design, be forward biased. Applied input and output voltage should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 μ F typical) located across the supply rails as close to the device as possible.



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APPLICATION INFORMATION

latch-up (continued)

The current path established if latch-up occurs is usually between the positive supply rail and ground; it can be triggered by surges on the supply lines and/or voltages on either the output or inputs that exceed the supply voltage. Once latch-up occurs, the current flow is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor and usually results in the destruction of the device. The chance of latch-up occurring increases with increasing temperature and supply voltages.



Figure 45. Precision Low-Current Sink



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 $V_{\text{REF}} = 0 \text{ V to } V_{\text{DD}} - 2 \text{ V}$

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Figure 47. Photo-Diode Amplifier With Ambient Light Rejection

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