- Push-Pull CMOS Output Drives Capacitive Loads Without Pullup Resistor, I<sub>O</sub> = ± 8 mA
- Very Low Power . . . 100 μW Typ at 5 V
- Fast Response Time . . . t<sub>PLH</sub> = 2.7 μs Typ With 5-mV Overdrive
- Single-Supply Operation ... 3 V to 16 V TLC3702M ... 4 V to 16 V
- On-Chip ESD Protection

#### description

The TLC3702 consists of two independent micropower voltage comparators designed to operate from a single supply and be compatible with modern HCMOS logic systems. They are functionally similar to the LM339 but use onetwentieth of the power for similar response times. The push-pull CMOS output stage drives capacitive loads directly without a powerconsuming pullup resistor to achieve the stated response time. Eliminating the pullup resistor not only reduces power dissipation, but also saves board space and component cost. The output stage is also fully compatible with TTL requirements.

Texas Instruments LinCMOS<sup>™</sup> process offers superior analog performance to standard CMOS processes. Along with the standard CMOS advantages of low power without sacrificing speed, high input impedance, and low bias currents, the LinCMOS<sup>™</sup> process offers extremely stable input offset voltages with large differential input voltages. This characteristic makes it possible to build reliable CMOS comparators.



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NC - No internal connection

#### symbol (each comparator)



The TLC3702C is characterized for operation over the commercial temperature range of 0°C to 70°C. The TLC3702I is characterized for operation over the extended industrial temperature range of –40°C to 85°C. The TLC3702M is characterized for operation over the full military temperature range of –55°C to 125°C.

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AVAILABLE OPTIONS								
WWW	N. C. Mark	W	PACK	AGES				
TA	at 25°C	SMALL OUTLINE (D)	CERAMIC (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)			
0°C to 70°C	5 mV	TLC3702CD	ATW .	100X.00	TLC3702CP			
–40°C to 85°C	5 mV	TLC3702ID	-WWW	N.COM	TLC3702IP			
–55°C to 125°C	5 mV	TLC3702MD	TLC3702MFK	TLC3702MJG				

The D package is available taped and reeled. Add R suffix to the device type (e.g., TLC3702CDR).

# WW.100Y functional block diagram (each comparator)



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{DD}$ (see Note	1)	–0.3 V to 18 V
Differential input voltage, VID (see No	te 2)	±18 V
Input voltage range, V <sub>1</sub>		–0.3 V to V <sub>DD</sub>
Output voltage range, Vo		– 0.3 V to V <sub>D</sub>
Input current, I <sub>1</sub>		±5 mA
Output current, In (each output)		±20 mA
Total supply current into VDD		40 mA
Total current out of GND		40 mA
Continuous total power dissipation .		See Dissipation Rating Table
Operating free-air temperature range,	T <sub>A</sub> : TLC3702C	0°C to 70°C
WWW.LOWCOMIC W	TLC3702I	–40°C to 85°C
	TLC3702M	–55°C to 125°C
Storage temperature range		–65°C to 150°C
Case temperature for 60 seconds: FK	package	
Lead temperature 1,6 mm (1/16 inch)	from case for 10 seconds: D or P package	e 260°C
Lead temperature 1,6 mm (1/16 inch)	from case for 60 seconds: JG package	

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.

2. Differential voltages are at IN+ with respect to IN-.



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			DISSIPATION	RATING TABLE		
PA	CKAGE	T <sub>A</sub> ≤ 25°C POWER RATING	DERATING FACTOR ABOVE T <sub>A</sub> = 25°C	T <sub>A</sub> = 70°C POWER RATING	T <sub>A</sub> = 85°C POWER RATING	T <sub>A</sub> = 125°C POWER RATING
N	D	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
W	FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
-	JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
7.1	Р	1000 mW	8.0 mW/°C	640 mW	520 mW	N/A

# WW.100Y.CO

COM WWWWWWWWWWWWW			TLC370	)2C
CONT AN ALWAY CONTAIN	You WWW	MIN	NOM	MAX
Supply voltage, VDD	WW.Ioo	CO3	5	16
Common-mode input voltage, VIC	VY 100	- 0.2	V.L	V <sub>DD</sub> - 1
High-level output current, I <sub>OH</sub>	WW 100	JY.C	TIM	-20
Low-level output current, IOL	WWW.	V.C.	1	20
Operating free-air temperature, TA	I.WW.	0	O <sub>N</sub> r.	70

#### electrical characteristics at specified operating free-air temperature, V<sub>DD</sub> = 5 V (unless otherwise noted) WWW.L.

DADAMETED				TLC3702C				
	PARAMETER	TEST CONDITIONS	IA	MIN	TYP	MAX	UNI	
	100X.001.TW WY	$V_{DD} = 5 V \text{ to } 10 V,$	25°C	W.1001	1.2	5		
VIO	Input offset voltage	VIC = VICRmin, See Note 3	0°C to 70°C	N 1. 100		6.5	٣V	
NW	NT NT V	N OF N	25°C	W 10	1	M	рA	
10	Input offset current	VIC = 2.5 V	70°C	WW	NY.C	0.3	nA	
	Reput him automat		25°C	WWW.L	5	COM	pА	
IB	input bias current	vIC = 2.5 v	70°C	WIG	Ino .	0.6	nA	
		NW 100Y.C	25°C	0 to V <sub>DD</sub> – 1	1007			
ICR	Common-mode input voltage range	WWW.Looy.C	0°C to 70°C	0 to V <sub>DD</sub> – 1.5	100	Y.Co	] v	
	W.IVO CON.	WW.Los	25°C	WW	84	N.C	) MAR	
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}min$	70°C		84		dB	
			0°C		84	001.		
	WWW.PON.COM	WWW. OO	25°C	W W	85	Yoor		
SVR	Supply-voltage rejection ratio	$V_{DD} = 5 V \text{ to } 10 V$	70°C		85		dB	
		W 10	0°C		85	1.100		
	The State of the	VID = 1 V,	25°C	4.5	4.7	N 10		
∨ОН	Hign-level output voltage	$I_{OH} = -4 \text{ mA}$	70°C	4.3	AN.	-10	v	
	N.I. COM.	$V_{ID} = -1 V_{1}$	25°C	N/	210	300	~~~	
VOL	Low-level output voltage	$I_{OH} = 4 \text{ mA}$	70°C	M.L		375	mv	
	Currently assessed (h ath assessment)	Outputs law. No load	25°C	M.T.M.	18	40	100	
DD	Supply current (both comparators)	Outputs low, INO IOad	0°C to 70°C	WT .	1	50	ο μΑ	



#### recommended operating conditions

recommended operating conditions						
TW WWWWW 100Y.CO. MTW WWW 100Y.CO.M.T	WI.IW	TLC3702I				
ONLY WWW.LOOV.COME TW WWW.LOOY.	MIN	NOM	MAX	UNIT		
Supply voltage, V <sub>DD</sub>	3	5	16	V		
Common-mode input voltage, V <sub>IC</sub>	-0.2		V <sub>DD</sub> – 1.5	V		
High-level output current, I <sub>OH</sub>	M	L.A.	-20	mA		
Low-level output current, I <sub>OL</sub>	NY.	WT	20	mA		
Operating free-air temperature, T <sub>A</sub>	-40	W	85	°C		

# electrical characteristics at specified operating free-air temperature, V<sub>DD</sub> = 5 V (unless otherwise noted)

DADAMETED		Trategorie	ALL	TLC3702I			118117	
	PARAMETER	TEST CONDITIONS	'A	MIN	TYP	MAX	UNIT	
		$V_{DD} = 5 V \text{ to } 10 V,$	25°C	100×.	1.2	5		
VIO	Input onset voltage	$V_{IC} = V_{ICR}$ min, See Note 3	-40°C to 85°C	ANY.C		7	mv	
1. N.L	loguit offect ourrent	Via 2EV	25°C	. I and	01	W	pА	
O	input onset current	VIC = 2.5 V	85°C	W.100 -	coM	1	nA	
M	W WT	Yes 0.5.Y	25°C	-1100X	5	V.T.V	pА	
IΒ	input bias current	VIC = 2.5 V	85°C	100	Y.C.	2	nA	
NW	N.100 COM.	WWW.100 COM.	N 25°C 🔨	0 to V <sub>DD</sub> – 1	oy.cc	OM.I	N	
VICR	Common-mode input voitage range	ommon-mode input voltage range		0 to V <sub>DD</sub> – 1.5	007.0	COM		
N	TIME TOOL	W 1001. ON	25°C	N.	84	c01	dB	
CMRR	R Common-mode rejection ratio VIC = VICRmin	VIC = VICRmin	85°C	N.	84			
		WWW.ICO.CO.	–40°C	WWY	83	N.CU		
	W.IOU.COM.	NW.IVO TCO	25°C	WIG	85	N.C	Diar.	
ksvr	Supply-voltage rejection ratio	$V_{DD} = 5 V$ to 10 V	85°C		85		dB	
	WWW. OOY.COM TW	WWW INOY.C	-40°C	N.	83	001.		
			25°C	4.5	4.7	1001		
∨ОН	High-level output voltage	$v_{\text{ID}} = 1 v$ , $i_{\text{OH}} = -4 \text{ mA}$	85°C	4.3	WW	.10		
V	Low lovel output veltore		25°C	-	210	300		
VOL	Low-level output voltage	$V_{\text{ID}} = -1$ V, $I_{\text{OH}} = -4$ mA	85°C	N	$M_{II}$	400	mv	
	Supply surrent (both componetors)	Quitauta laur. Na laad	25°C	N	18	40		
DD	Supply current (both comparators)	Outputs low, No load	-40°C to 85°C			65	μΑ	

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#### recommended operating conditions

TW WWW. 100Y.CO.M.TW	WW 1001. ON.T		TLC370	)2M	LINUT
		MIN	NOM	MAX	
Supply voltage, V <sub>DD</sub>	MMM.L. COM.	4	5	16	V
Common-mode input voltage, VIC	N. 100 L COM	0		V <sub>DD</sub> – 1.5	V
High-level output current, I <sub>OH</sub>	W	T.T.M.		- 20	mA
Low-level output current, IOL	WW TOOX.CO.	VT .		20	mA
Operating free-air temperature, T <sub>A</sub>	WWW.LCC	- 55	N	125	°C
WILL WITH TOP ONLY	N.IOO	ON.	~1		

# electrical characteristics at specified operating free-air temperature, V<sub>DD</sub> = 5 V (unless otherwise noted)

ST C	DADAMETED	CON-	NWW.	TLC	3702M		LINUT
01	PARAMETER	TEST CONDITIONS	IA.	MIN	ТҮР	MAX	UNIT
001.		V <sub>DD</sub> = 5 V to 10 V,	25°C	Mon	1.2	5	
VIO	input offset voltage	$V_{IC} = V_{ICR}$ min, See Note 3	–55°C to 125°C	DY.	NT.	10	mv
100		Via - 25 V	25°C	NY.CUT	1		pА
10	input onset current	V C = 2.5 V	125°C	CO IN	Dr.	15	nA
-110	N. M.		25°C	100	5		pА
ΊΒ	Input bias current	$V_{1C} = 2.5 V$	125°C	100Y.	A	30	nA
NN.1	100X.COM.TW WY	W.100Y.COM.TW	25°C	0 to V <sub>DD</sub> – 1	COM	TW	N/
VICR	Common-mode input voltage range	WW.100Y.COM.TW	–55°C to 125°C	0 to V <sub>DD</sub> – 1.5	v.col	1.1	v
	N.1001. CONT.I.	NN.100 COM.	25°C	WW.IOO	84	Wr.	-
CMRR	Common-mode rejection ratio	VIC = VICRmin	125°C	10	83	M.	dB
WW		WWW. ADDY.COM	_55°C		82	140	NT N
-1	NW.100 J CONT.	ALWN.10 N.COM	25°C	WWW.	85	CORT	Wn
<b>k</b> SVR	Supply-voltage rejection ratio	V <sub>DD</sub> = 5 V to 10 V	125°C	WW.	85	CON	dB
V		WW 100Y.CC	– 55°C	N.	82		1.1
	NT NO.YOUTH	WWWWWWWWW	25°C	4.5	4.7	Y	TIM
⊻он	High-level output voltage	$V_{ID} = 1 V$ , $I_{OH} = -4 mA$	125°C	4.2	NN	N.C	V
.,	Way 100 TONIT	.100	25°C		210	300	ON.
VOL	Low-level output voltage	VID = -1 V, $IOH = -4 mA$	125°C	111		500	mv
	NWWW. COMMIN		25°C	1	18	40	
'DD	Supply current (both comparators)	Outputs low, No load	-55°C to 125°C	1	JAN W	90	μΑ

<sup>†</sup> All characteristics are measured with zero common-mode voltage unless otherwise noted.

NOTE 3. The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V. 勝 掛 カ お や or o



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# switching characteristics, V<sub>DD</sub> = 5 V, T<sub>A</sub> = 25°C

oM.	PARAMETER	TES	TEST CONDITIONS			TLC3702C, TLC3702I TLC3702M			
						MAX			
	TW WW 100Y. M.T	14 14	Overdrive = 2 mV	41.1	4.5				
		7	Overdrive = 5 mV	WT.I.	2.7				
PLH	Propagation delay time, low-to-high-level output <sup>†</sup>	f = 10  kHz,	Overdrive = 10 mV	1	1.9		μs		
		0 <u></u> = 50 pr	Overdrive = 20 mV	OM.	1.4				
		01.000	Overdrive = 40 mV	- Mo	1.1				
N.	COMMAN WWWWWW	V <sub>I</sub> = 1.4 V ste	ep at IN+		1.1				
	Propagation delay time, high-to-low-level output <sup>†</sup> $f = 10 \text{ kHz}$	MI.TW	Overdrive = 2 mV	COr-	4				
			Overdrive = 5 mV	1 CON	2.3	1	μs		
PHD		f = 10  kHz,	Overdrive = 10 mV		1.5				
		CL = 50 pr	Overdrive = 20 mV	NOY.C	0.95	N			
		CONT.	Overdrive = 40 mV	J.V	0.65	W			
		V <sub>I</sub> = 1.4 V ste	ep at IN+	100	0.15				
EN VI	Fall time	f = 10 kHz, C <sub>L</sub> = 50 pF	Overdrive = 50 mV	1100 1.	50		ns		
	Rise time	f = 10  kHz, $C_1 = 50 \text{ pF}$	Overdrive = 50 mV	100	125	M.T	N ns		

<sup>†</sup> Simultaneous switching of inputs causes degradation in output response. WWW.100Y.COM.TW WWW.100Y.C

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## PRINCIPLES OF OPERATION

#### LinCMOS<sup>™</sup> process

The LinCMOS<sup>™</sup> process is a linear polysilicon-gate CMOS process. Primarily designed for single-supply applications, LinCMOS<sup>™</sup> products facilitate the design of a wide range of high-performance analog functions from operational amplifiers to complex mixed-mode converters.

While digital designers are experienced with CMOS, MOS technologies are relatively new for analog designers. This short guide is intended to answer the most frequently asked questions related to the quality and reliability of LinCMOS<sup>™</sup> products. Further questions should be directed to the nearest TI field sales office.

#### electrostatic discharge

CMOS circuits are prone to gate oxide breakdown when exposed to high voltages even if the exposure is only for very short periods of time. Electrostatic discharge (ESD) is one of the most common causes of damage to CMOS devices. It can occur when a device is handled without proper consideration for environmental electrostatic charges, e.g., during board assembly. If a circuit in which one amplifier from a dual op amp is being used and the unused pins are left open, high voltages tend to develop. If there is no provision for ESD protection, these voltages may eventually punch through the gate oxide and cause the device to fail. To prevent voltage buildup, each pin is protected by internal circuitry.

Standard ESD-protection circuits safely shunt the ESD current by providing a mechanism whereby one or more transistors break down at voltages higher than the normal operating voltages but lower than the breakdown voltage of the input gate. This type of protection scheme is limited by leakage currents which flow through the shunting transistors during normal operation after an ESD voltage has occurred. Although these currents are small, on the order of tens of nanoamps, CMOS amplifiers are often specified to draw input currents as low as tens of picoamps.

To overcome this limitation, TI design engineers developed the patented ESD-protection circuit shown in Figure 1. This circuit can withstand several successive 2-kV ESD pulses, while reducing or eliminating leakage currents that may be drawn through the input pins. A more detailed discussion of the operation of the TI ESD-protection circuit is presented on the next page.

All input and output pins on LinCMOS<sup>™</sup> and Advanced LinCMOS<sup>™</sup> products have associated ESD-protection circuitry that undergoes qualification testing to withstand 2000 V discharged from a 100-pF capacitor through a 1500-Ω resistor (human body model) and 200 V from a 100-pF capacitor with no current-limiting resistor (charged device model). These tests simulate both operator and machine handling of devices during normal test and assembly operations.



Figure 1. LinCMOS<sup>™</sup> ESD-Protection Schematic

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# PRINCIPLES OF OPERATION

#### input protection circuit operation

Texas Instruments patented protection circuitry allows for both positive- and negative-going ESD transients. These transients are characterized by extremely fast rise times and usually low energies, and can occur both when the device has all pins open and when it is installed in a circuit.

#### positive ESD transients

Initial positive charged energy is shunted through Q1 to V<sub>SS</sub>. Q1 turns on when the voltage at the input rises above the voltage on the V<sub>DD</sub> pin by a value equal to the V<sub>BE</sub> of Q1. The base current increases through R2 with input current as Q1 saturates. The base current through R2 forces the voltage at the drain and gate of Q2 to exceed its threshold level (V<sub>T</sub> ~ 22 to 26 V) and turn Q2 on. The shunted input current through Q1 to V<sub>SS</sub> is now shunted through the n-channel enhancement-type MOSFET Q2 to V<sub>SS</sub>. If the voltage on the input pin continues to rise, the breakdown voltage of the zener diode D3 is exceeded and all remaining energy is dissipated in R1 and D3. The breakdown voltage of D3 is designed to be 24 V to 27 V, which is well below the gate-oxide voltage of the circuit to be protected.

#### negative ESD transients

The negative charged ESD transients are shunted directly through D1. Additional energy is dissipated in R1 and D2 as D2 becomes forward biased. The voltage seen by the protected circuit is -0.3 V to -1 V (the forward voltage of D1 and D2).

#### circuit-design considerations

LinCMOS<sup>™</sup> products are being used in actual circuit environments that have input voltages that exceed the recommended common-mode input voltage range and activate the input protection circuit. Even under normal operation, these conditions occur during circuit power up or power down, and in many cases, when the device is being used for a signal conditioning function. The input voltages can exceed V<sub>ICR</sub> and not damage the device only if the inputs are current limited. The recommended current limit shown on most product data sheets is ±5 mA. Figure 2 and Figure 3 show typical characteristics for input voltage versus input current.

Normal operation and correct output state can be expected even when the input voltage exceeds the positive supply voltage. Again, the input current should be externally limited even though internal positive current limiting is achieved in the input protection circuit by the action of Q1. When Q1 is on, it saturates and limits the current to approximately 5-mA collector current by design. When saturated, Q1 base current increases with input current. This base current is forced into the V<sub>DD</sub> pin and into the device I<sub>DD</sub> or the V<sub>DD</sub> supply through R2 producing the current limiting effects shown in Figure 2. This internal limiting lasts only as long as the input voltage is below the V<sub>T</sub> of Q2.

When the input voltage exceeds the negative supply voltage, normal operation is affected and output voltage states may not be correct. Also, the isolation between channels of multiple devices (duals and quads) can be severely affected. External current limiting must be used since this current is directly shunted by D1 and D2 and no internal limiting is achieved. If normal output voltage states are required, an external input voltage clamp is required (see Figure 4).



**PRINCIPLES OF OPERATION** 



NOTE A: If the correct input state is required when the negative input exceeds GND, a Schottky clamp is required. Figure 4. Typical Input Current-Limiting Configuration for a LinCMOS<sup>™</sup> Comparator

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# PARAMETER MEASUREMENT INFORMATION

The TLC3702 contains a digital output stage which, if held in the linear region of the transfer curve, can cause damage to the device. Conventional operational amplifier/comparator testing incorporates the use of a servo loop which is designed to force the device output to a level within this linear region. Since the servo-loop method of testing cannot be used, we offer the following alternatives for measuring parameters such as input offset voltage, common-mode rejection, etc.

To verify that the input offset voltage falls within the limits specified, the limit value is applied to the input as shown in Figure 5(a). With the noninverting input positive with respect to the inverting input, the output should be high. With the input polarity reversed, the output should be low.

A similar test can be made to verify the input offset voltage at the common-mode extremes. The supply voltages can be slewed to provide greater accuracy, as shown in Figure 5(b) for the  $V_{ICR}$  test. This slewing is done instead of changing the input voltages.

A close approximation of the input offset voltage can be obtained by using a binary search method to vary the differential input voltage while monitoring the output state. When the applied input voltage differential is equal, but opposite in polarity, to the input offset voltage, the output changes states.

Figure 6 illustrates a practical circuit for direct dc measurement of input offset voltage that does not bias the comparator in the linear region. The circuit consists of a switching mode servo loop in which IC1a generates a triangular waveform of approximately 20-mV amplitude. IC1b acts as a buffer, with C2 and R4 removing any residual dc offset. The signal is then applied to the inverting input of the comparator under test, while the noninverting input is driven by the output of the integrator formed by IC1c through the voltage divider formed by R8 and R9. The loop reaches a stable operating point when the output of the comparator under test has a duty cycle of exactly 50%, which can only occur when the incoming triangle wave is sliced symmetrically or when the voltage at the noninverting input exactly equals the input offset voltage.

Voltage dividers R8 and R9 provide an increase in input offset voltage by a factor of 100 to make measurement easier. The values of R5, R7, R8, and R9 can significantly influence the accuracy of the reading; therefore, it is suggested that their tolerance level be one percent or lower.

Measuring the extremely low values of input current requires isolation from all other sources of leakage current and compensation for the leakage of the test socket and board. With a good picoammeter, the socket and board leakage can be measured with no device in the socket. Subsequently, this open socket leakage value can be subtracted from the measurement obtained with a device in the socket to obtain the actual input current of the device.





(a)  $V_{IO}$  WITH  $V_{IC} = 0$  V

(b)  $V_{IO}$  WITH  $V_{IC} = 4 V$ 

Figure 5. Method for Verifying That Input Offset Voltage Is Within Specified Limits

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#### PARAMETER MEASUREMENT INFORMATION



Response time is defined as the interval between the application of an input step function and the instant when the output reaches 50% of its maximum value. Response time for the low-to-high-level output is measured from the leading edge of the input pulse, while response time for the high-to-low-level output is measured from the trailing edge of the input pulse. Response time measurement at low input signal levels can be greatly affected by the input offset voltage. The offset voltage should be balanced by the adjustment at the inverting input as shown in Figure 7, so that the circuit is just at the transition point. A low signal, for example 105-mV or 5-mV overdrive, causes the output to change state.



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# PARAMETER MEASUREMENT INFORMATION

NOTE A: CL includes probe and jig capacitance.

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Figure 7. Response, Rise, and Fall Times Circuit and Voltage Waveforms

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# **TYPICAL CHARACTERISTICS<sup>†</sup>**

	CONT.	WW.LUC COM.	FIG
VIO	Input offset voltage	Distribution	8
IB	Input bias current	vs Free-air temperature	
CMRR	Common-mode rejection ratio	vs Free-air temperature	1
<b>k</b> SVR	Supply-voltage rejection ratio	vs Free-air temperature	1
VOH	High-level output current	vs Free-air temperature vs High-level output current	1
VOL	Low-level output voltage	vs Low-level output current vs Free-air temperature	1
tt	Transition time	vs Load capacitance	1
COR	Supply current response	vs Time	1
100 L	Low-to-high-level output response	Low-to-high level output propagation delay time	1
	High-to-low level output response	High-to-low level output propagation delay time	1
<sup>t</sup> PLH	Low-to-high level output propagation delay time	vs Supply voltage	2
<sup>t</sup> PHL	High-to-low level output propagation delay time	vs Supply voltage	2
IDD	Supply current	vs Frequency vs Supply voltage vs Free-air temperature	2222

#### **Table of Graphs**



**DISTRIBUTION OF INPUT** 

#### **INPUT BIAS CURRENT** VS FREE-AIR TEMPERATURE







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**COMMON-MODE REJECTION RATIO** 

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# TYPICAL CHARACTERISTICS<sup>†</sup>







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# TLC3702 DUAL MICROPOWER LinCMOS™ VOLTAGE COMPARATORS

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**TYPICAL CHARACTERISTICS<sup>†</sup>** 









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# TYPICAL CHARACTERISTICS







#### TYPICAL CHARACTERISTICS<sup>†</sup>



# **APPLICATION INFORMATION**

The inputs should always remain within the supply rails in order to avoid forward biasing the diodes in the electrostatic discharge (ESD) protection structure. If either input exceeds this range, the device is not damaged as long as the input is limited to less than 5 mA. To maintain the expected output state, the inputs must remain within the common-mode range. For example, at 25°C with  $V_{DD} = 5$  V, both inputs must remain between -0.2 V and 4 V to ensure proper device operation.

To ensure reliable operation, the supply should be decoupled with a capacitor  $(0.1 \,\mu\text{F})$  that is positioned as close to the device as possible.

The TLC3702 has internal ESD-protection circuits that prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parametric performance.

W TAN 100X. CONFILM	FIGURE
Pulse-width-modulated motor speed controller	25
Enhanced supply supervisor	26
Two-phase nonoverlapping clock generator	27
Micropower switching regulator	28

Table of Applications



#### NOTES: A. The recommended minimum capacitance is 10 μF to eliminate common ground switching noise. B. Adjust C1 for change in oscillator frequency.

# Figure 25. Pulse-Width-Modulated Motor Speed Controller



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Figure 26. Enhanced Supply Supervisor

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- NOTES: A. Adjust C1 for a change in oscillator frequency where:  $1/f = 1.85(100 \text{ k}\Omega)\text{C1}$ 
  - B. Adjust R1 and R3 to change duty cycle
  - C. Adjust R2 to change deadtime

Figure 27. Two-Phase Nonoverlapping Clock Generator



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**APPLICATION INFORMATION** 

- NOTES: A. Adjust C1 for a change in oscillator frequency
  - B. TLC271 Tie pin 8 to pin 7 for low bias operation

WWW.100

- C. SK9504 VDS = 40 V
  - IDS = 1 A
- D. To achieve microampere current drive, the inductance of the circuit must be increased.

Figure 28. Micropower Switching Regulator



XAS

**MECHANICAL DATA** 

#### D (R-PDSO-G\*\*)

#### PLASTIC SMALL-OUTLINE PACKAGE

#### **14 PIN SHOWN**



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-012



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**MECHANICAL DATA** 

#### LEADLESS CERAMIC CHIP CARRIER

FK (S-CQCC-N\*\*) 28 TERMINAL SHOWN



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. The terminals are gold plated.
- E. Falls within JEDEC MS-004



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#### JG (R-GDIP-T8)

#### MECHANICAL DATA

**CERAMIC DUAL-IN-LINE PACKAGE** 



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

WWW.100Y.C

- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL-STD-1835 GDIP1-T8



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- NOTES: A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.

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C. Falls within JEDEC MS-001



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