TMS 9914 GENERAL PURPOSE INTERFACE BUS ADAPTER

990/9900 FAMILY MICROCOMPUTER COMPONENTS

- IEEE Std. 488-1975 Compatible
- Source and Acceptor Handshake
- Complete Talker and Listener Functions with Extended Addressing
- Controller and System Controller Capability
- Service Request
- Remote and Local with Lockout
- Serial and Parallel Polling
- Device Clear
- Device Trigger
- Compatible with TMS 9911 DMA Controller
- Single +5 V Power Supply
- Interfaces directly to SN75160/1/2 Transceivers

DESCRIPTION

The TMS 9914 General Purpose Interface Bus Adapter is a microprocessor controlled versatile device which enables the designer to implement all of the functions or a subset described in the IEEE Std. 488-1975. Using this standard, a variety of instruments can be interconnected and remotely or automatically programmed and controlled. The TMS 9914 is fabricated with N-channel silicon-gate technology and is completely TTL compatible on all inputs and outputs including the power supply (+5 V). It needs a single phase clock (nominally 5 MHz) which may be independent of the microprocessor system clock and, therefore, it can easily be interfaced with most microprocessors. The general purpose interface bus adapter (GPIBA) performs the majority of the functions contained in IEEE STd. 488-1975 and is versatile enough to allow software implementation of those sections not directly implemented in hardware.

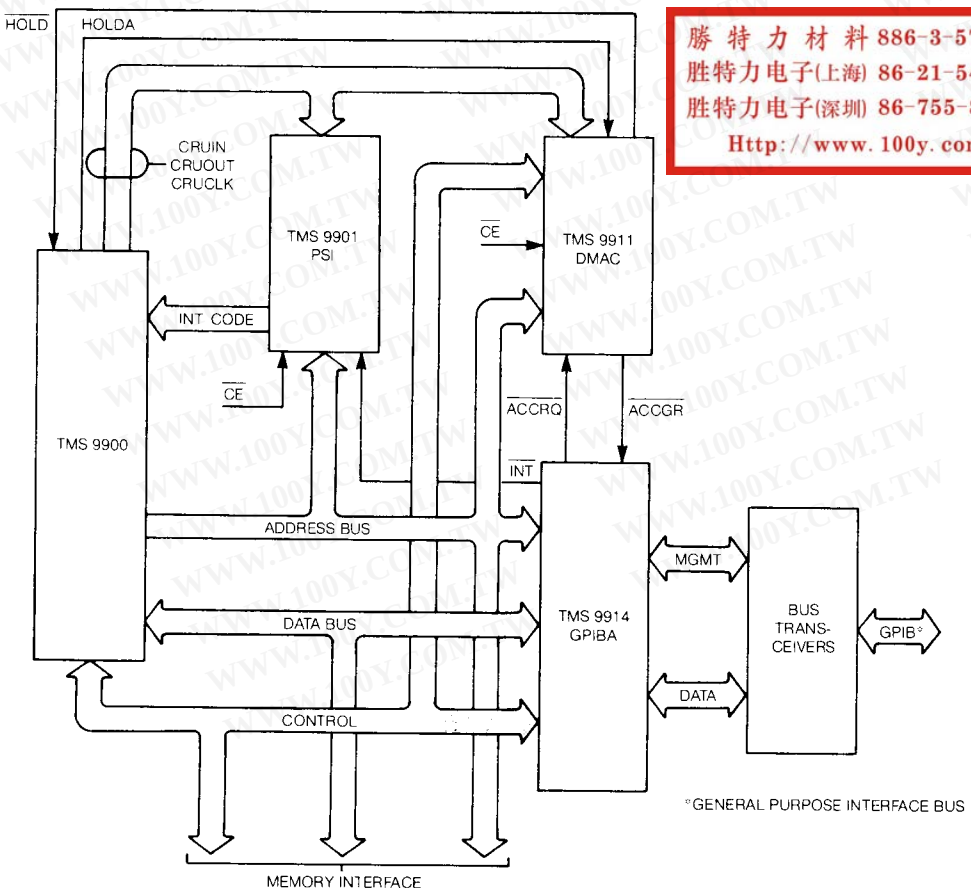

Figure 1. *Typical System Interconnect*

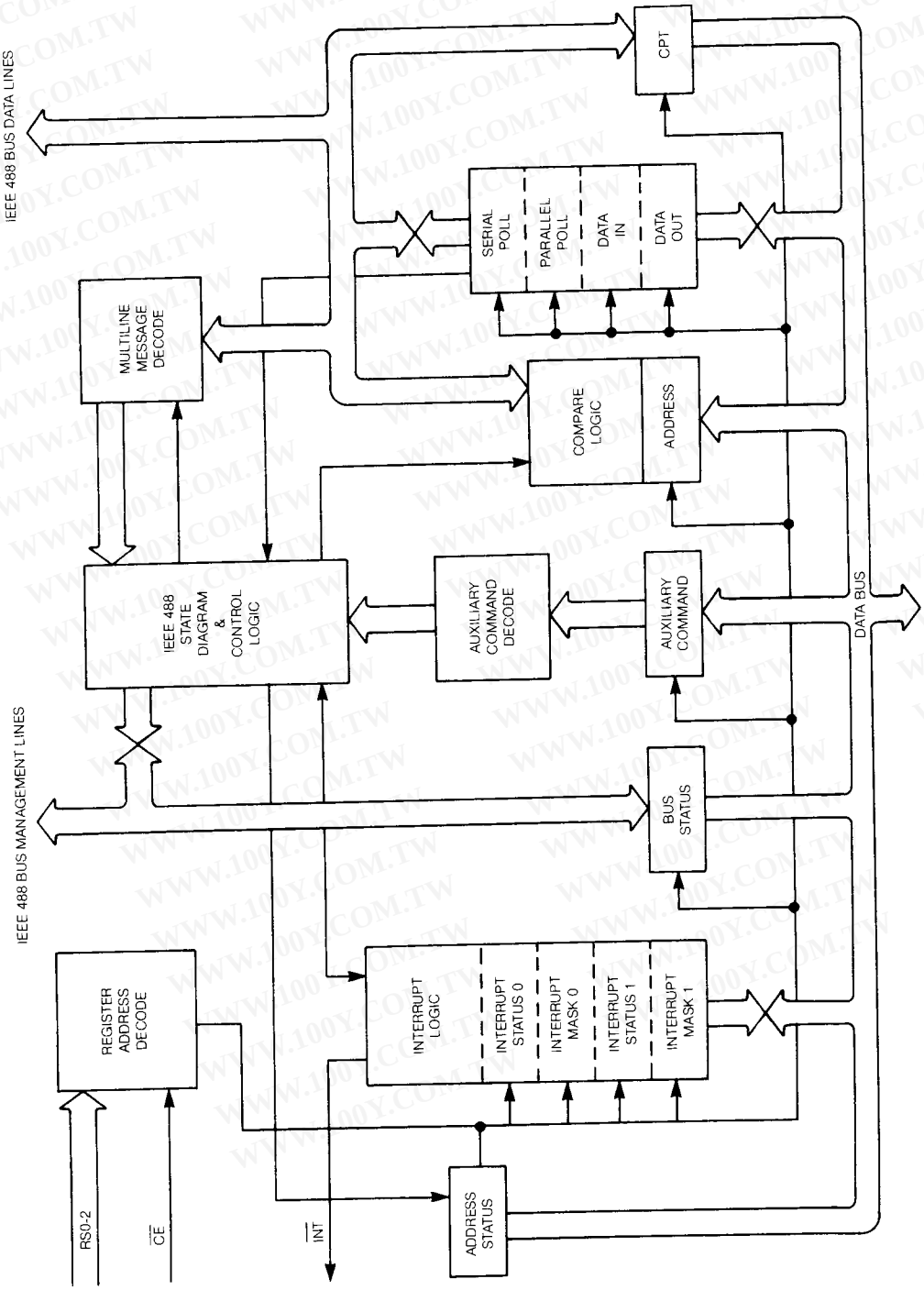

Figure 2. TMS 9914 Simplified Block Diagram

Table 1. Pin Description

Name	*I/O*	*Description*
DI01 through DI08	I/O	DATA I/O lines: allow data transfer between the TMS 9914 and the IEEE 488 data bus.
DAV	I/O	DATA VALID: Handshake Line. Sent by source device to indicate to acceptors that there is valid data on the IEEE bus data lines.
NRFD	I/O	NOT READY FOR DATA: Handshake Line. Sent by the acceptor to the source device to indicate when it is ready for a new byte of data.
NDAC	I/O	DATA NOT ACCEPTED: Handshake Line. Sent by acceptor to source device to indicate when it has accepted the current byte on the data bus.
ATN	I/O	ATTENTION: Management Line. Sent by the controller. When ATN is asserted, the information on the data lines is interpreted as commands, sent by the controller . . . When ATN is false, the data lines carry data.
IFC	I/O	INTERFACE CLEAR. Management Line. Sent by system controller to set the interface system, portions of which are contained in all interconnected devices in a known quiescent state. System controller assumes control. Open drain output with internal pullup.
REN	I/O	REMOTE ENABLE: Management Line. Sent by system controller and is used in conjunction with other messages to select between two alternate sources of programming data, e.g. via interface or front panel. Open drain output with internal pullup.
SRQ	I/O	SERVICE REQUEST: Management Line. Issued by a device on the bus to the controller to indicate a need for service.
EOI	I/O	END OR IDENTIFY: Management Line. If ATN is false, this signal is sent by the "talker" to indicate the end of a multiple byte transfer. If sent by the controller with ATN true, this will perform the parallel polling sequence.
$\overline{\text{CONTROLLER}}$	O	Bus transceiver control line. Indicates that the device is the controller.
TE	O	TALK ENABLE: Bus transceiver control line. Indicates the direction of data transfer on the data bus.
D0 through D7	I/O	Data I/O lines that allow transfer of data between TMS 9914 and the microprocessor.
RS0 through RS2	I	Address lines through which the TMS 9914 registers can be accessed by the microprocessor.
DBIN	I	When true (high) DBIN indicates to the TMS 9914 that the microprocessor is about to read from one of its registers. When false, that the microprocessor is about to write to one of its registers.
$\overline{\text{WE}}$	I	$\overline{\text{WRITE ENABLE}}$: indicates to the TMS 9914 that one of its registers is being written to.
$\overline{\text{CE}}$	I	$\overline{\text{CHIP ENABLE}}$: selects and enables the TMS 9914 for an microprocessor data transfer.
$\overline{\text{INT}}$	O	$\overline{\text{INT}}$: Open drain output. Sent to microprocessor to indicate the occurrence of an event on the bus requiring service.
$\overline{\text{ACCRQ}}$	O	$\overline{\text{ACCESS REQUEST}}$: Signal to TMS 9911 DMA controller requesting DMA.

PIN OUTS TO BE ASSIGNED

NOTE: The names of the IEEE bus lines have been maintained, and are therefore negative logic signals.

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FUNCTIONAL DESCRIPTION

The TMS 9914 interfaces to the CPU with an eight-bit bidirectional data bus, three register select lines, two DMA control lines, reset and interrupt request lines, a DBIN and a $\overline{WE}$ line.

The internal architecture of the TMS 9914 is arranged into 13 registers, there being seven WRITE and six READ registers. Some are actually address ports through which current status can be obtained. Table 2 lists these registers and their addresses. The microporcessor accesses a TMS 9914 register by supplying the correct register address in conjunction with $\overline{WE}$ and DBIN. The $\overline{CE}$ is used to enable the address decode.

Table 2. TMS 9914 Registers and Addresses

NAME	TYPE	RS2	RS1	RS0	DBIN	$\overline{WE}$
INTERRUPT STATUS 0	R	0	0	0	1	1
INTERRUPT MASK 0	W	0	0	0	0	0
INTERRUPT STATUS 1	R	0	0	1	1	1
INTERRUPT MASK 1	W	0	0	1	0	0
ADDRESS STATUS	R	0	1	0	1	1
BUS STATUS	R	0	1	1	1	1
AUXILIARY COMMAND	W	0	1	1	0	0
ADDRESS SWITCH	R	1	0	0	1	1
ADDRESS	W	1	0	0	0	0
SERIAL POLL	W	1	0	1	0	0
COMMAND PASS THROUGH	R	1	1	0	1	1
PARALLEL POLL	W	1	1	0	0	0
DATA IN	R	1	1	1	1	1
DATA OUT	W	1	1	1	0	0

NOTE: The Address Switch register is external to the TMS 9914

In DMA operation the TMS 9911 supplies the memory address but not the peripheral device address (i.e., RS0-2, $\overline{CE}$) are not supplied). When the TMS 9914 sets $\overline{ACCRQ}$ low true, it is either because of a byte input or a byte output, and this will happen whether or not DMA transfer will take place. If in response to $\overline{ACCRQ}$ an $\overline{ACCGR}$ (access granted) is received, the $\overline{ACCRQ}$ will be reset and a DMA transfer will take place between the system memory and either the Data In or Data Out register. If the data transfer is with the microprocessor and if the microprocessor addresses either the Data In or Data Out register, the $\overline{ACCRQ}$ line will be reset. Note that in DMA mode the sense of DBIN is inverted.

Table 3 lists the commands which are directly handled by the TMS 9914, and those which require intervention by the microprocessor for their implementation.

Table 3. Remote Multiple Message Coding

		DIO8	DIO7	DIO6	DIO5	DIO4	DIO3	DIO2	DIO1		Note
Addressed Command Group	ACG	X	0	0	0	X	X	X	X	AC	
Device Clear	DCL	X	0	0	1	0	1	0	0	UC	
Group Execute Trigger	GET	X	0	0	0	1	0	0	0	AC	
Go To Local	GTL	X	0	0	0	0	0	0	1	AC	
Listen Address Group	LAG	X	0	1	X	X	X	X	X	AD	
Local Lock Out	LLO	X	0	0	1	0	0	0	1	UC	
My Listen Address	MLA	X	0	1	L	L	L	L	L	AD	1
My Talk Address	MTA	X	1	0	T	T	T	T	T	AD	2
My Secondary Address	MSA	X	1	1	S	S	S	S	S	SE	3, 4
Other Secondary Address	OSA									SE	4, 5
Other Talk Address	OTA					TAG • MTA				AD	
Primary Command Group	PCG									—	6
Parallel Poll Configure	PPC	X	0	0	0	0	1	0	1	AC	7
Parallel Poll Enable	PPE	X	1	1	0	S	P	P	P	SE	8, 9
Parallel Poll Disable	PPD	X	1	1	1	D	D	D	D	SE	8, 10
Parallel Poll Unconfigure	PPU	X	0	0	1	0	1	0	1	UC	11
Secondary Command Group	SCG	X	1	1	X	X	X	X	X	SE	
Selected Device Clear	SDC	X	0	0	0	0	1	0	0	AC	
Serial Poll Disable	SPD	X	0	0	1	1	0	0	1	UC	
Serial Poll Enable	SPE	X	0	0	1	1	0	0	0	UC	
Take Control	TCT	X	0	0	0	1	0	0	1	AC	12
Talk Address Group	TAG	X	1	0	X	X	X	X	X	AD	
Universal Command Group	UCG	X	0	0	1	X	X	X	X	UC	
Unlisten	UNL	X	0	1	1	1	1	1	1	AD	
Untalk	UNT	X	1	0	1	1	1	1	1	AD	

Symbols: AC — Addressed Command
AD — Address (Talk or Listen)
UC — Universal Command
SE — Secondary (Command or Address)
0 — Logical Zero (high level on IEEE Bus; Low level within 9914).
1 — Logical One (Low level on IEEE Bus; High level within 9914).
X — Don't Care (received message)
X — Must Not Drive (transmitted message)

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Notes to Table 3:

1. L L L L L: Represents the coding for the device listen address.
2. T T T T T: Represents the coding for the device talk address.
3. S S S S S: Represents the coding for the device secondary address.
4. Secondary addresses will be handled via address pass through.
5. OSA will be handled as an invalid secondary address pass through by the MPU.
6. PCG = ACG v UCG v LAG v TAG
7. PPC will be handled in software by the MPU via Unrecognized Address Command Group pass through.
8. PPE, PPD will be handled via pass through next secondary feature.
9. S P P P represents the sense and bit for remote configurable parallel poll.
10. D D D D specify don't care bits that must be sent all zeroes, but need not be decoded by receiving device.
11. PPU is handled via Unrecognized Universal Command Group pass through.
12. TCT will be handled via Unrecognized Addressed Command Group pass through. However, in this case, the device must be in TADS before the pass through will occur.

Interrupt Status Registers 0 and 1

INT0	INT1	BI	BO	END	SPAS	RLC	MAC
GET	UUCG	UACG	APT	DCAS	MA	SRQ	IFC

INT0	An interrupt occurred in register 0
INT1	An interrupt occurred in register 1
BI	A byte has been received
BO	A byte has been output
END	An EOI occurred with ATN false
SPAS	Serial Poll Active State has occurred with rsv set in the Serial Poll register
RLC	A REMOTE/LOCAL change has occurred
MAC	An address change has occurred
GET	A Group Execute Trigger has occurred
UUCG	An Undefined Universal Command has been received
UACG	An Undefined Addressed Command has been received. This bit will also be set on receipt of a secondary command when the pts feature in the Auxiliary Command register is utilized.
APT	A secondary address has occurred
DCAS	Device Clear Active State has occurred
MA	My Address (MLAVMTA)·$\overline{\text{SPSM}}$
SRQ	A Service Request has been received
IFC	An IFC has been received

INT0 is the logical OR of each bit of Interrupt Status Register 0 ANDed with the respective bit of Interrupt Mask Register 0. INT1 is the same but applies to Interrupt Mask and Status Register 1. Reading either Interrupt Status Register will also clear it. The INT line will be cleared only when the interrupt status register which caused the interrupt is read.

Interrupt Mask Registers 0 and 1

		BI	BO	END	IFC	RLC	MAC
GET	UUCG	UACG	APT	DCAS	MA	SRQ	SPAS

The Interrupt Mask Registers 0 and 1 correspond to the Interrupt Status Registers 0 and 1 respectively, with the exception of INT0 and INT1.

Address Status Register

REM	LLO	ATN	LPAS	TPAS	LADS v LACS	TADS v TACS	ulpa

The Address Status Register is used to convey the addressed state of the talker/listener and the remote/local and local lockout condition. This information is derived from the TMS 9914 internal logic states at the time of reading. The ulpa bit is used for dual addressing and indicates the state of the LSB of the bus at last primary addressed time.

Bus Status Register

ATN	DAV	NDAC	NRFD	EOI	SRQ	IFC	REN

The Bus Status Register allows the microprocessor to obtain the current status of the IEEE 488 Bus Management Lines.

Auxiliary Command Register

C/S			f4	f3	f2	f1	f0

The Auxiliary Command Register allows control of additional features on chip and provides a means of inputting some of the local messages to the interface functions. Table 4 lists these messages and commands. If C/S = 1, the feature will be set and if C/S = 0, the feature will be cleared. If C/S = NA, it should be sent as zero.

Table 4. Auxiliary Commands

Function	*Mnemonic*	*C/S*	*f4*	*f3*	*f2*	*f1*	*f0*
Chip Reset	rst	0/1	0	0	0	0	0
Release ACDS holdoff	dacr	0/1	0	0	0	0	1
Release RFD holdoff	rhfd	NA	0	0	0	1	0
Holdoff on all data	hdfa	0/1	0	0	0	1	1
Holdoff on EOI only	hdfe	0/1	0	0	1	0	0
Set new byte available false	nbaf	NA	0	0	1	0	1
Force group execute trigger	fget	0/1	0	0	1	1	0
Return to local	rtl	0/1	0	0	1	1	1
Return to local immediate	rtli	0	0	0	1	1	1
Send EOI with next byte	feoi	NA	0	1	0	0	0
Listen only	lon	0/1	0	1	0	0	1
Talk only	ton	0/1	0	1	0	1	0
Take control synchronously	tcs	NA	0	1	1	0	1
Take control asynchronously	tca	NA	0	1	1	0	0
Go to standby	gts	NA	0	1	0	1	1
Request parallel poll	rpp	0/1	0	1	1	1	0
Send interface clear	sic	0/1	0	1	1	1	1
Send remote enable	sre	0/1	1	0	0	0	0
Request contol	rqc	NA	1	0	0	0	1
Release control	rlc	NA	1	0	0	1	0
Disable all interrupts	dai	0/1	1	0	0	1	1
Pass through next secondary	pts	NA	1	0	1	0	0
Set T1 delay	stdl	0/1	1	0	1	0	1

Address Register

edpa	dal	dat	A5	A4	A3	A2	A1

edpa enable dual primary addressing
dal disable the listen function
dat disable the talk function
A1 — A5 primary device address

The Address Switch Register corresponds to the Address Register. A power-up RESET or a rst command with C/S = 1 will leave the chip in a totally idle state. At this point, the Address Switch Register is read and the value is written into the Address Register. The reset condition is then cleared by sending rst with C/S = 0.

Serial Poll Register

S8	rsv	S6	S5	S4	S3	S2	S1

The Serial Poll register is used to establish the status byte that is sent out when the controller conducts a serial poll. Bits 1 through 6 and 8 contain status information, while bit 7, rsv, is used to enable the SRQ line and to indicate to the controller which device(s) was responsible for making a service request.

Command Pass Through Register

DIO8	DIO7	DIO6	DIO5	DIO4	DIO3	DIO2	DIO1

The Command Pass Through Register is used to pass through to the microprocessor any commands or secondary addresses that are not automatically handled in the TMS 9914.

Parallel Poll Register

PP8	PP7	PP6	PP5	PP4	PP3	PP2	PP1

This register contains the status bit that is output when the controller conducts a parallel poll.

Data-In Register

DIO8	DIO7	DIO6	DIO5	DIO4	DIO3	DIO2	DIO1

The data-in register is used to move data from the interface bus when the chip is addressed as a listener. Upon receipt of a data byte, the chip will hold NRFD true until the microprocessor reads the data-in register, when NRFD will be set false automatically.

Data-Out Register

DIO8	DIO7	DIO6	DIO5	DIO4	DIO3	DIO2	DIO1

The data-out register is used to move data from the TMS 9914 onto the IEEE std 488-1975 data bus.

After sending a byte out on the bus, the device can take part in a new handshake only after a new byte is placed in the data-out register, when it will be able to send DAV true again.

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IEEE 488.2 Controller Chip —

NAT9914

- Pin compatible with TI TMS9914A
- Software compatible with NEC µPD7210 or TI TMS9914A controller chips
- Low power consumption
- Meets all IEEE 488.2 requirements
  - Bus line monitoring
  - Preferred implementation of requesting service
  - Will not send messages when there are no Listeners
- Performs all IEEE 488.1 interface functions
- Programmable data transfer rate (T1 delays of 350 ns, 500 ns, 1.1 µs, and 2 µs)
- Automatic EOS and/or NL message detection
- Direct memory access (DMA)
- Automatically processes IEEE 488 commands and reads undefined commands
- TTL-compatible CMOS device
- Programmable clock rate up to 20 MHz
- Reduces driver overhead
  - Does not lose a data byte if ATN is asserted while transmitting data

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Description

The NAT9914 IEEE 488.2 controller chip can perform all the interface functions defined by that the IEEE Standard 488.1-1987, and also meets the additional requirements and recommendations of the IEEE Standard 488.2-1987. Connected between the processor and the IEEE 488 bus, the NAT9914 provides high-level management of the IEEE 488 bus, significantly increases the throughput of driver software, and simplifies both the hardware and software design. The NAT9914 performs complete IEEE 488 Talker, Listener, and Controller functions. In addition to its numerous improvements, the NAT9914 is also completely pin compatible with the TI TMS 9914A and software compatible with the NEC µPD7210 and TI TMS9914A controller chips.

IEEE 488.2 Overview

The IEEE 488.2 standard removes the ambiguities of IEEE 488.1 by standardizing the way instruments and controllers operate. It defines data formats, status reporting, error handling, and common configuration commands to which all IEEE 488.2 instruments must respond in a precise manner. It also defines a set of controller requirements. The benefits of IEEE 488.2 for the test system developer are reduced development time and cost because systems are more compatible and reliable. The NAT9914 brings the full power of IEEE 488.2 to the design engineer along with numerous other design and performance benefits, while retaining the 40-pin and 44-pin hardware configurations of the TI TMS 9914A.

General

The NAT9914 manages the IEEE 488 bus. You program the IEEE 488 bus by writing control words into the appropriate registers. CPU-readable status registers supply operational feedback. The NAT9914 mode determines the function of these registers. On power up or reset, the NAT9914 registers resemble the TMS9914A register set with additional registers that supply extra functionality and IEEE 488.2 compatibility. In this mode, the NAT9914 is completely pin compatible with the TI TMS9914A. If you enable the 7210 mode, the registers resemble the NEC µPD7210 register set with additional registers that supply extra functionality and IEEE 488.2 compatibility. This mode is not pin compatible with the NECµPD7210. Figure 3 shows the key components of the NAT9914.

NATIONAL INSTRUMENTS™

IEEE 488.2 Controller Chip

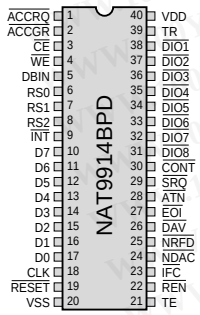

Figure 1. NAT9914BPD Pin Configuration

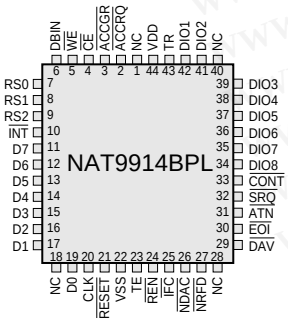

Figure 2. NAT9914BPL Pin Configuration

Pin Identification

Pin Number		Mnemonic	Type	Description
PLCC	DIP			
11, 12, 13, 14, 15, 16, 17, 19	10, 11, 12, 13, 14, 15, 16, 17	D(7-0)	I/O†	Bidirectional 3-state data bus transfers commands, data, and status between the NAT9914 and the CPU. **D0 is the most significant bit.**
4	3	CE*	I	Chip Enable gives access to the register selected by a read or write operation, and the register selects RS(2-0).
6	5	DBIN	I†	With the Data Bus Input, you can place the contents of the register selected by RS(2-0) and CE* onto the data bus D(7-0). The polarity of DBIN is reversed for DMA operation.
5	4	WE*	I†	The Write input latches the contents of the data bus D(7-0) into the register selected by RS(2-0).
3	2	ACCGR*	I†	The Access Grant signal selects the DIR or CDOR for the current read or write cycle.
2	1	ACCRQ*	O	The Access Request output asserts to request a DMA Acknowledge cycle.
20	18	CLK	I†	The CLK input can be up to 20 MHz.
21	19	RESET*	I†	Asserting the RESET* input places the NAT9914 in an initial, idle state.
10	9	INT* (OC)	0	The Interrupt output asserts when one of the unmasked interrupt conditions is true. The NAT9914 does not drive INT* high. The INT* pin must be pulled up by an external resistor.
9, 8, 7	8, 7, 6	RS(2-0)	I†	The Register Selects determine which register to access during a read or write operation.
25	23	IFC* (OC)	I/O†,††	Bidirectional control line initializes the IEEE 488 interface functions.
24	22	REN* (OC)	I/O†	Bidirectional control line selects either remote or local control of devices.
31	28	ATN*	I/O†	Bidirectional control line indicates whether data on the DIO lines is an interface or device-dependent message.
32	29	SRQ*	I/O†	Bidirectional control line requests service from the controller.
34, 35, 36, 37, 38, 39, 41, 42	31, 32, 33, 34, 35, 36 37, 38	DIO(8-1)*	I/O†	8-bit bidirectional IEEE 488 data bus
29	26	DAV*	I/O†	Handshake line indicates that the data on the DIO(8-1)* lines is valid.
27	25	NRFD*	I/O†	Handshake line indicates that the device is ready for data.
26	24	NDAC*	I/O†	Handshake line indicates the completion of a message reception.
30	27	EOI*	I/O†	Bidirectional control line indicates the last byte of a data message or executes a parallel poll.
23	21	TE	O†	Talk Enable controls the direction of the IEEE 488 data transceiver.

Pin Number		Mnemonic	Type	Description
PLCC	DIP			
43	39	TR	O†	Trigger asserts when one of the trigger conditions is satisfied.
33	30	CONT*	O†	Controller asserts when the NAT9914 is Controller-In-Charge.
44	40	VDD	–	Power pin – +5 V (±5%)
22	20	VSS	–	Ground pin – 0 V
1, 18, 28,40	–	NC	–	No connect

OC= Open collector.

† The pin contains an internal pull-up resistor of 25 to 100 kΩ.

* Active low.

†† In controller applications where the CLK signal frequency is > 8 MHz, IFC* should be pulled up with a 4.7 kΩ resistor.

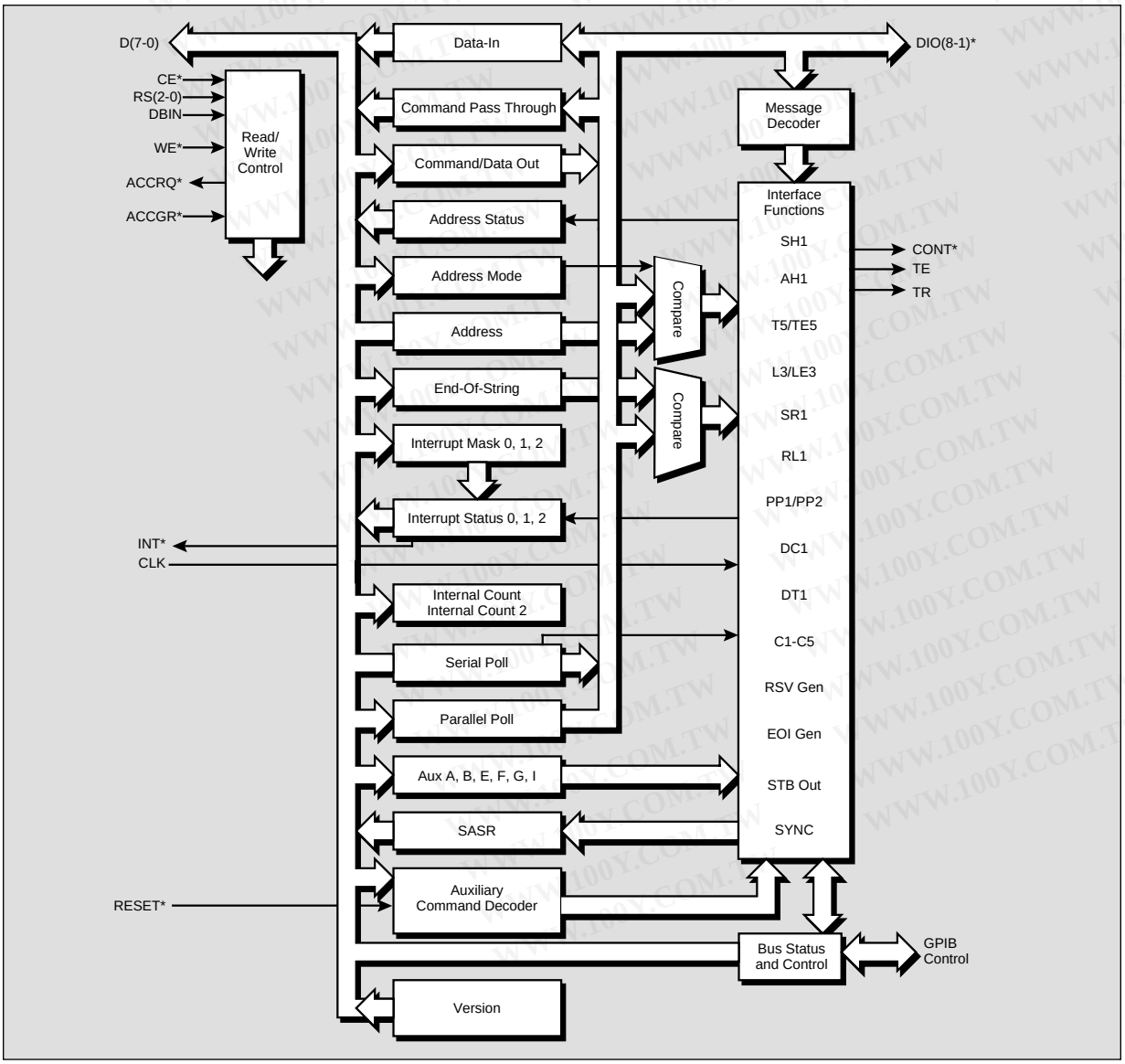

Figure 3. NAT9914 Block Diagram

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IEEE 488.2 Controller Chip

9914 Mode Registers

In 9914 mode, the NAT9914 registers consist of all the TI TMS9914A registers and two types of additional registers – newly defined registers and paged-in registers. The NAT9914 maps the newly defined registers into the unused portion of the 9914 address space. Each paged-in register appears at offset 2 immediately after you issue an auxiliary page-in command, and it remains there until you page another register into the same space or you issue a reset. The table below lists all the registers in the 9914 register set. See the NAT9914 Reference Manual available at **ni.com** for more information.

9914 Register Set

Register	Page In	RS(2-0)			WE*	DBIN	CE*	ACCGR*
Interrupt Status 0	U	0	0	0	1	1	0	1
Interrupt Mask 0	U	0	0	0	0	0	0	1
Interrupt Status 1	U	0	0	1	1	1	0	1
Interrupt Mask 1	U	0	0	1	0	0	0	1
Address Status	U	0	1	0	1	1	0	1
Interrupt Mask 2†	P	0	1	0	0	0	0	1
End-of-String†	P	0	1	0	0	0	0	1
Bus Control†	P	0	1	0	0	0	0	1
Accessory†	P	0	1	0	0	0	0	1
Bus Status	U	0	1	1	1	1	0	1
Auxiliary Command	U	0	1	1	0	0	0	1
Interrupt Status 2†	P	1	0	0	1	1	0	1
Address	U	1	0	0	0	0	0	1
Serial Poll Status†	P	1	0	1	1	1	0	1
Serial Poll Mode	U	1	0	1	0	0	0	1
Command Pass Thru	U	1	1	0	1	1	0	1
Parallel Poll	U	1	1	0	0	0	0	1
Data-In	U	1	1	1	1	1	0	1
Data-In	U	X	X	X	X	0	X	0
Command/Data Out	U	1	1	1	0	0	0	1
Command/Data Out	U	X	X	X	0	1	X	0

The '†' symbol denotes features (such as registers and auxiliary commands) that are not available in the TMS9914A.

Notes for the PAGE-IN column:

U = Page-in auxiliary commands do not affect the register offset.

P = The register offset is valid only after a page-in auxiliary command.

7210 Mode Registers

The NAT9914 registers include all the NEC µPD7210 registers plus two types of additional registers – extra auxiliary registers and paged-in registers. You write the extra auxiliary registers the same as standard µPD7210 auxiliary registers. On issuing an auxiliary page-in command, the paged-in registers appear at the same offsets as existing µPD7210 registers. At the end of the next CPU access, the chip pages out the paged-in registers. The following table lists all the registers in the 7210 mode register set. See the NAT9914 Reference Manual available at **ni.com** for more information.

7210 Register Set

Register	PAGE-IN	A(2-0)			WE*	DBIN	CE*	ACCGR*
Data-In	U	0	0	0	1	1	0	1
Data-In	X	X	X	X	X	0	X	0
Command/Data Out	U	0	0	0	0	0	0	1
Command/Data Out	X	X	X	X	0	1	X	0
Interrupt Status 1	U	0	0	1	1	1	0	1
Interrupt Mask 1	U	0	0	1	0	0	0	1
Interrupt Status 2	U	0	1	0	1	1	0	1
Interrupt Mask 2	U	0	1	0	0	0	0	1
Serial Poll Status	N	0	1	1	1	1	0	1
Serial Poll Mode	N	0	1	1	0	0	0	1
Version	P	0	1	1	1	1	0	1
Internal Counter 2	P	0	1	1	0	0	0	1
Address Status	U	1	0	0	1	1	0	1
Address Mode	U	1	0	0	0	0	0	1
Command Pass Through	N	1	0	1	1	1	0	1
Auxiliary Mode	U	1	0	1	0	0	0	1
Source/Acceptor Status†	P	1	0	1	1	1	0	1
Address 0	N	1	1	0	1	1	0	1
Address	N	1	1	0	0	0	0	1
Interrupt Status 0†	P	1	1	0	1	1	0	1
Interrupt Mask 0†	P	1	1	0	0	0	0	1
Address 1	N	1	1	1	1	1	0	1
End-Of-String	N	1	1	1	0	0	0	1
Bus Status†	P	1	1	1	1	1	0	1
Bus Control†	P	1	1	1	0	0	0	1

The '†' symbol denotes features (such as registers and auxiliary commands) that are not available in the TMS9914A.

Notes for the PAGE-IN column:

U = The page-in auxiliary command does not affect the register.

N = The register offset is always valid except for immediately after a page-in auxiliary command.

P = The register is valid only immediately after a page-in auxiliary command.

Preliminary DC Characteristics

T_A 0 to 70 °C; V_{CC} = 5 V ±5%

Parameter	Symbol	Limits Min	Limits Max	Unit	Test Condition
Voltage input low	V_{IL}	-0.5	+0.8	V	–
Voltage input high	V_{IH}	+2.0	V_{CC}	V	–
Voltage output low	V_{OL}	0	0.4	V	–
Voltage output high	V_{OH}	+2.4	VCC	V	–
Input/output Leakage current	–	-10	+10	µA	without internal pull-up
Input/output Leakage current	–	-200	+200	µA	with internal pull-up
Supply current	–	–	45	mA	–
Output current low					
All pins except ACCRQ	I_{OL}	2	–	mA	0.4 V @ I_{OL}
ACCRQ	I_{OL}	4	–	mA	0.4 V @ I_{OL}
Input current low	I_{IL}	–	- 0.5	mA	–
Supply voltage	V_{DD}	4.75	5.25	V	–

Capacitance

T_A 0 to 70 °C; V_{CC} = 5 V ±5%

Parameter	Symbol	Limits Min	Limits Max	Unit	Test Condition
Input capacitance	C_{IN}	–	10	pF	–
Output capacitance	C_{OUT}	–	10	pF	–
I/O capacitance	$C_{I/O}$	–	10	pF	–

Absolute Maximum Ratings

Property	Range
Supply voltage, V_{DD}	-0.5 to +7.0 V
Input voltage, V_I	-0.5 to V_{DD} +0.5 V
Operating temperature, T_{OPR}	0 to +70° C
Storage temperature, T_{STG}	-40 to +125° C

Comment: Exposing the device to stresses above those listed could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

AC Characteristics

T_A 0 to 70 °C; V_{CC} = 5 V ±5%

Parameter	Symbol	Limits Min	Limits Max	Unit	Test Condition
Address hold from $\overline{CE}$, $\overline{WE}$,and DBIN	t_{AH}	0	–	ns	–
Address setup to $\overline{CE}$, $\overline{WE}$, and DBIN	t_{AS}	0	–	ns	–
Data float from $\overline{CE}$ or DBIN	t_{DF}	–	20	ns	–
Data delay from DBIN↓	t_{DR}	–	75	ns	$\overline{ACCGR}$=0
$\overline{ACCRQ}$ unassertion	t_{DU}	–	20	ns	–
Data delay from $\overline{CE}$↓	t_{RD}	–	80	ns	$\overline{ACCGR}$=1
$\overline{CE}$ recovery width	t_{RR}	80	–	ns	–
$\overline{CE}$ pulse width	t_{RW}	80	–	ns	–
Data hold from $\overline{WE}$↑	t_{WH}	0	–	ns	–
Data setup to $\overline{WE}$↑	t_{WS}	60	–	ns	–

Notes:

- t_{AS} is the setup time to $\overline{CE}$↓ or $\overline{WE}$↓ whichever is later.
- t_{AH} is the hold time from $\overline{WE}$↑ or $\overline{CE}$↑ whichever is earlier.

Timing Waveforms

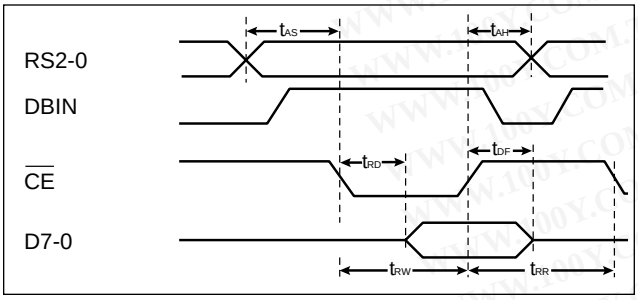

Figure 4. CPU Read

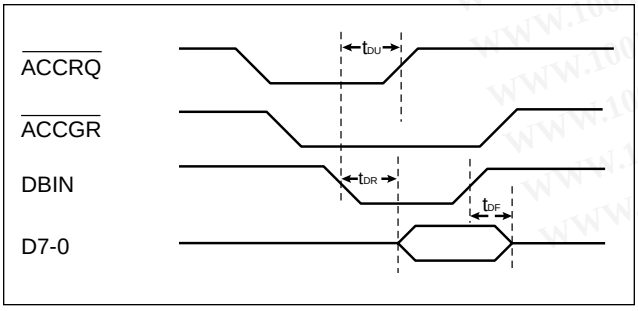

Figure 5. DMA Read

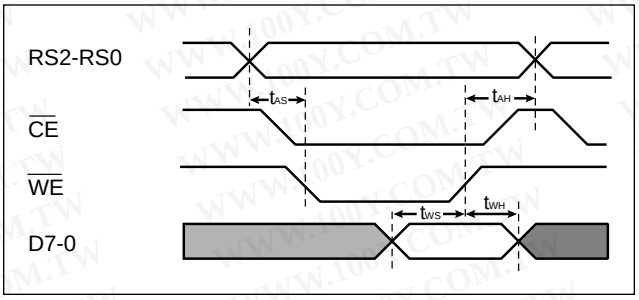

Figure 6. CPU Write

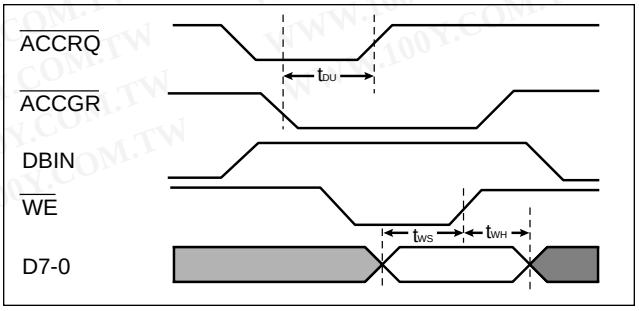

Figure 7. DMA Write

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Source Handshake

Parameter	Symbol	Limits (ns) Min	Limits (ns) Max	Test Condition
$\overline{NDAC}\uparrow$ to $\overline{DAV}\uparrow$	t_{ND}	–	40	–
$\overline{NDAC}\uparrow$ to $\overline{INT}\downarrow$ or $\overline{ACCRQ}\downarrow$	t_{NI}	–	40	INT(DOIE Bit=1) ACCGR (DMAO Bit=1)
$\overline{WE}\uparrow$ to $\overline{DAV}\downarrow$	t_{WD}	2000	2180	2 µs T1, 5MHz
$\overline{WE}\uparrow$ to $\overline{DAV}\downarrow$	t_{WD}	1200	1380	1.1 µs T1, 5MHz
$\overline{WE}\uparrow$ to $\overline{DAV}\downarrow$	t_{WD}	600	780	500 ns T1, 5MHz
$\overline{WE}\uparrow$ to $\overline{DAV}\downarrow$	t_{WD}	400	580	350 ns T1, 5MHz

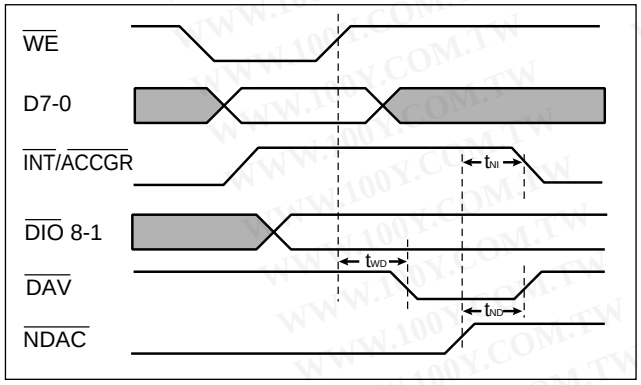

Figure 8. Source Handshake Timing

Acceptor Handshake

Parameter	Symbol	Limits (ns) Min	Limits (ns) Max	Test Condition
$\overline{DAV}\downarrow$ to $\overline{NDAC}\uparrow$	t_{DD}		35+3T	
$\overline{DAV}\uparrow$ to $\overline{NDAC}\downarrow$	t_{DF}		25	
$\overline{DAV}\downarrow$ to $\overline{INT}\downarrow$ or $\overline{ACCRQ}\downarrow$	t_{DI}		50+2T	INT(DIIE Bit=1), ACCGR (DMAI Bit=1)
$\overline{DAV}\downarrow$ to $\overline{NRFD}\downarrow$	t_{DR}		20	
$\overline{DBIN}\uparrow$ to $\overline{NRFD}\uparrow$	t_{NR}		35	Read of DIR, not in Holdoff state

Note: T = one clock period

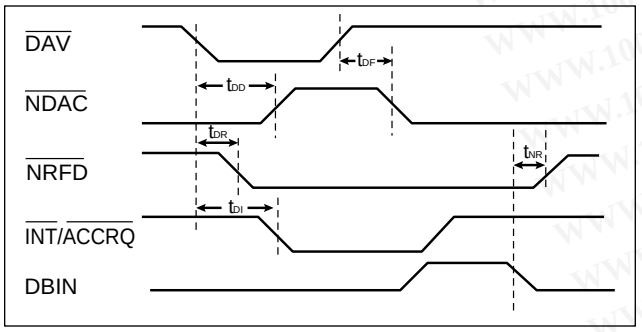

Figure 9. Acceptor Handshake Timing

Response to ATN

Parameter	Symbol	Limits (ns) Min	Limits (ns) Max	Test Condition
$\overline{ATN}\uparrow$ to $\overline{NRFD}\downarrow$	t_{AF}		35	Acceptor handshake holdoff
$\overline{ATN}\downarrow$ to $\overline{NDAC}\downarrow$	t_{AN}		35	AIDS → ANRS
$\overline{ATN}\downarrow$ to $\overline{TE}\downarrow$	t_{AT}		30	TACS → TADS

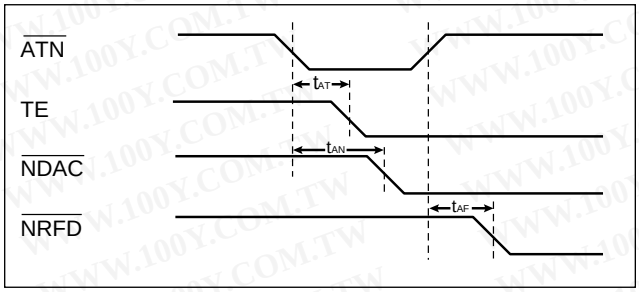

Figure 10. ATN Response Timing

Parallel Poll

Parameter	Symbol	Limits (ns) Min	Limits (ns) Max	Test Condition
$\overline{EOI}\downarrow$ to $\overline{DIO}\downarrow$ valid	t_{ED}		90	PPSS → PPAS
$\overline{EOI}\downarrow$ to $\overline{TE}\uparrow$	t_{ET}		30	PPSS → PPAS
$\overline{EOI}\uparrow$ to $\overline{TE}\downarrow$	t_{TE}		30	PPAS → PPSS

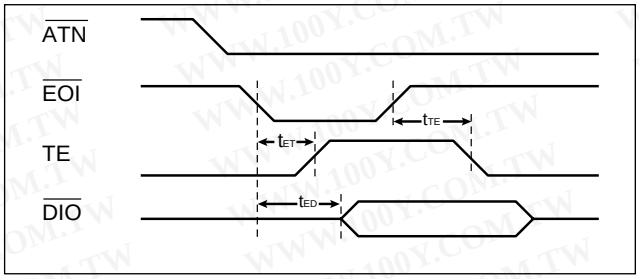

Figure 11. Parallel Poll Response Timing

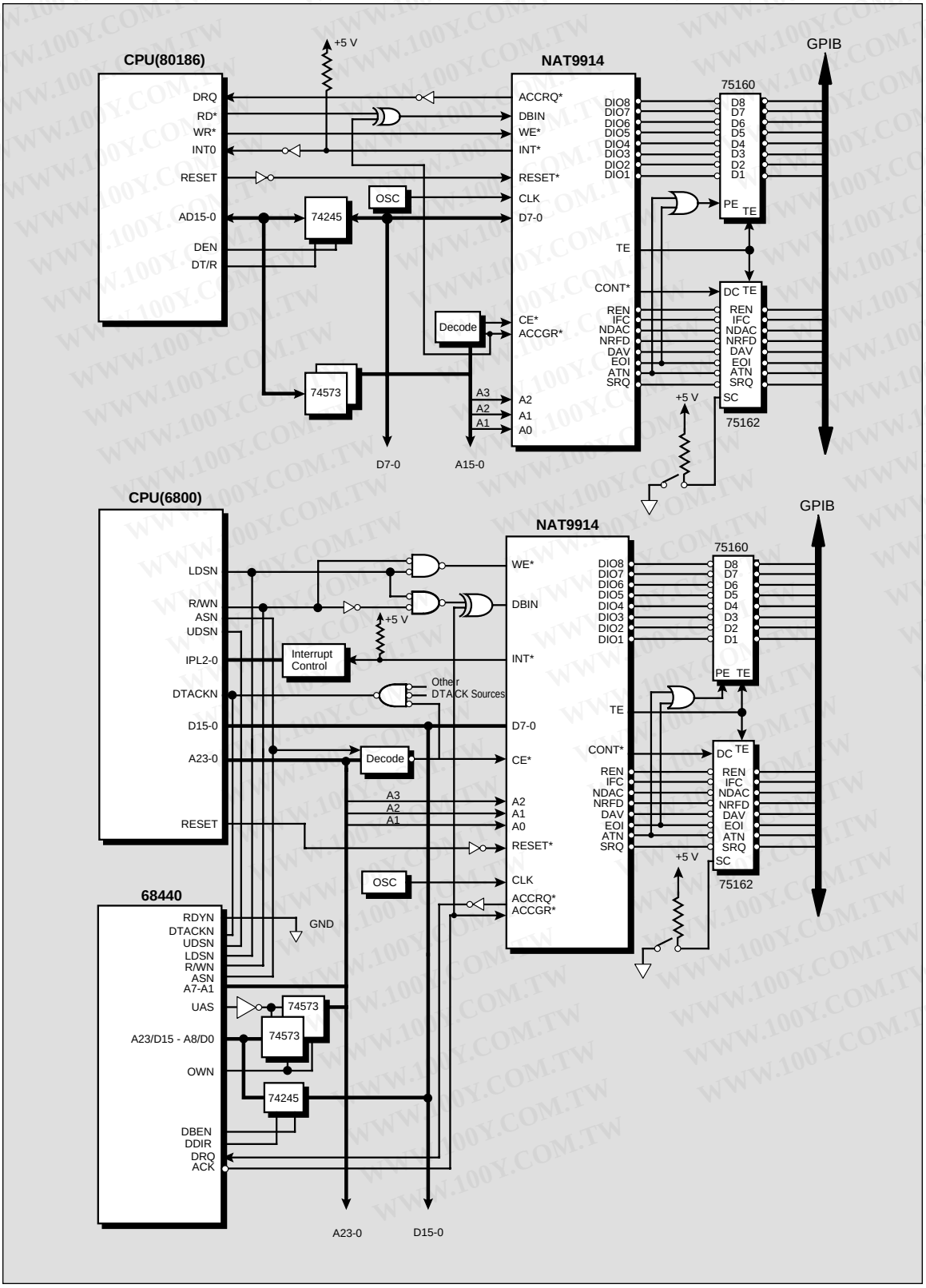

Figure 12. Typical CPU Systems with NAT9914

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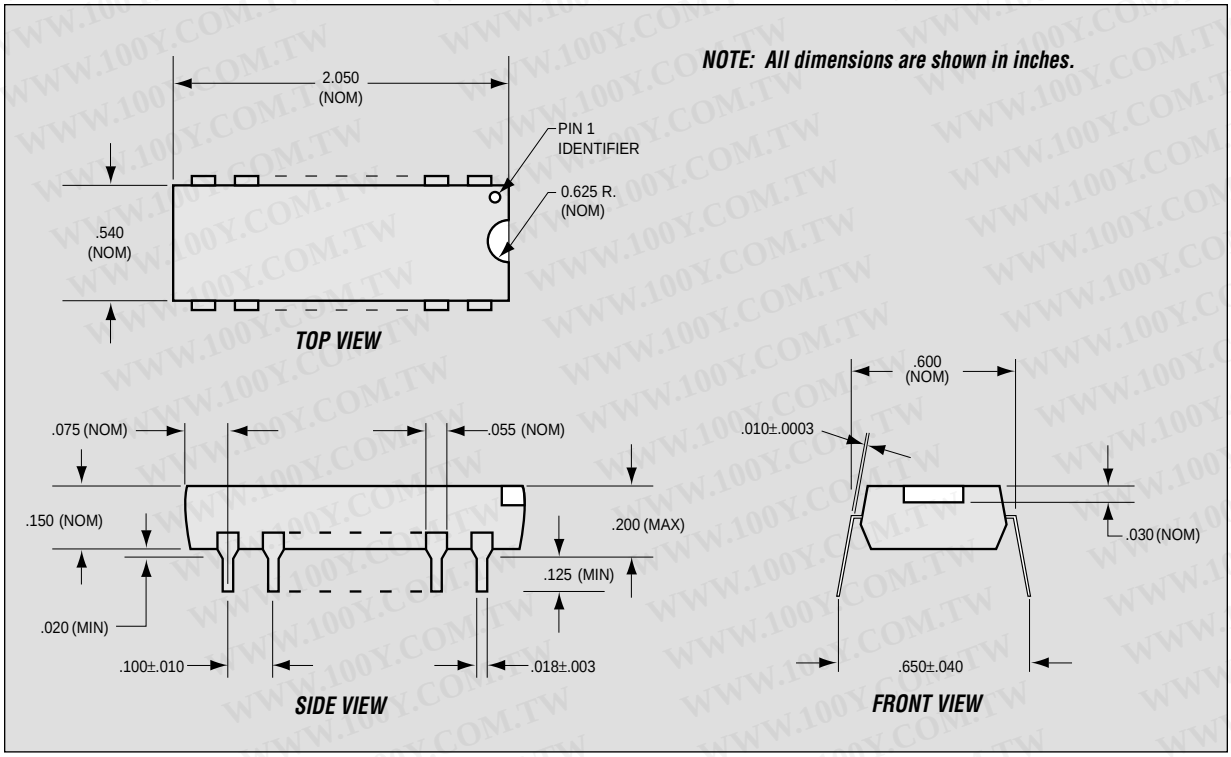

Figure 13. Mechanical Data 40-Pin Plastic DIP

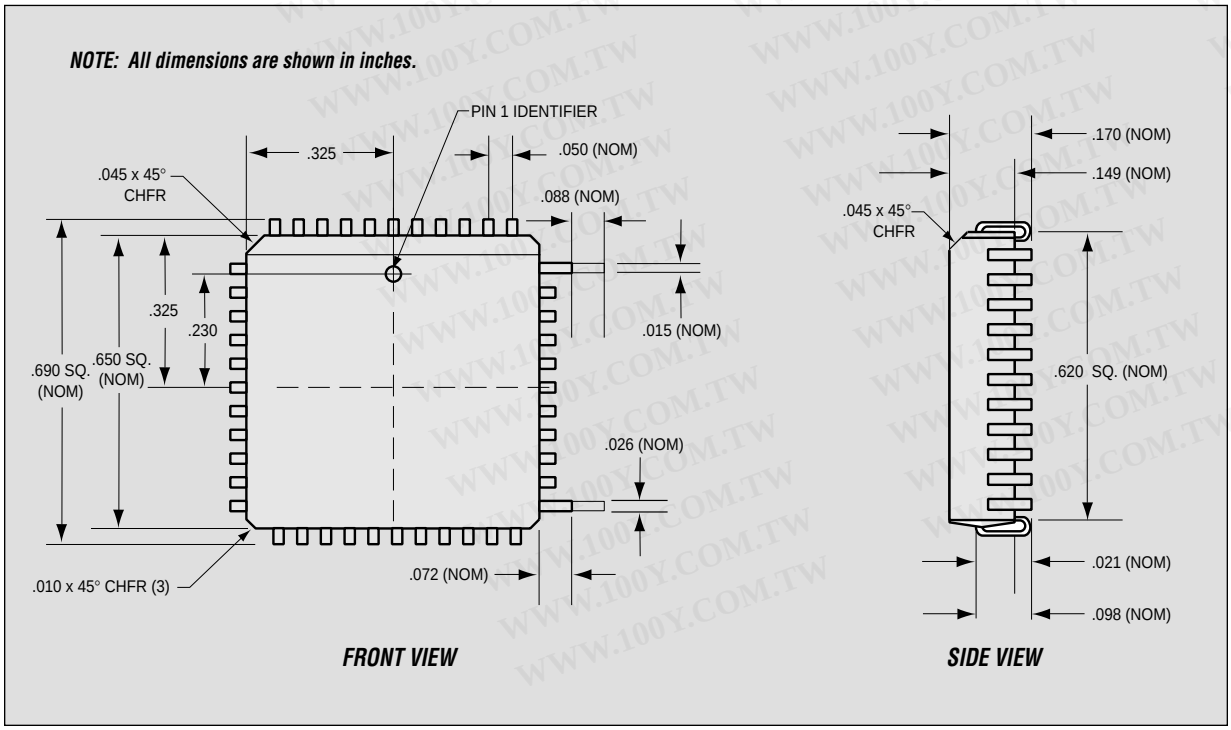

Figure 14. Mechanical Data 44-Pin PLCC

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Ordering Information

NAT9914BPD
NAT9914BPL

Part Number Legend

a	b	c	d	e
NAT	9914	B	P	D

a. Family name – NAT = 8-bit GPIB Talker/Listener/Controller interface
b. Device number – 9914 = TI TMS9914A pin-compatible part
c. Revision
d. Package material – P = plastic
e. Package type – D = Dual Inline Package (DIP)
L = Plastic Leaded Chip Carrier (PLCC)

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