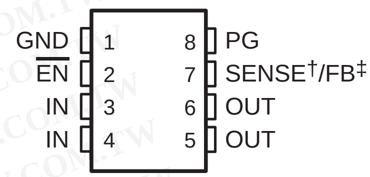
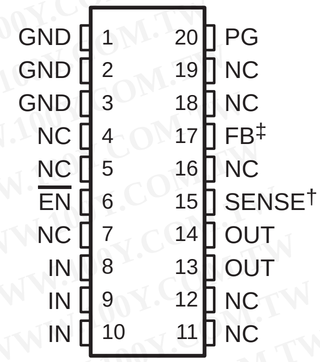
- **Available in 5-V, 4.85-V, and 3.3-V Fixed-Output and Adjustable Versions**
- **Very Low-Dropout Voltage . . . Maximum of 32 mV at I_O = 100 mA (TPS7150)**
- **Very Low Quiescent Current – Independent of Load . . . 285 μA Typ**
- **Extremely Low Sleep-State Current 0.5 μA Max**
- **2% Tolerance Over Specified Conditions For Fixed-Output Versions**
- **Output Current Range of 0 mA to 500 mA**
- **TSSOP Package Option Offers Reduced Component Height for Space-Critical Applications**
- **Power-Good (PG) Status Output**

D OR P PACKAGE
(TOP VIEW)



PW PACKAGE
(TOP VIEW)



NC – No internal connection
† SENSE – Fixed voltage options only (TPS7133, TPS7148, and TPS7150)
‡ FB – Adjustable version only (TPS7101)

description

The TPS71xx integrated circuits are a family of micropower low-dropout (LDO) voltage regulators. An order of magnitude reduction in dropout voltage and quiescent current over conventional LDO performance is achieved by replacing the typical pnp pass transistor with a PMOS device.

Because the PMOS device behaves as a low-value resistor, the dropout voltage is very low (maximum of 32 mV at an output current of 100 mA for the TPS7150) and is directly proportional to the output current (see Figure 1). Additionally, since the PMOS pass element is a voltage-driven device, the quiescent current is very low and remains independent of output loading (typically 285 μA over the full range of output current, 0 mA to 500 mA). These two key specifications yield a significant improvement in operating life for battery-powered systems. The LDO family also features a sleep mode; applying a TTL high signal to EN (enable) shuts down the regulator, reducing the quiescent current to 0.5 μA maximum at T_J = 25°C.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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description (continued)

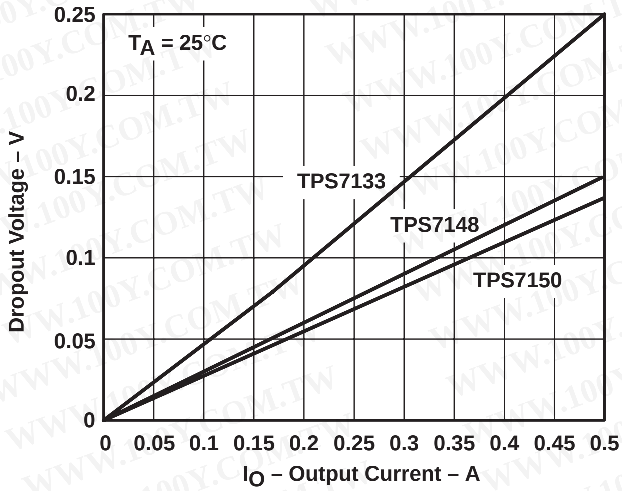


Figure 1. Dropout Voltage Versus Output Current

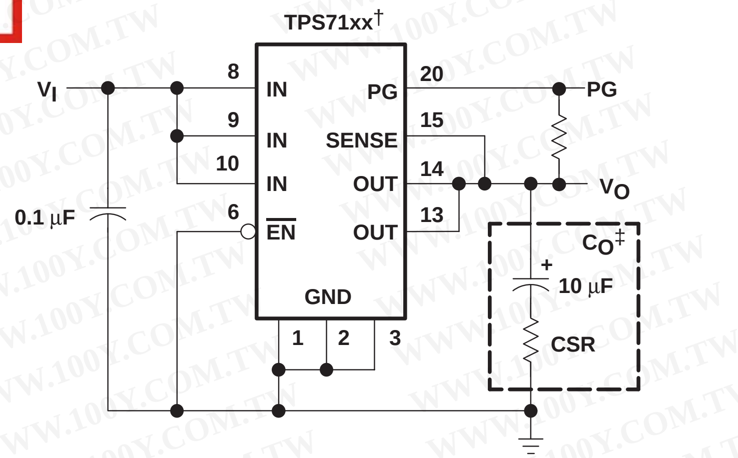
Power good (PG) reports low output voltage and can be used to implement a power-on reset or a low-battery indicator.

The TPS71xx is offered in 3.3-V, 4.85-V, and 5-V fixed-voltage versions and in an adjustable version (programmable over the range of 1.2 V to 9.75 V). Output voltage tolerance is specified as a maximum of 2% over line, load, and temperature ranges (3% for adjustable version). The TPS71xx family is available in PDIP (8 pin), SO (8 pin), and TSSOP (20-pin) packages. The TSSOP has a maximum height of 1.2 mm.

AVAILABLE OPTIONS

T_J	OUTPUT VOLTAGE (V)			PACKAGED DEVICES			CHIP FORM (Y)
	MIN	TYP	MAX	SMALL OUTLINE (D)	PLASTIC DIP (P)	TSSOP (PW)	
–40°C to 125°C	4.9	5	5.1	TPS7150QD	TPS7150QP	TPS7150QPW	TPS7150Y
	4.75	4.85	4.95	TPS7148QD	TPS7148QP	TPS7148QPW	TPS7148Y
	3.23	3.3	3.37	TPS7133QD	TPS7133QP	TPS7133QPW	TPS7133Y
	Adjustable† 1.2 V to 9.75 V			TPS7101QD	TPS7101QP	TPS7101QPW	TPS7101Y

† The D and PW packages are available taped and reeled. Add R suffix to device type (e.g., TPS7150QDR). The TPS7101Q is programmable using an external resistor divider (see application information). The chip form is tested at 25°C.



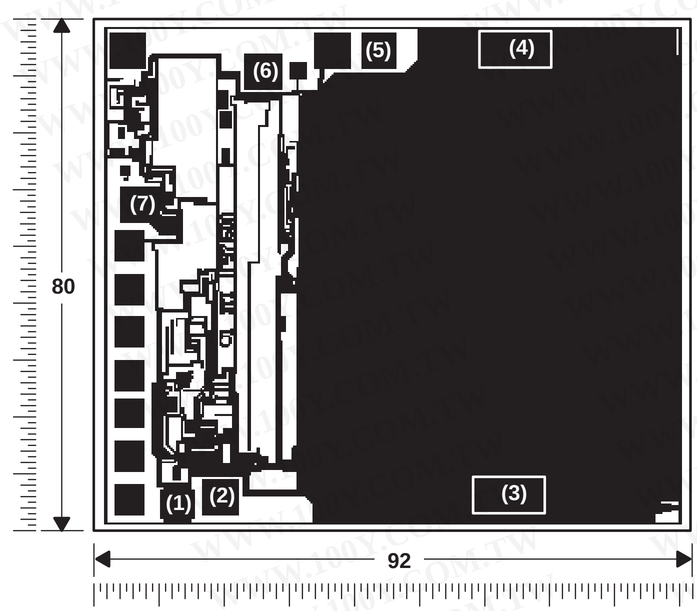
† TPS7133, TPS7148, TPS7150 (fixed-voltage options)
‡ Capacitor selection is nontrivial. See application information section for details.

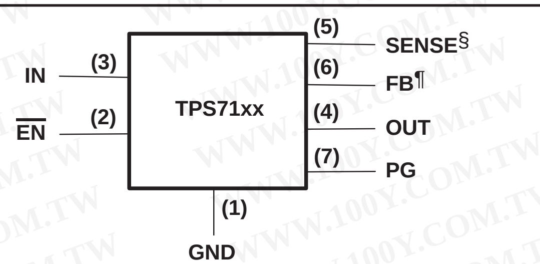
Figure 2. Typical Application Configuration

TPS71xx chip information

These chips, when properly assembled, display characteristics similar to the TPS71xxQ. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. The chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 MILS TYPICAL

BONDING PADS: 4 × 4 MILS MINIMUM

$T_J$max = 150°C

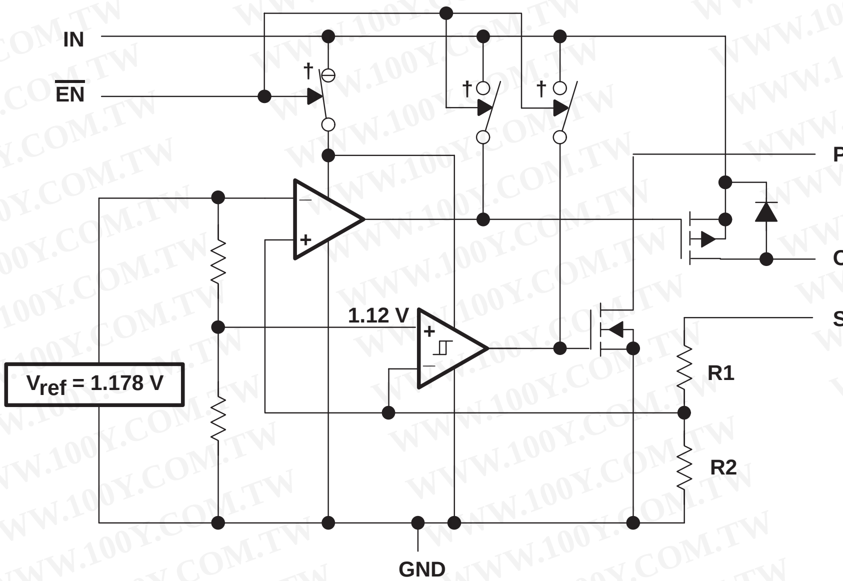
TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

§ SENSE – Fixed voltage options only (TPS7133, TPS7148, and TPS7150)
¶ FB – Adjustable version only (TPS7101)

NOTE A: For most applications, OUT and SENSE should be tied together as close as possible to the device; for other implementations, refer to SENSE-pin connection discussion in the Applications Information section of this data sheet.

functional block diagram



RESISTOR DIVIDER OPTIONS

DEVICE	R1	R2	UNIT
TPS7101	0	∞	Ω
TPS7133	420	233	kΩ
TPS7148	726	233	kΩ
TPS7150	756	233	kΩ

NOTE A: Resistors are nominal values only.

COMPONENT COUNT	
MOS transistors	464
Bilpolar transistors	41
Diodes	4
Capacitors	17
Resistors	76

† Switch positions are shown with EN low (active).
‡ For most applications, SENSE should be externally connected to OUT as close as possible to the device. For other implementations, refer to SENSE-pin connection discussion in Applications Information section.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)§

Input voltage range¶, V_I, PG, SENSE, EN	–0.3 V to 11 V
Output current, I_O	2 A
Continuous total power dissipation	See Dissipation Rating Tables 1 and 2
Operating virtual junction temperature range, T_J	–55°C to 150°C
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

§ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
¶ All voltage values are with respect to network terminal ground.

DISSIPATION RATING TABLE 1 – FREE-AIR TEMPERATURE (see Figure 3)#

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	145 mW
P	1175 mW	9.4 mW/°C	752 mW	235 mW
PW‖	700 mW	5.6 mW/°C	448 mW	140 mW

DISSIPATION RATING TABLE 2 – CASE TEMPERATURE (see Figure 4)#

PACKAGE	$T_C \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_C = 25°C$	$T_C = 70°C$ POWER RATING	$T_C = 125°C$ POWER RATING
D	2188 mW	17.5 mW/°C	1400 mW	438 mW
P	2738 mW	21.9 mW/°C	1752 mW	548 mW
PW‖	4025 mW	32.2 mW/°C	2576 mW	805 mW

Dissipation rating tables and figures are provided for maintenance of junction temperature at or below absolute maximum temperature of 150°C. For guidelines on maintaining junction temperature within recommended operating range, see the Thermal Information section.
‖ Refer to Thermal Information section for detailed power dissipation considerations when using the TSSOP packages.

DISSIPATION DERATING CURVE†
vs
FREE-AIR TEMPERATURE

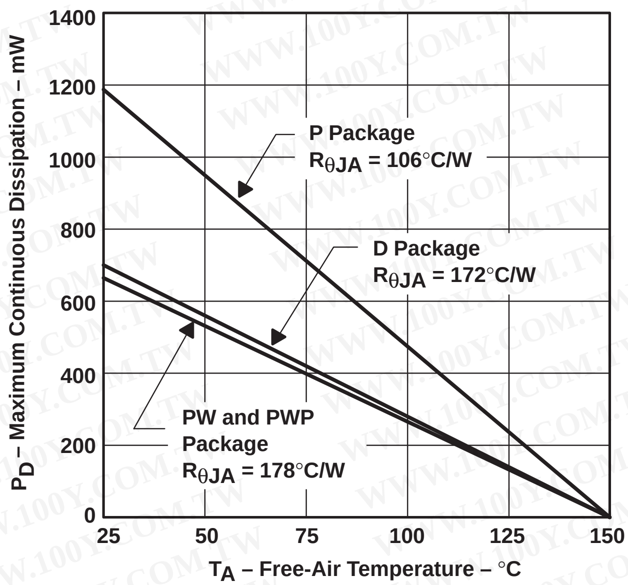


Figure 3

DISSIPATION DERATING CURVE†
vs
CASE TEMPERATURE

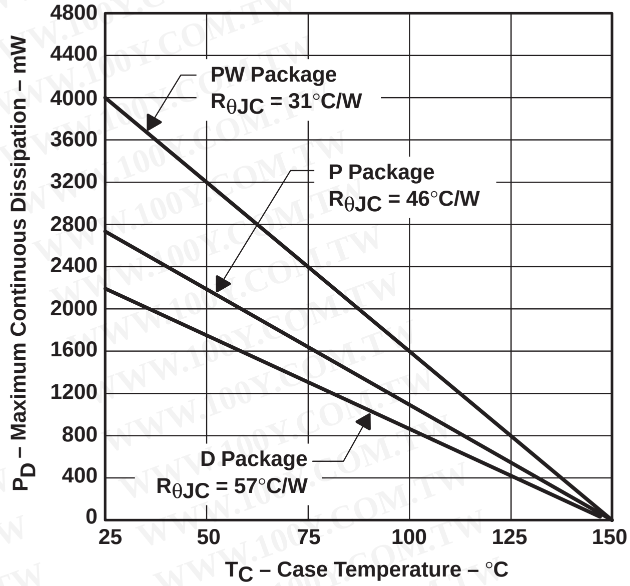


Figure 4

† Dissipation rating tables and figures are provided for maintenance of junction temperature at or below absolute maximum temperature of 150°C. For guidelines on maintaining junction temperature within recommended operating range, see the Thermal Information section.

recommended operating conditions

		MIN	MAX	UNIT
Input voltage, V_I‡	TPS7101Q	2.5	10	V
	TPS7133Q	3.77	10	
	TPS7148Q	5.2	10	
	TPS7150Q	5.33	10	
High-level input voltage at $\overline{EN}$, V_{IH}		2		V
Low-level input voltage at $\overline{EN}$, V_{IL}			0.5	V
Output current range, I_O		0	500	mA
Operating virtual junction temperature range, T_J		–40	125	°C

‡ Minimum input voltage defined in the recommended operating conditions is the maximum specified output voltage plus dropout voltage at the maximum specified load range. Since dropout voltage is a function of output current, the usable range can be extended for lighter loads. To calculate the minimum input voltage for your maximum output current, use the following equation: $V_{I(min)} = V_{O(max)} + V_{DO(max\ load)}$. Because the TPS7101 is programmable, $r_{DS(on)}$ should be used to calculate V_{DO} before applying the above equation. The equation for calculating V_{DO} from $r_{DS(on)}$ is given in Note 2 in the electrical characteristics table. The minimum value of 2.5 V is the absolute lower limit for the recommended input voltage range for the TPS7101.

electrical characteristics at I_O = 10 mA, $\overline{EN}$ = 0 V, C_O = 4.7 μF/CSR† = 1 Ω, SENSE/FB shorted to OUT (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡	T_J	TPS7101Q, TPS7133Q TPS7148Q, TPS7150Q MIN	TYP	MAX	UNIT
Ground current (active mode)	$\overline{EN}$ ≤ 0.5 V, $V_I = V_O + 1$ V, 0 mA ≤ I_O ≤ 500 mA	25°C		285	350	μA
		–40°C to 125°C			460	
Input current (standby mode)	$\overline{EN} = V_I$, 2.7 V ≤ V_I ≤ 10 V	25°C			0.5	μA
		–40°C to 125°C			2	
Output current limit	V_O = 0, V_I = 10 V	25°C		1.2	2	A
		–40°C to 125°C			2	
Pass-element leakage current in standby mode	$\overline{EN} = V_I$, 2.7 V ≤ V_I ≤ 10 V	25°C			0.5	μA
		–40°C to 125°C			1	
PG leakage current	Normal operation, V_{PG} = 10 V	25°C		0.02	0.5	μA
		–40°C to 125°C			0.5	
Output voltage temperature coefficient		–40°C to 125°C		61	75	ppm/°C
Thermal shutdown junction temperature				165		°C
$\overline{EN}$ logic high (standby mode)	2.5 V ≤ V_I ≤ 6 V	–40°C to 125°C	2			V
	6 V ≤ V_I ≤ 10 V		2.7			
$\overline{EN}$ logic low (active mode)	2.7 V ≤ V_I ≤ 10 V	25°C			0.5	V
		–40°C to 125°C			0.5	
$\overline{EN}$ hysteresis voltage		25°C		50		mV
$\overline{EN}$ input current	0 V ≤ V_I ≤ 10 V 0 V ≤ V_I ≤ 10 V	25°C	–0.5		0.5	μA
		–40°C to 125°C	–0.5		0.5	
Minimum V_I for active pass element		25°C		2.05	2.5	V
		–40°C to 125°C			2.5	
Minimum V_I for valid PG	I_{PG} = 300 μA I_{PG} = 300 μA	25°C		1.06	1.5	V
		–40°C to 125°C			1.9	

† CSR (compensation series resistance) refers to the total series resistance, including the equivalent series resistance (ESR) of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.
‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

TPS7101 electrical characteristics at I_O = 10 mA, V_I = 3.5 V, $\overline{EN}$ = 0 V, C_O = 4.7 µF/CSR† = 1 Ω, FB shorted to OUT at device leads (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡		T_J	TPS7101Q MIN	TPS7101Q TYP	TPS7101Q MAX	UNIT
Reference voltage (measured at FB with OUT connected to FB)	V_I = 3.5 V,	I_O = 10 mA	25°C		1.178		V
	2.5 V ≤ V_I ≤ 10 V, See Note 1	5 mA ≤ I_O ≤ 500 mA,	−40°C to 125°C	1.143		1.213	V
Reference voltage temperature coefficient			−40°C to 125°C		61	75	ppm/°C
Pass-element series resistance (see Note 2)	V_I = 2.4 V,	50 µA ≤ I_O ≤ 150 mA	25°C		0.7	1	Ω
			−40°C to 125°C			1	
	V_I = 2.4 V,	150 mA ≤ I_O ≤ 500 mA	25°C		0.83	1.3	
			−40°C to 125°C			1.3	
	V_I = 2.9 V,	50 µA ≤ I_O ≤ 500 mA	25°C		0.52	0.85	
			−40°C to 125°C			0.85	
	V_I = 3.9 V,	50 µA ≤ I_O ≤ 500 mA	25°C		0.32		
	V_I = 5.9 V,	50 µA ≤ I_O ≤ 500 mA	25°C		0.23		
Input regulation	V_I = 2.5 V to 10 V, See Note 1	50 µA ≤ I_O ≤ 500 mA,	25°C			18	mV
			−40°C to 125°C			25	
Output regulation	I_O = 5 mA to 500 mA, See Note 1	2.5 V ≤ V_I ≤ 10 V,	25°C			14	mV
			−40°C to 125°C			25	
	I_O = 50 µA to 500 mA, See Note 1	2.5 V ≤ V_I ≤ 10 V,	25°C			22	mV
			−40°C to 125°C			54	
Ripple rejection	f = 120 Hz	I_O = 50 µA	25°C	48	59		dB
			−40°C to 125°C	44			
		I_O = 500 mA, See Note 1	25°C	45	54		
			−40°C to 125°C	44			
Output noise-spectral density	f = 120 Hz		25°C		2		µV/√Hz
Output noise voltage	10 Hz ≤ f ≤ 100 kHz, CSR† = 1 Ω	C_O = 4.7 µF	25°C		95		µVrms
		C_O = 10 µF	25°C		89		
		C_O = 100 µF	25°C		74		
PG trip-threshold voltage§	V_{FB} voltage decreasing from above V_{PG}		−40°C to 125°C	1.101		1.145	V
PG hysteresis voltage§	Measured at V_{FB}		25°C		12		mV
PG output low voltage§	I_{PG} = 400 µA,	V_I = 2.13 V	25°C		0.1	0.4	V
			−40°C to 125°C			0.4	
FB input current			25°C	−10	0.1	10	nA
			−40°C to 125°C	−20		20	

† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.
‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.
§ Output voltage programmed to 2.5 V with closed-loop configuration (see application information).

NOTES: 1. When V_I < 2.9 V and I_O > 150 mA simultaneously, pass element $r_{DS(on)}$ increases (see Figure 27) to a point such that the resulting dropout voltage prevents the regulator from maintaining the specified tolerance range.

2. To calculate dropout voltage, use equation:

$$V_{DO} = I_O \cdot r_{DS(on)}$$

$r_{DS(on)}$ is a function of both output current and input voltage. The parametric table lists $r_{DS(on)}$ for V_I = 2.4 V, 2.9 V, 3.9 V, and 5.9 V, which corresponds to dropout conditions for programmed output voltages of 2.5 V, 3 V, 4 V, and 6 V, respectively. For other programmed values, refer to Figure 26.

TPS7133 electrical characteristics at I_O = 10 mA, V_I = 4.3 V, $\overline{EN}$ = 0 V, C_O = 4.7 µF/CSR† = 1 Ω, SENSE shorted to OUT (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡		T_J	TPS7133Q MIN	TPS7133Q TYP	TPS7133Q MAX	UNIT
Output voltage	V_I = 4.3 V,	I_O = 10 mA	25°C		3.3		V
	4.3 V ≤ V_I ≤ 10 V,	5 mA ≤ I_O ≤ 500 mA	−40°C to 125°C	3.23		3.37	
Dropout voltage	I_O = 10 mA,	V_I = 3.23 V	25°C		4.5	7	mV
			−40°C to 125°C			8	
	I_O = 100 mA,	V_I = 3.23 V	25°C		47	60	
			−40°C to 125°C			80	
	I_O = 500 mA,	V_I = 3.23 V	25°C		235	300	
			−40°C to 125°C			400	
Pass-element series resistance	(3.23 V – V_O)/I_O, I_O = 500 mA	V_I = 3.23 V,	25°C		0.47	0.6	Ω
			−40°C to 125°C			0.8	
Input regulation	V_I = 4.3 V to 10 V,	50 µA ≤ I_O ≤ 500 mA	25°C			20	mV
			−40°C to 125°C			27	
Output regulation	I_O = 5 mA to 500 mA,	4.3 V ≤ V_I ≤ 10 V	25°C		21	38	mV
			−40°C to 125°C			75	
	I_O = 50 µA to 500 mA,	4.3 V ≤ V_I ≤ 10 V	25°C		30	60	mV
			−40°C to 125°C			120	
Ripple rejection	f = 120 Hz	I_O = 50 µA	25°C	43	54		dB
			−40°C to 125°C	40			
		I_O = 500 mA	25°C	39	49		
			−40°C to 125°C	36			
Output noise-spectral density	f = 120 Hz		25°C		2		µV/√Hz
Output noise voltage	10 Hz ≤ f ≤ 100 kHz, CSR† = 1 Ω	C_O = 4.7 µF	25°C		274		µVrms
		C_O = 10 µF	25°C		228		
		C_O = 100 µF	25°C		159		
PG trip-threshold voltage	V_O voltage decreasing from above V_{PG}		−40°C to 125°C	2.868		3	V
PG hysteresis voltage			25°C		35		mV
PG output low voltage	I_{PG} = 1 mA,	V_I = 2.8 V	25°C		0.22	0.4	V
			−40°C to 125°C			0.4	

† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.
‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

TPS7148 electrical characteristics at $I_O = 10$ mA, $V_I = 5.85$ V, $\overline{EN} = 0$ V, $C_O = 4.7$ µF/CSR† = 1 Ω, SENSE shorted to OUT (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡		T_J	TPS7148Q MIN	TPS7148Q TYP	TPS7148Q MAX	UNIT
Output voltage	$V_I = 5.85$ V,	$I_O = 10$ mA	25°C		4.85		V
	5.85 V ≤ V_I ≤ 10 V,	5 mA ≤ I_O ≤ 500 mA	–40°C to 125°C	4.75		4.95	
Dropout voltage	$I_O = 10$ mA,	$V_I = 4.75$ V	25°C		2.9	6	mV
			–40°C to 125°C			8	
	$I_O = 100$ mA,	$V_I = 4.75$ V	25°C		30	37	
			–40°C to 125°C			54	
	$I_O = 500$ mA,	$V_I = 4.75$ V	25°C		150	180	
			–40°C to 125°C			250	
Pass-element series resistance	$(4.75\ V - V_O)/I_O$, $I_O = 500$ mA	$V_I = 4.75$ V,	25°C		0.32	0.35	Ω
			–40°C to 125°C			0.52	
Input regulation	$V_I = 5.85$ V to 10 V,	50 µA ≤ I_O ≤ 500 mA	25°C			27	mV
			–40°C to 125°C			37	
Output regulation	$I_O = 5$ mA to 500 mA,	5.85 V ≤ V_I ≤ 10 V	25°C		12	42	mV
			–40°C to 125°C			80	
	$I_O = 50$ µA to 500 mA,	5.85 V ≤ V_I ≤ 10 V	25°C		42	60	mV
			–40°C to 125°C			130	
Ripple rejection	f = 120 Hz	$I_O = 50$ µA	25°C	42	53		dB
			–40°C to 125°C	39			
		$I_O = 500$ mA	25°C	39	50		
			–40°C to 125°C	35			
Output noise-spectral density	f = 120 Hz		25°C		2		µV/√Hz
Output noise voltage	10 Hz ≤ f ≤ 100 kHz, CSR† = 1 Ω	$C_O = 4.7$ µF	25°C		410		µVrms
		$C_O = 10$ µF	25°C		328		
		$C_O = 100$ µF	25°C		212		
PG trip-threshold voltage	V_O voltage decreasing from above V_{PG}		–40°C to 125°C	4.5		4.7	V
PG hysteresis voltage			25°C		50		mV
PG output low voltage	$I_{PG} = 1.2$ mA,	$V_I = 4.12$ V	25°C		0.2	0.4	V
			–40°C to 125°C			0.4	

† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.
‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

TPS7150 electrical characteristics at I_O = 10 mA, V_I = 6 V, $\overline{EN}$ = 0 V, C_O = 4.7 μF/CSR† = 1 Ω, SENSE shorted to OUT (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡		T_J	TPS7150Q MIN	TPS7150Q TYP	TPS7150Q MAX	UNIT
Output voltage	V_I = 6 V,	I_O = 10 mA	25°C		5		V
	6 V ≤ V_I ≤ 10 V,	5 mA ≤ I_O ≤ 500 mA	–40°C to 125°C	4.9		5.1	
Dropout voltage	I_O = 10 mA,	V_I = 4.88 V	25°C		2.9	6	mV
			–40°C to 125°C			8	
	I_O = 100 mA,	V_I = 4.88 V	25°C		27	32	
			–40°C to 125°C			47	
	I_O = 500 mA,	V_I = 4.88 V	25°C		146	170	
			–40°C to 125°C			230	
Pass-element series resistance	(4.88 V – V_O)/I_O, I_O = 500 mA	V_I = 4.88 V,	25°C		0.29	0.32	Ω
			–40°C to 125°C			0.47	
Input regulation	V_I = 6 V to 10 V,	50 μA ≤ I_O ≤ 500 mA	25°C			25	mV
			–40°C to 125°C			32	
Output regulation	I_O = 5 mA to 500 mA,	6 V ≤ V_I ≤ 10 V	25°C		30	45	mV
			–40°C to 125°C			86	
	I_O = 50 μA to 500 mA,	6 V ≤ V_I ≤ 10 V	25°C		45	65	mV
			–40°C to 125°C			140	
Ripple rejection	f = 120 Hz	I_O = 50 μA	25°C	45	55		dB
			–40°C to 125°C	40			
		I_O = 500 mA	25°C	42	52		
			–40°C to 125°C	36			
Output noise-spectral density	f = 120 Hz		25°C		2		$\mu V/\sqrt{Hz}$
Output noise voltage	10 Hz ≤ f ≤ 100 kHz, CSR† = 1 Ω	C_O = 4.7 μF	25°C		430		μVrms
		C_O = 10 μF	25°C		345		
		C_O = 100 μF	25°C		220		
PG trip-threshold voltage	V_O voltage decreasing from above V_{PG}		–40°C to 125°C	4.55		4.75	V
PG hysteresis voltage			25°C		53		mV
PG output low voltage	I_{PG} = 1.2 mA,	V_I = 4.25 V	25°C		0.2	0.4	V
			–40°C to 125°C			0.4	

† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.
‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

electrical characteristics at I_O = 10 mA, $\overline{EN}$ = 0 V, C_O = 4.7 μF/CSR† = 1 Ω, T_J = 25°C, SENSE/FB shorted to OUT (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡		TPS7101Y, TPS7133Y TPS7148Y, TPS7150Y MIN	TYP	MAX	UNIT
Ground current (active mode)	$\overline{EN}$ ≤ 0.5 V, 0 mA ≤ I_O ≤ 500 mA	$V_I = V_O + 1$ V,		285		μA
Output current limit	V_O = 0,	V_I = 10 V		1.2		A
PG leakage current	Normal operation,	V_{PG} = 10 V		0.02		μA
Thermal shutdown junction temperature				165		°C
$\overline{EN}$ hysteresis voltage				50		mV
Minimum V_I for active pass element				2.05		V
Minimum V_I for valid PG	I_{PG} = 300 μA			1.06		V

PARAMETER	TEST CONDITIONS‡		TPS7101Y MIN	TYP	MAX	UNIT
Reference voltage (measured at FB with OUT connected to FB)	V_I = 3.5 V,	I_O = 10 mA		1.178		V
Pass-element series resistance (see Note 2)	V_I = 2.4 V,	50 μA ≤ I_O ≤ 150 mA		0.7		Ω
	V_I = 2.4 V,	150 mA ≤ I_O ≤ 500 mA		0.83		
	V_I = 2.9 V,	50 μA ≤ I_O ≤ 500 mA		0.52		
	V_I = 3.9 V,	50 μA ≤ I_O ≤ 500 mA		0.32		
	V_I = 5.9 V,	50 μA ≤ I_O ≤ 500 mA		0.23		
Input regulation	V_I = 2.5 V to 10 V, See Note 1	50 μA ≤ I_O ≤ 500 mA,			18	mV
Output regulation	2.5 V ≤ V_I ≤ 10 V, See Note 1	I_O = 5 mA to 500 mA,			14	mV
	2.5 V ≤ V_I ≤ 10 V, See Note 1	I_O = 50 μA to 500 mA,			22	mV
Ripple rejection	V_I = 3.5 V, I_O = 50 μA	f = 120 Hz,		59		dB
Output noise-spectral density	V_I = 3.5 V,	f = 120 Hz		2		μV/√Hz
Output noise voltage	V_I = 3.5 V, 10 Hz ≤ f ≤ 100 kHz, CSR† = 1 Ω	C_O = 4.7 μF		95		μVrms
		C_O = 10 μF		89		
		C_O = 100 μF		74		
PG hysteresis voltage§	V_I = 3.5 V,	Measured at V_{FB}		12		mV
PG output low voltage§	V_I = 2.13 V,	I_{PG} = 400 μA		0.1		V
FB input current	V_I = 3.5 V	V_I = 3.5 V		0.1		nA

† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.
‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.
§ Output voltage programmed to 2.5 V with closed-loop configuration (see application information).

NOTES: 1. When V_I < 2.9 V and I_O > 150 mA simultaneously, pass element $r_{DS(on)}$ increases (see Figure 27) to a point such that the resulting dropout voltage prevents the regulator from maintaining the specified tolerance range.

2. To calculate dropout voltage, use equation:

$$V_{DO} = I_O \cdot r_{DS(on)}$$

$r_{DS(on)}$ is a function of both output current and input voltage. The parametric table lists $r_{DS(on)}$ for V_I = 2.4 V, 2.9 V, 3.9 V, and 5.9 V, which corresponds to dropout conditions for programmed output voltages of 2.5 V, 3 V, 4 V, and 6 V, respectively. For other programmed values, refer to Figure 26.

electrical characteristics at I_O = 10 mA, $\overline{EN}$ = 0 V, C_O = 4.7 μF/CSR† = 1 Ω, T_J = 25°C, SENSE shorted to OUT (unless otherwise noted) (continued)

PARAMETER	TEST CONDITIONS‡		TPS7133Y			UNIT
			MIN	TYP	MAX	
Output voltage	V_I = 4.3 V,	I_O = 10 mA		3.3		V
Dropout voltage	V_I = 3.23 V,	I_O = 10 mA		0.02		mV
	V_I = 3.23 V,	I_O = 100 mA		47		
	V_I = 3.23 V,	I_O = 500 mA		235		
Pass-element series resistance	(3.23 V – V_O)/I_O, I_O = 500 mA	V_I = 3.23 V,		0.47		Ω
Output regulation	4.3 V ≤ V_I ≤ 10 V,	I_O = 5 mA to 500 mA		21		mV
	4.3 V ≤ V_I ≤ 10 V,	I_O = 50 μA to 500 mA		30		mV
Ripple rejection	V_I = 4.3 V, f = 120 Hz	I_O = 50 μA		54		dB
		I_O = 500 mA		49		
Output noise-spectral density	V_I = 4.3 V,	f = 120 Hz		2		μV/√Hz
Output noise voltage	V_I = 4.3 V, 10 Hz ≤ f ≤ 100 kHz, CSR† = 1 Ω	C_O = 4.7 μF		274		μVrms
		C_O = 10 μF		228		
		C_O = 100 μF		159		
PG hysteresis voltage	V_I = 4.3 V			35		mV
PG output low voltage	V_I = 2.8 V,	I_{PG} = 1 mA		0.22		V

PARAMETER	TEST CONDITIONS‡		TPS7148Y			UNIT
			MIN	TYP	MAX	
Output voltage	V_I = 5.85 V,	I_O = 10 mA		4.85		V
Dropout voltage	V_I = 4.75 V,	I_O = 10 mA		0.08		mV
	V_I = 4.75 V,	I_O = 100 mA		30		
	V_I = 4.75 V,	I_O = 500 mA		150		
Pass-element series resistance	(4.75 V – V_O)/I_O, I_O = 500 mA	V_I = 4.75 V,		0.32		Ω
Output regulation	5.85 V ≤ V_I ≤ 10 V,	I_O = 5 mA to 500 mA		12		mV
	5.85 V ≤ V_I ≤ 10 V,	I_O = 50 μA to 500 mA		42		mV
Ripple rejection	V_I = 5.85 V, f = 120 Hz	I_O = 50 μA		53		dB
		I_O = 500 mA		50		
Output noise-spectral density	V_I = 5.85 V,	f = 120 Hz		2		μV/√Hz
Output noise voltage	V_I = 5.85 V, 10 Hz ≤ f ≤ 100 kHz, CSR† = 1 Ω	C_O = 4.7 μF		410		μVrms
		C_O = 10 μF		328		
		C_O = 100 μF		212		
PG hysteresis voltage	V_I = 5.85 V			50		mV
PG output low voltage	V_I = 4.12 V,	I_{PG} = 1.2 mA		0.2	0.4	V

† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.
‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

electrical characteristics at I_O = 10 mA, $\overline{EN}$ = 0 V, C_O = 4.7 µF/CSR† = 1 Ω, T_J = 25°C, SENSE shorted to OUT (unless otherwise noted) (continued)

PARAMETER	TEST CONDITIONS‡		TPS7150Y MIN	TPS7150Y TYP	TPS7150Y MAX	UNIT
Output voltage	V_I = 6 V,	I_O = 10 mA		5		V
Dropout voltage	V_I = 4.88 V,	I_O = 10 mA		0.13		mV
	V_I = 4.88 V,	I_O = 100 mA		27		
	V_I = 4.88 V,	I_O = 500 µA		146		
Pass-element series resistance	(4.88 V – V_O)/I_O, I_O = 500 mA	V_I = 4.88 V,		0.29		Ω
Output regulation	6 V ≤ V_I ≤ 10 V,	I_O = 5 mA to 500 mA		30		mV
	6 V ≤ V_I ≤ 10 V,	I_O = 50 µA to 500 mA		45		mV
Ripple rejection	V_I = 6 V, f = 120 Hz	I_O = 50 µA		55		dB
		I_O = 500 mA		52		
Output noise-spectral density	V_I = 6 V,	f = 120 Hz		2		µV/√Hz
Output noise voltage	V_I = 6 V, 10 Hz ≤ f ≤ 100 kHz, CSR† = 1 Ω	C_O = 4.7 µF		430		µVrms
		C_O = 10 µF		345		
		C_O = 100 µF		220		
PG hysteresis voltage	V_I = 6 V			53		mV
PG output low voltage	V_I = 4.25 V,	I_{PG} = 1.2 mA		0.2		V

† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.
‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

TYPICAL CHARACTERISTICS

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TYPICAL CHARACTERISTICS

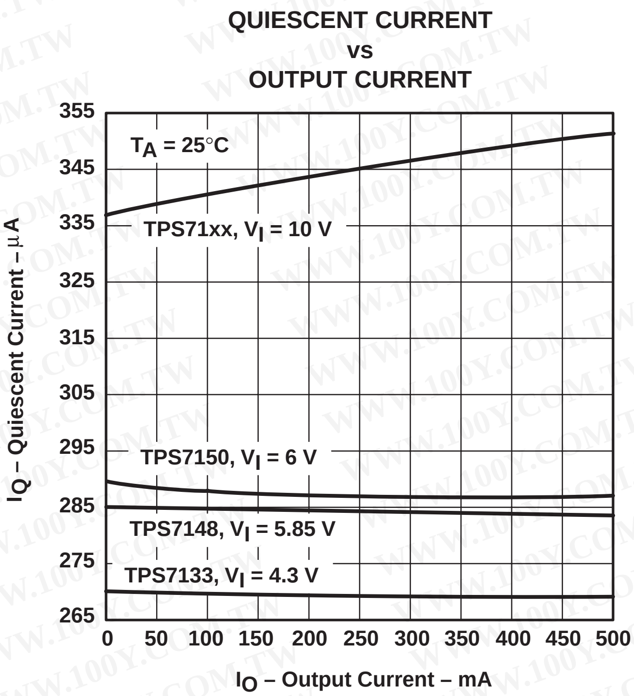


Figure 5

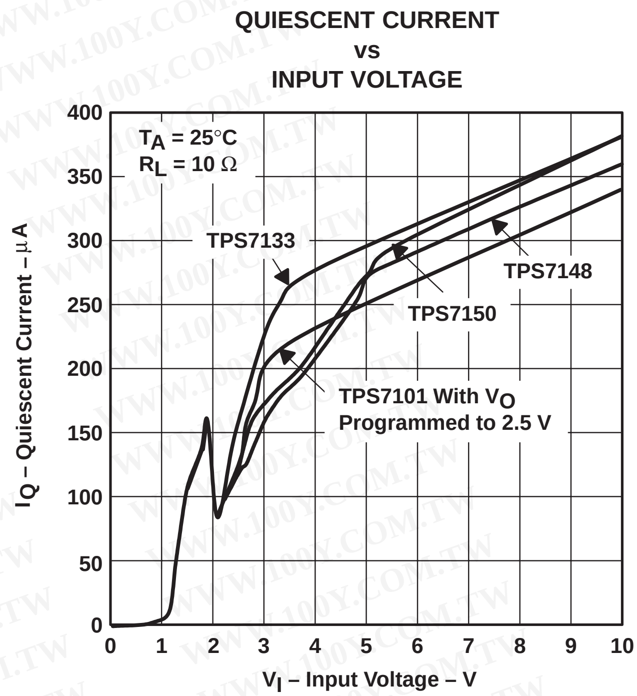


Figure 6

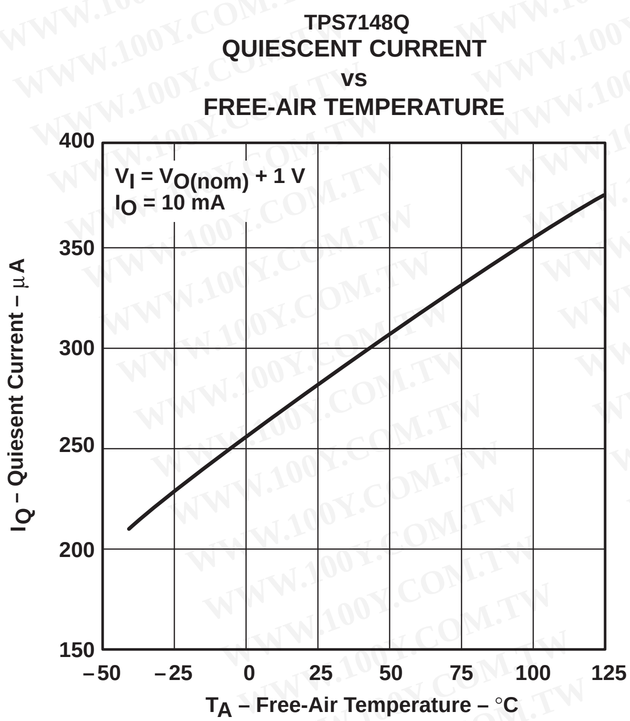


Figure 7

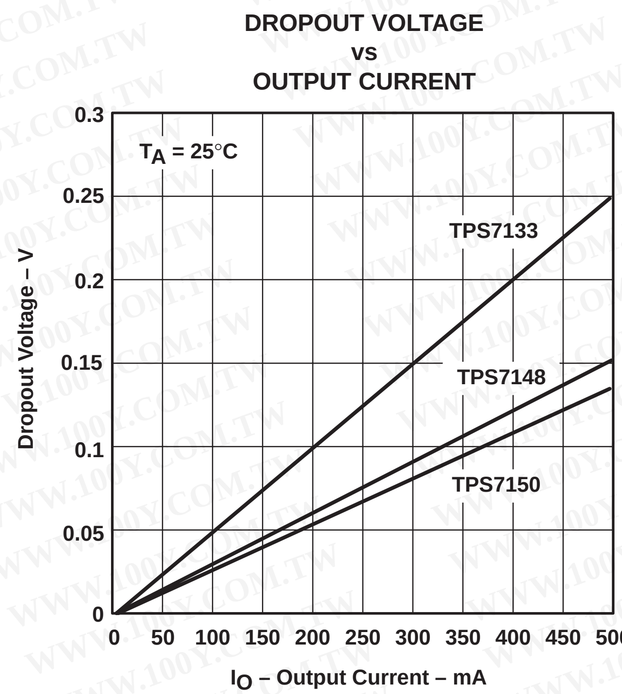


Figure 8

TYPICAL CHARACTERISTICS

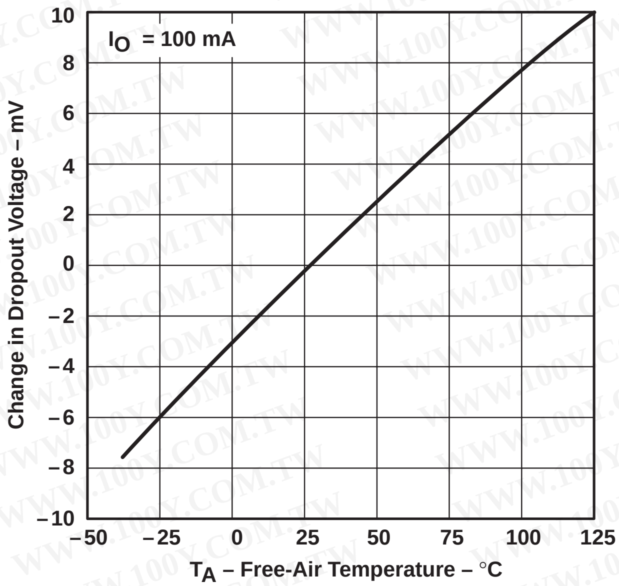


Figure 9

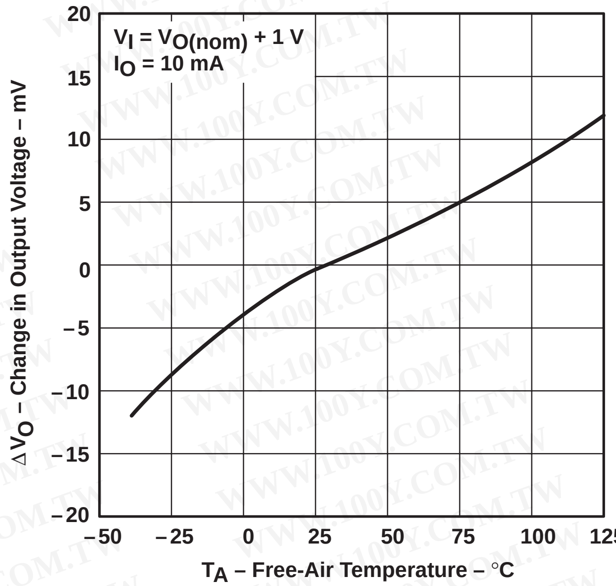


Figure 10

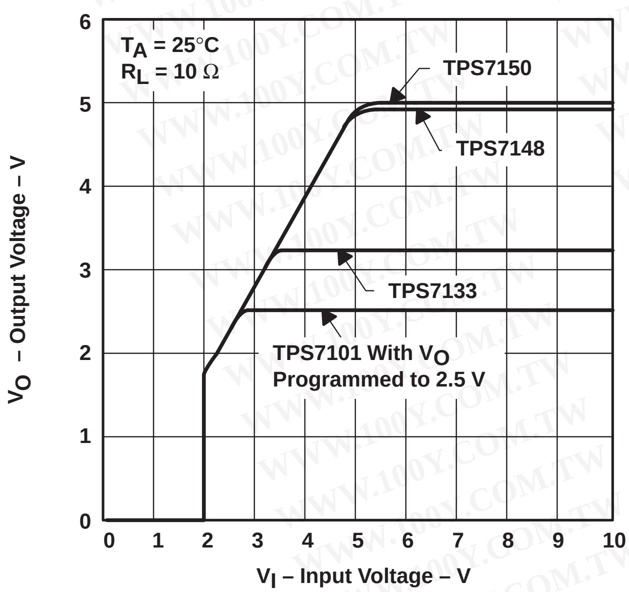


Figure 11

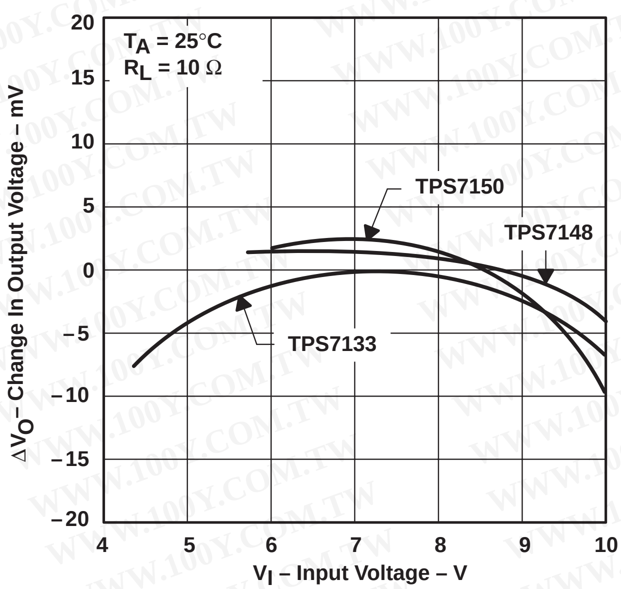


Figure 12

TYPICAL CHARACTERISTICS

TPS7101Q OUTPUT VOLTAGE vs OUTPUT CURRENT

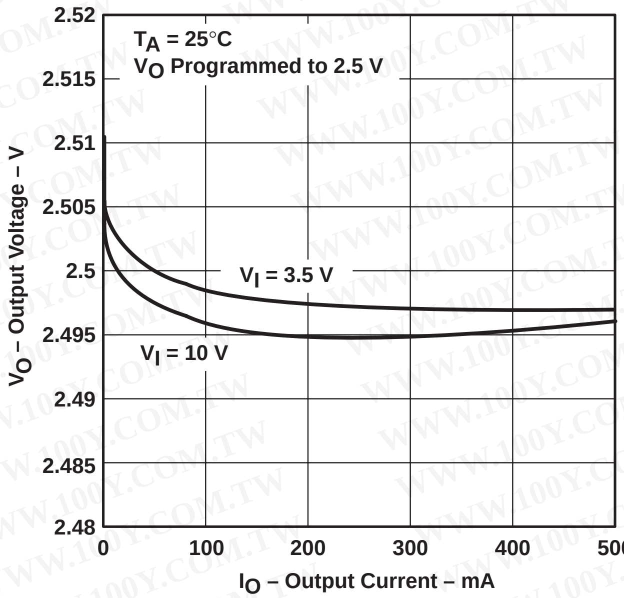


Figure 13

TPS7133Q OUTPUT VOLTAGE vs OUTPUT CURRENT

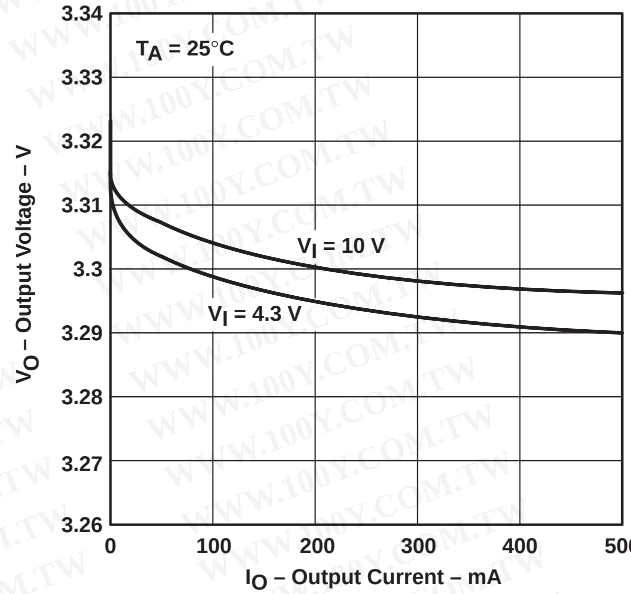


Figure 14

TPS7148Q OUTPUT VOLTAGE vs OUTPUT CURRENT

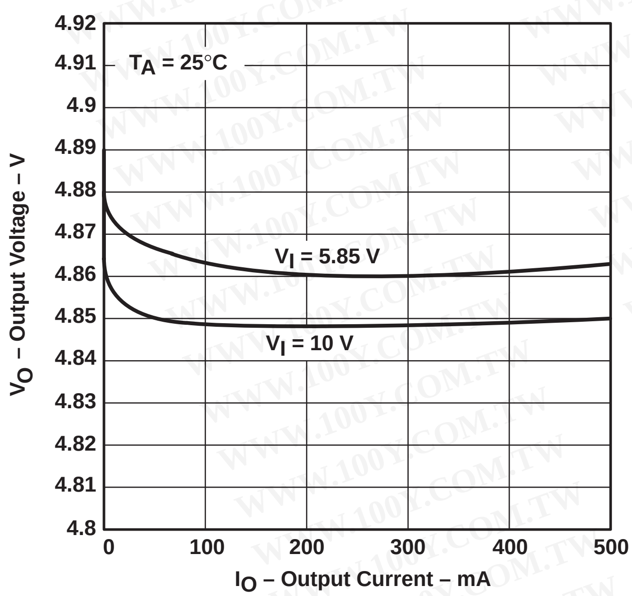


Figure 15

TPS7150Q OUTPUT VOLTAGE vs OUTPUT CURRENT

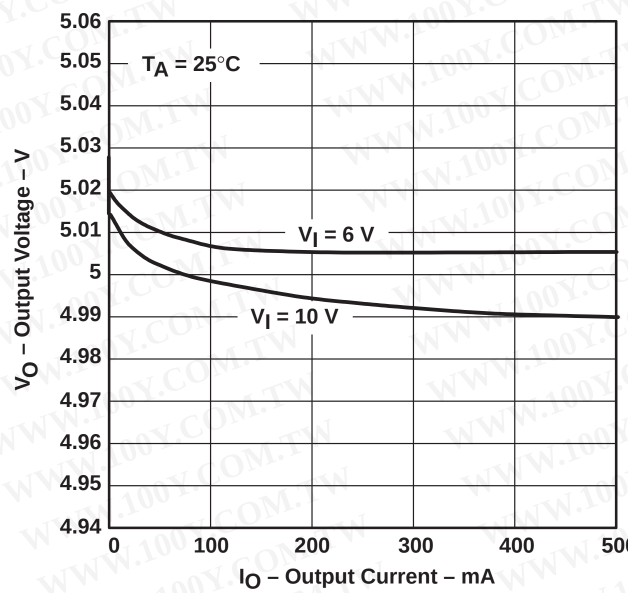


Figure 16

TYPICAL CHARACTERISTICS

TPS7101Q
RIPPLE REJECTION
vs
FREQUENCY

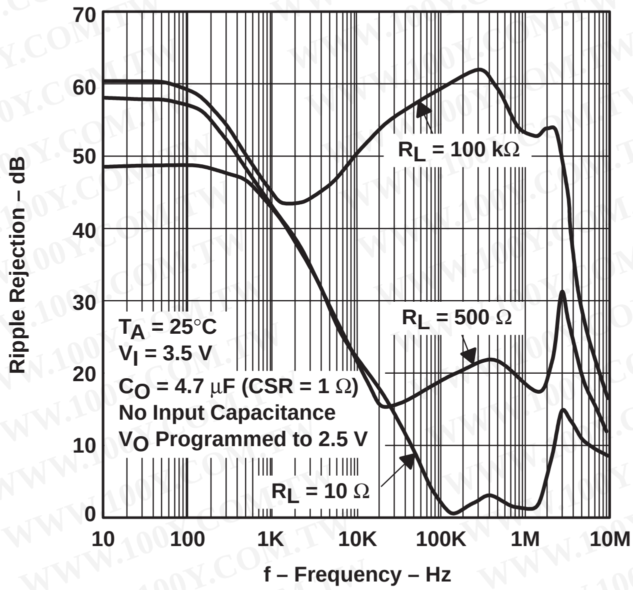


Figure 17

TPS7133Q
RIPPLE REJECTION
vs
FREQUENCY

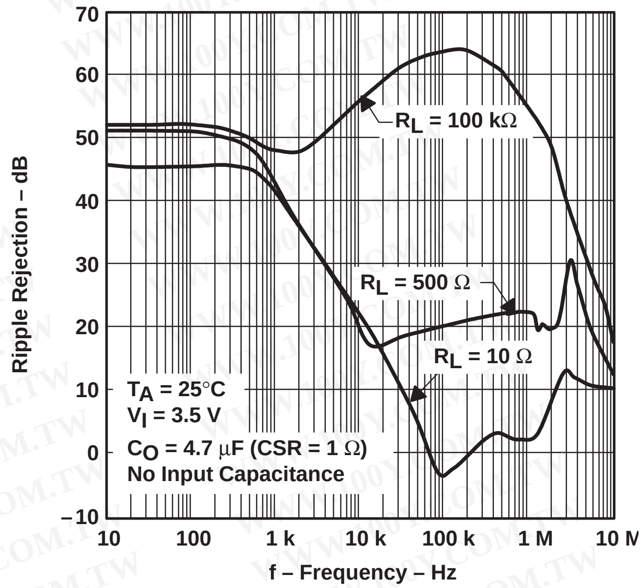


Figure 18

TPS7148Q
RIPPLE REJECTION
vs
FREQUENCY

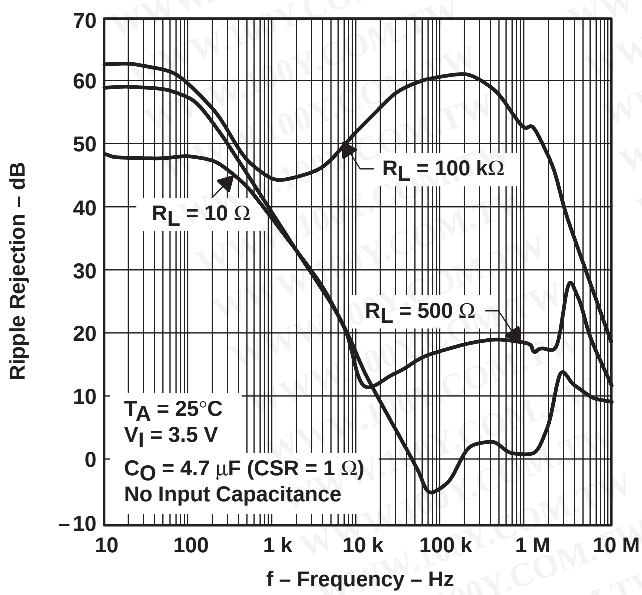


Figure 19

TPS7150Q
RIPPLE REJECTION
vs
FREQUENCY

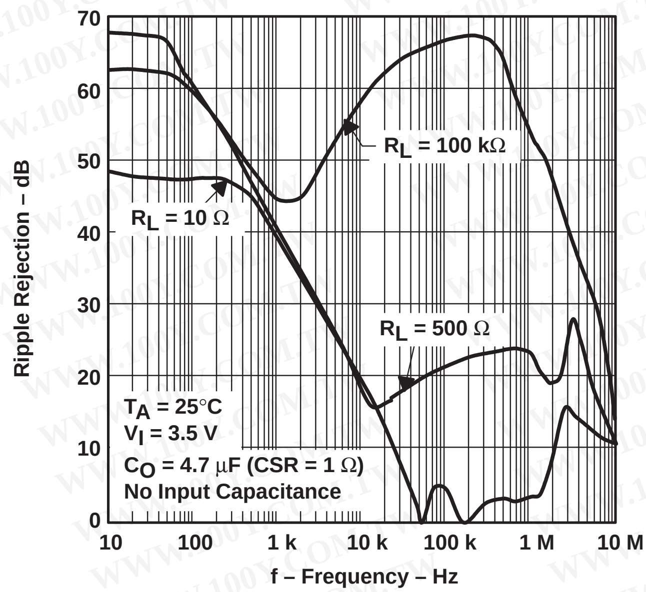


Figure 20

TYPICAL CHARACTERISTICS

TPS7101Q
OUTPUT SPECTRAL NOISE DENSITY
vs
FREQUENCY

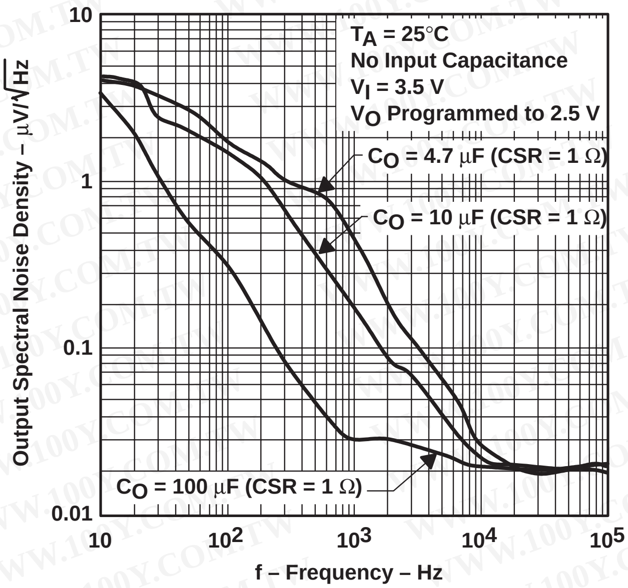


Figure 21

TPS7133Q
OUTPUT SPECTRAL NOISE DENSITY
vs
FREQUENCY

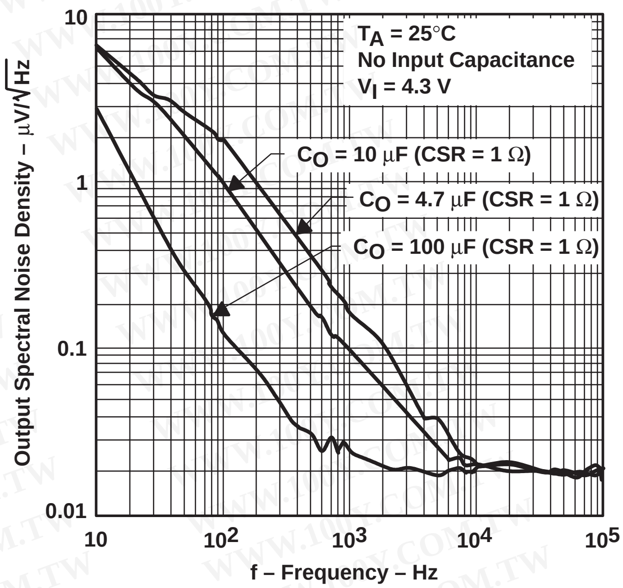


Figure 22

TPS7148Q
OUTPUT SPECTRAL NOISE DENSITY
vs
FREQUENCY

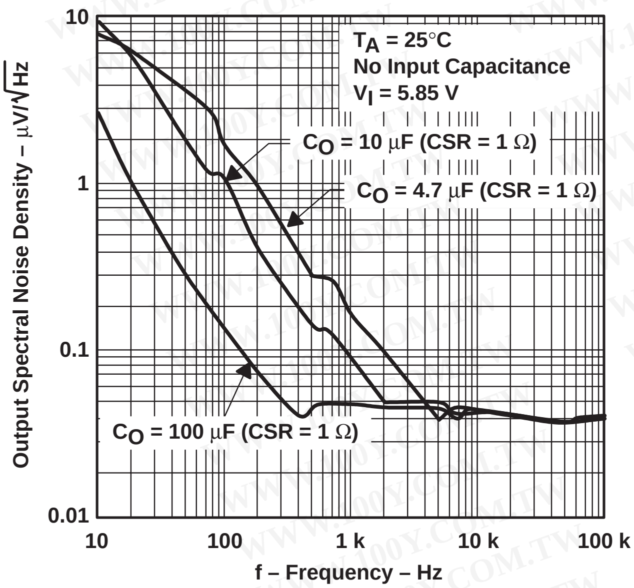


Figure 23

TPS7150Q
OUTPUT SPECTRAL NOISE DENSITY
vs
FREQUENCY

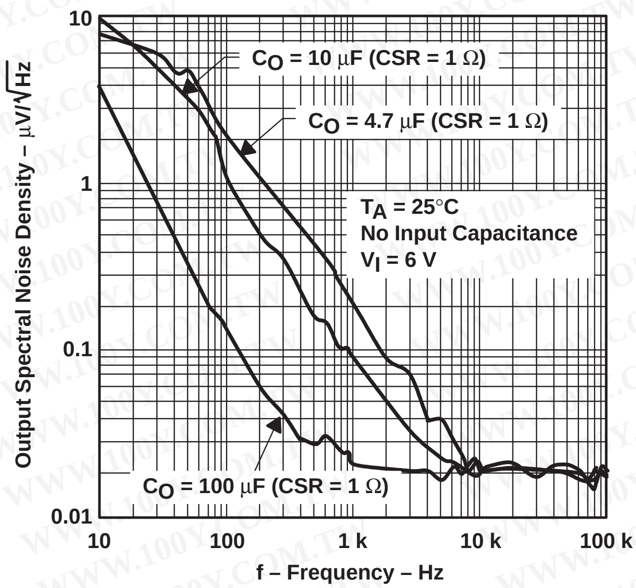


Figure 24

TYPICAL CHARACTERISTICS

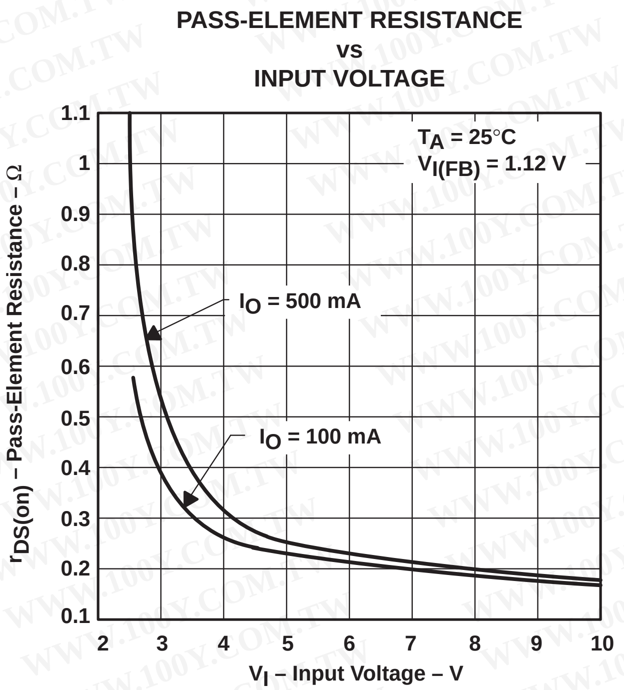


Figure 25

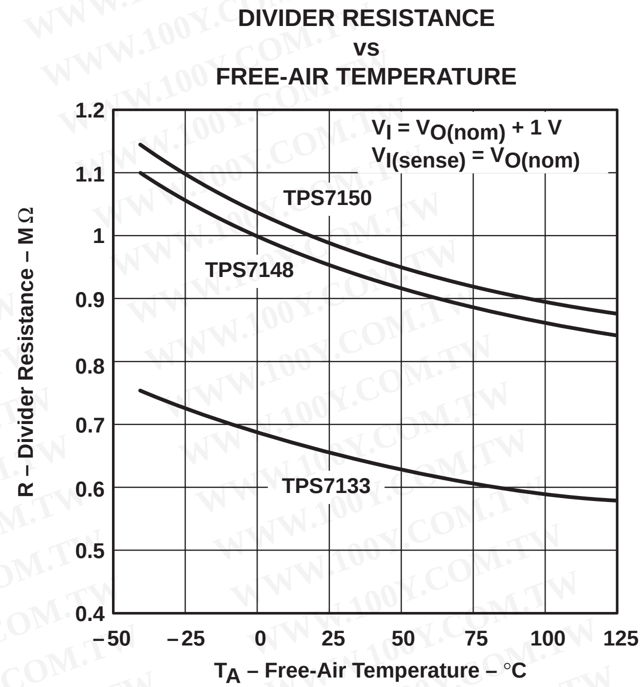


Figure 26

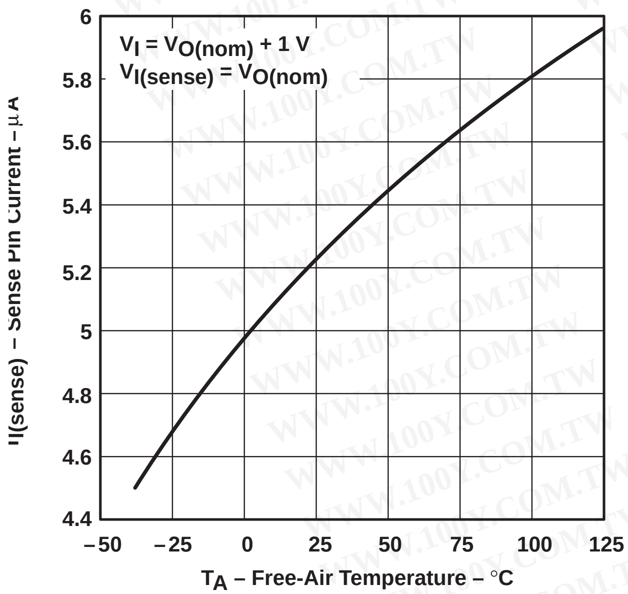


Figure 27

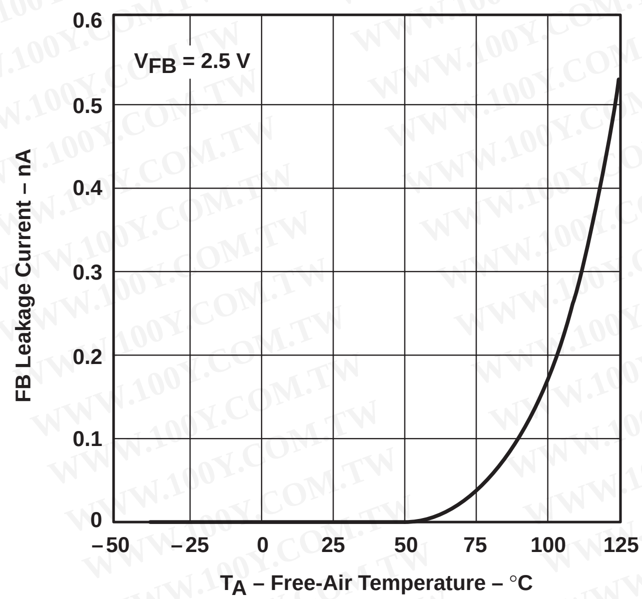


Figure 28

TYPICAL CHARACTERISTICS

MINIMUM INPUT VOLTAGE FOR ACTIVE PASS ELEMENT vs FREE-AIR TEMPERATURE

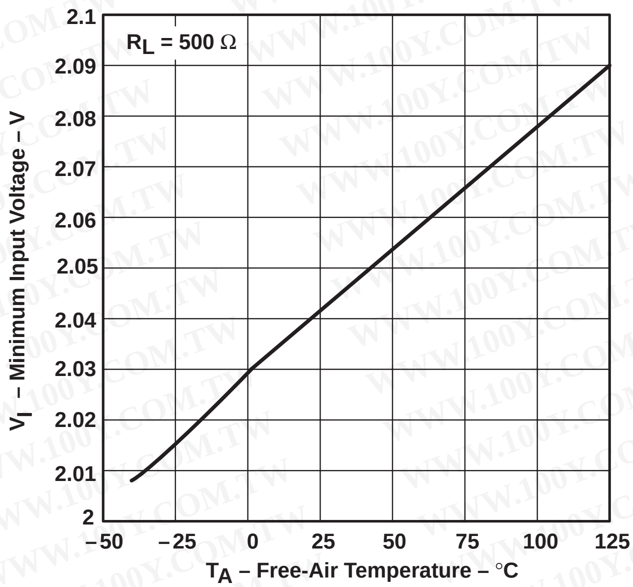


Figure 29

MINIMUM INPUT VOLTAGE FOR VALID POWER GOOD (PG) vs FREE-AIR TEMPERATURE

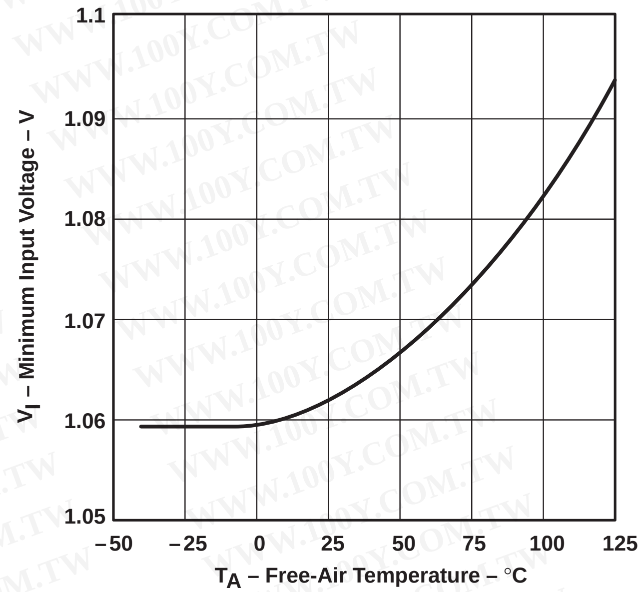


Figure 30

$\overline{EN}$ INPUT CURRENT vs FREE-AIR TEMPERATURE

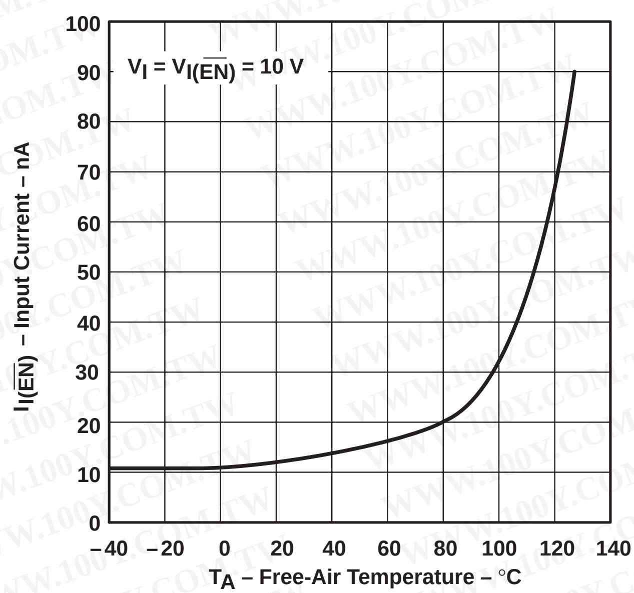


Figure 31

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE RESPONSE FROM ENABLE (EN)

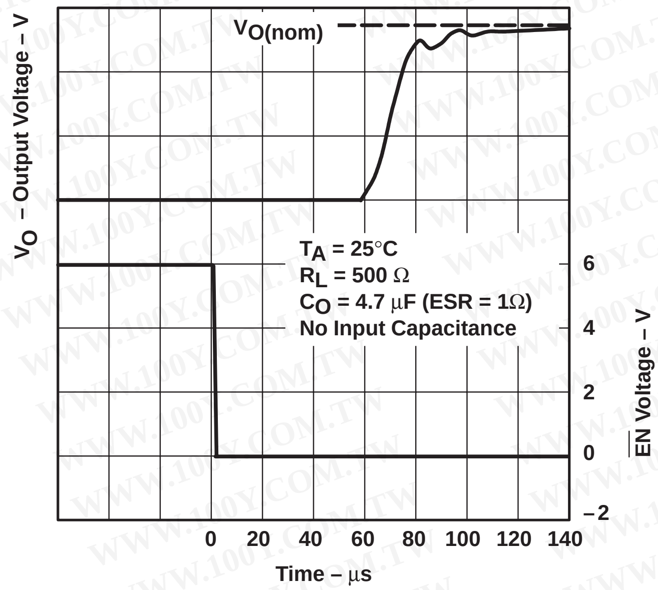


Figure 32

POWER-GOOD (PG) VOLTAGE vs OUTPUT VOLTAGE

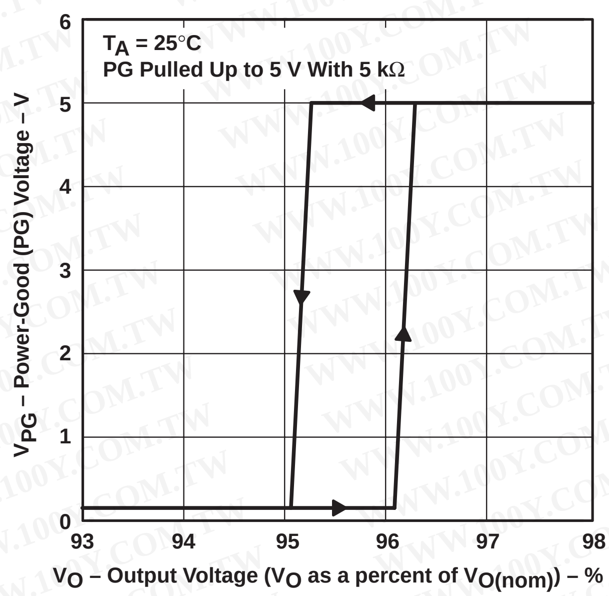


Figure 33

TYPICAL CHARACTERISTICS

TYPICAL REGIONS OF STABILITY
COMPENSATION SERIES RESISTANCE
vs
OUTPUT CURRENT

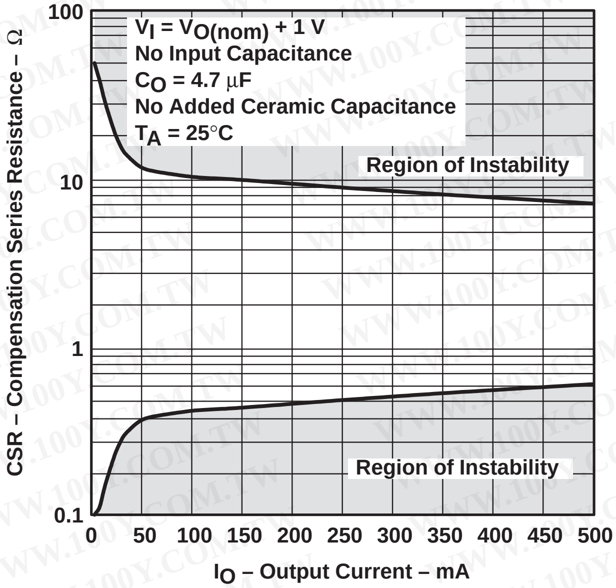


Figure 34

TYPICAL REGIONS OF STABILITY
COMPENSATION SERIES RESISTANCE
vs
OUTPUT CURRENT

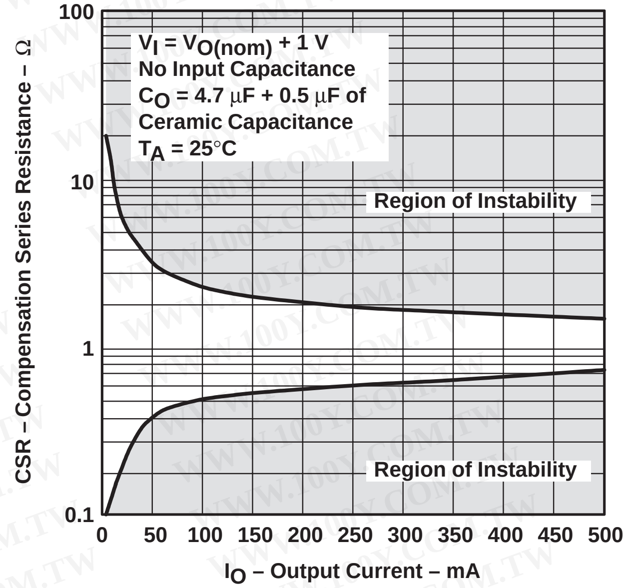


Figure 35

TYPICAL REGIONS OF STABILITY
COMPENSATION SERIES RESISTANCE
vs
ADDED CERAMIC CAPACITANCE

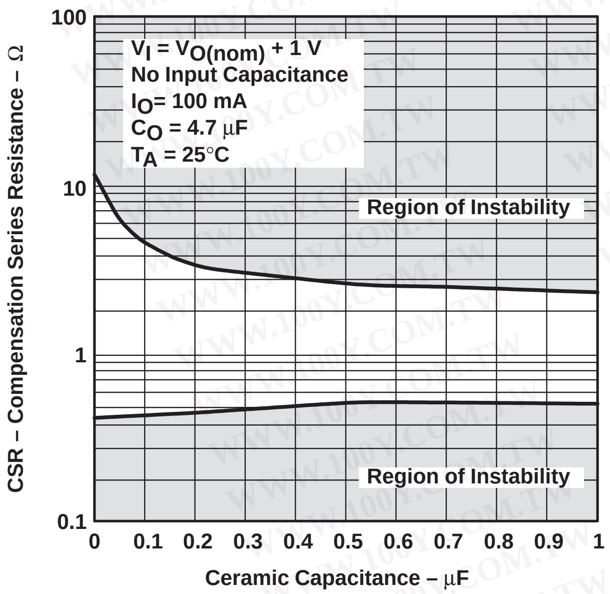


Figure 36

TYPICAL REGIONS OF STABILITY
COMPENSATION SERIES RESISTANCE
vs
ADDED CERAMIC CAPACITANCE

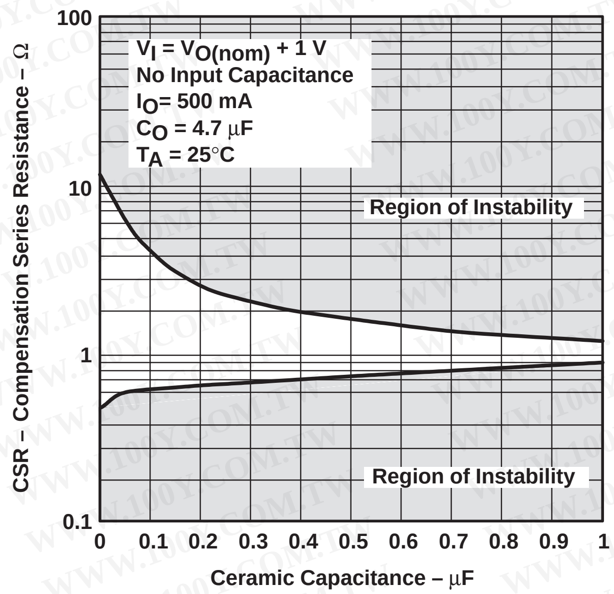


Figure 37

TYPICAL CHARACTERISTICS

TYPICAL REGIONS OF STABILITY†
COMPENSATION SERIES RESISTANCE
vs
OUTPUT CURRENT

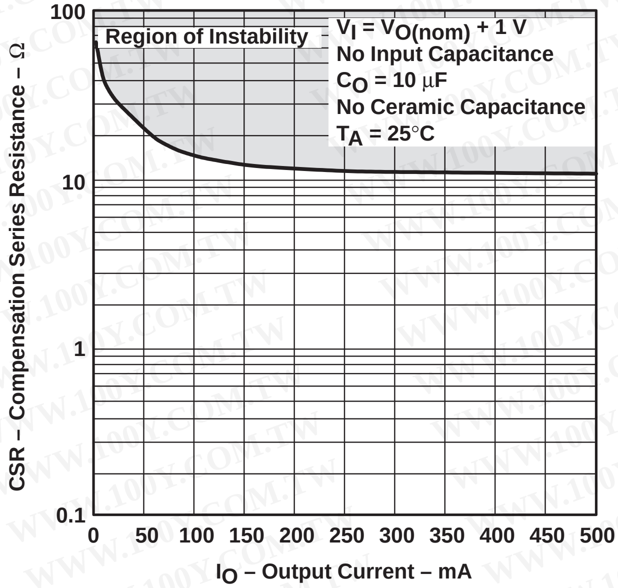


Figure 38

TYPICAL REGIONS OF STABILITY†
COMPENSATION SERIES RESISTANCE
vs
OUTPUT CURRENT

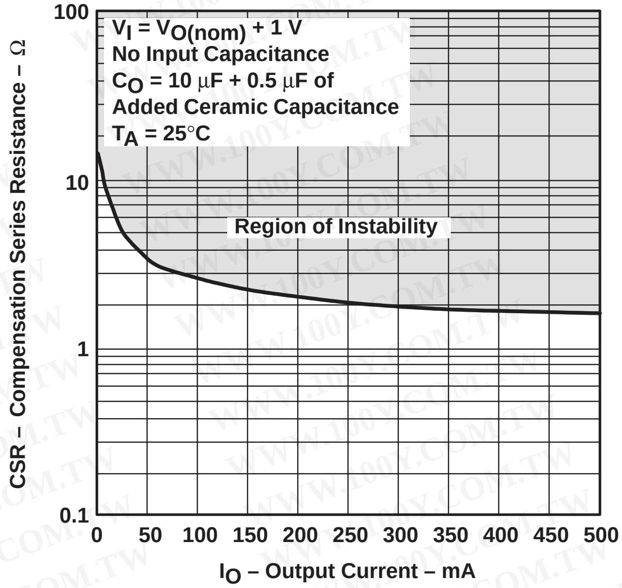


Figure 39

TYPICAL REGIONS OF STABILITY†
COMPENSATION SERIES RESISTANCE
vs
ADDED CERAMIC CAPACITANCE

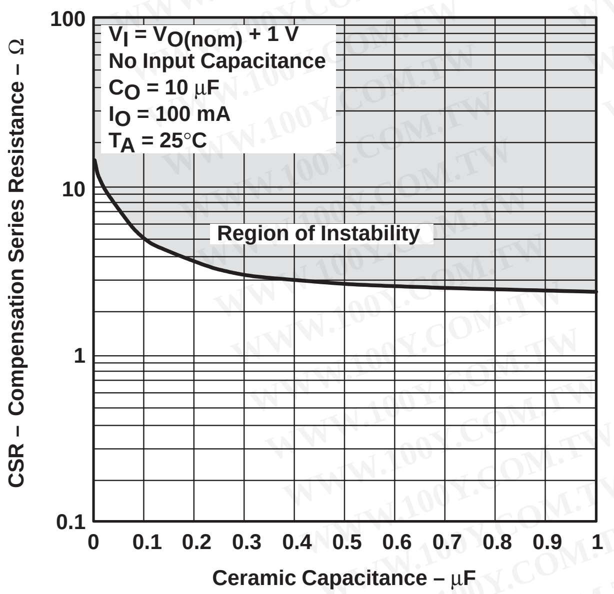


Figure 40

TYPICAL REGIONS OF STABILITY†
COMPENSATION SERIES RESISTANCE
vs
ADDED CERAMIC CAPACITANCE

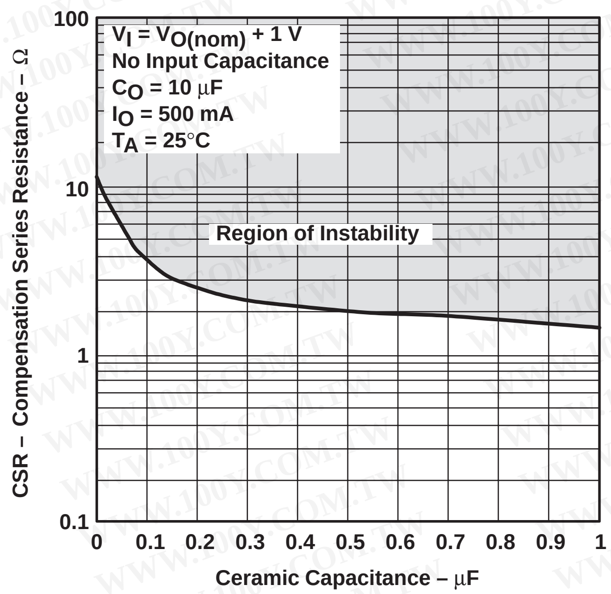
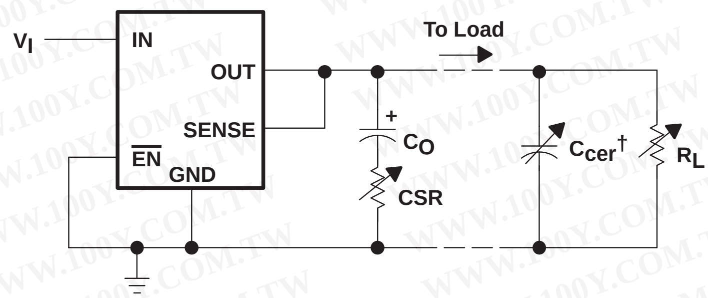


Figure 41

† CSR values below 0.1 Ω are not recommended.

TYPICAL CHARACTERISTICS



† Ceramic capacitor

Figure 42. Test Circuit for Typical Regions of Stability (Figures 34 through 41)

APPLICATION INFORMATION

The TPS71xx series of low-dropout (LDO) regulators is designed to overcome many of the shortcomings of earlier-generation LDOs, while adding features such as a power-saving shutdown mode and a power-good indicator. The TPS71xx family includes three fixed-output voltage regulators: the TPS7133 (3.3 V), the TPS7148 (4.85 V), and the TPS7150 (5 V). The family also offers an adjustable device, the TPS7101 (adjustable from 1.2 V to 9.75 V).

device operation

The TPS71xx, unlike many other LDOs, features very low quiescent currents that remain virtually constant even with varying loads. Conventional LDO regulators use a pnp-pass element, the base current of which is directly proportional to the load current through the regulator ($I_B = I_C/\beta$). Close examination of the data sheets reveals that those devices are typically specified under near no-load conditions; actual operating currents are much higher as evidenced by typical quiescent current versus load current curves. The TPS71xx uses a PMOS transistor to pass current; because the gate of the PMOS element is voltage driven, operating currents are low and invariable over the full load range. The TPS71xx specifications reflect actual performance under load.

Another pitfall associated with the pnp-pass element is its tendency to saturate when the device goes into dropout. The resulting drop in β forces an increase in I_B to maintain the load. During power up, this translates to large start-up currents. Systems with limited supply current may fail to start up. In battery-powered systems, it means rapid battery discharge when the voltage decays below the minimum required for regulation. The TPS71xx quiescent current remains low even when the regulator drops out, eliminating both problems.

Included in the TPS71xx family is a 4.85-V regulator, the TPS7148. Designed specifically for 5-V cellular systems, its 4.85-V output, regulated to within ± 2%, allows for operation within the low-end limit of 5-V systems specified to ± 5% tolerance; therefore, maximum regulated operating lifetime is obtained from a battery pack before the device drops out, adding crucial talk minutes between charges.

The TPS71xx family also features a shutdown mode that places the output in the high-impedance state (essentially equal to the feedback-divider resistance) and reduces quiescent current to under 2 µA. If the shutdown feature is not used, $\overline{EN}$ should be tied to ground. Response to an enable transition is quick; regulated output voltage is reestablished in typically 120 µs.

minimum load requirements

The TPS71xx family is stable even at zero load; no minimum load is required for operation.

SENSE-pin connection

The SENSE pin of fixed-output devices must be connected to the regulator output for proper functioning of the regulator. Normally, this connection should be as short as possible; however, the connection can be made near a critical circuit (remote sense) to improve performance at that point. Internally, SENSE connects to a high-impedance wide-bandwidth amplifier through a resistor-divider network and noise pickup feeds through to the regulator output. Routing the SENSE connection to minimize/avoid noise pickup is essential. Adding an RC network between SENSE and OUT to filter noise is not recommended because it can cause the regulator to oscillate.

external capacitor requirements

An input capacitor is not required; however, a ceramic bypass capacitor (0.047 pF to 0.1 µF) improves load transient response and noise rejection if the TPS71xx is located more than a few inches from the power supply. A higher-capacitance electrolytic capacitor may be necessary if large (hundreds of milliamps) load transients with fast rise times are anticipated.

APPLICATION INFORMATION

external capacitor requirements (continued)

As with most LDO regulators, the TPS71xx family requires an output capacitor for stability. A low-ESR 10-µF solid-tantalum capacitor connected from the regulator output to ground is sufficient to ensure stability over the full load range (see Figure 43). Adding high-frequency ceramic or film capacitors (such as power-supply bypass capacitors for digital or analog ICs) can cause the regulator to become unstable unless the ESR of the tantalum capacitor is less than 1.2 Ω over temperature. Capacitors with published ESR specifications such as the AVX TPSD106K035R0300 and the Sprague 593D106X0035D2W work well because the maximum ESR at 25°C is 300 mΩ (typically, the ESR in solid-tantalum capacitors increases by a factor of 2 or less when the temperature drops from 25°C to –40°C). Where component height and/or mounting area is a problem, physically smaller, 10-µF devices can be screened for ESR. Figures 34 through 41 show the stable regions of operation using different values of output capacitance with various values of ceramic load capacitance.

In applications with little or no high-frequency bypass capacitance (< 0.2 µF), the output capacitance can be reduced to 4.7 µF, provided ESR is maintained between 0.7 and 2.5 Ω. Because minimum capacitor ESR is seldom if ever specified, it may be necessary to add a 0.5-Ω to 1-Ω resistor in series with the capacitor and limit ESR to 1.5 Ω maximum. As show in the ESR graphs (Figures 34 through 41), minimum ESR is not a problem when using 10-µF or larger output capacitors.

Below is a partial listing of surface-mount capacitors usable with the TPS71xx family. This information (along with the ESR graphs, Figures 34 through 41) is included to assist in selection of suitable capacitance for the user's application. When necessary to achieve low height requirements along with high output current and/or high ceramic load capacitance, several higher ESR capacitors can be used in parallel to meet the guidelines above.

All load and temperature conditions with up to 1 µF of added ceramic load capacitance:

PART NO.	MFR.	VALUE	MAX ESR†	SIZE (H × L × W)†
T421C226M010AS	Kemet	22 µF, 10 V	0.5	2.8 × 6 × 3.2
593D156X0025D2W	Sprague	15 µF, 25 V	0.3	2.8 × 7.3 × 4.3
593D106X0035D2W	Sprague	10 µF, 35 V	0.3	2.8 × 7.3 × 4.3
TPSD106M035R0300	AVX	10 µF, 35 V	0.3	2.8 × 7.3 × 4.3

Load < 200 mA, ceramic load capacitance < 0.2 µF, full temperature range:

PART NO.	MFR.	VALUE	MAX ESR†	SIZE (H × L × W)†
592D156X0020R2T	Sprague	15 µF, 20 V	1.1	1.2 × 7.2 × 6
595D156X0025C2T	Sprague	15 µF, 25 V	1	2.5 × 7.1 × 3.2
595D106X0025C2T	Sprague	10 µF, 25 V	1.2	2.5 × 7.1 × 3.2
293D226X0016D2W	Sprague	22 µF, 16 V	1.1	2.8 × 7.3 × 4.3

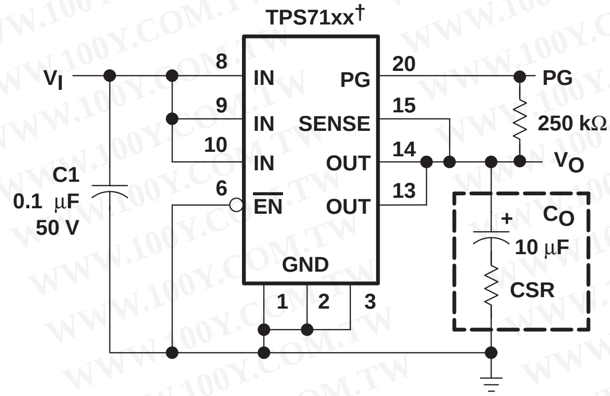
Load < 100 mA, ceramic load capacitance < 0.2 µF, full temperature range:

PART NO.	MFR.	VALUE	MAX ESR†	SIZE (H × L × W)†
195D106X06R3V2T	Sprague	10 µF, 6.3 V	1.5	1.3 × 3.5 × 2.7
195D106X0016X2T	Sprague	10 µF, 16 V	1.5	1.3 × 7 × 2.7
595D156X0016B2T	Sprague	15 µF, 16 V	1.8	1.6 × 3.8 × 2.6
695D226X0015F2T	Sprague	22 µF, 15 V	1.4	1.8 × 6.5 × 3.4
695D156X0020F2T	Sprague	15 µF, 20 V	1.5	1.8 × 6.5 × 3.4
695D106X0035G2T	Sprague	10 µF, 35 V	1.3	2.5 × 7.6 × 2.5

† Size is in mm. ESR is maximum resistance at 100 kHz and T_A = 25°C. Listings are sorted by height.

APPLICATION INFORMATION

external capacitor requirements (continued)



† TPS7133, TPS7148, TPS7150 (fixed-voltage options)

Figure 43. Typical Application Circuit

programming the TPS7101 adjustable LDO regulator

Programming the adjustable regulators is accomplished using an external resistor divider as shown in Figure 44. The equation governing the output voltage is:

$$V_O = V_{ref} \cdot \left(1 + \frac{R1}{R2}\right)$$

where

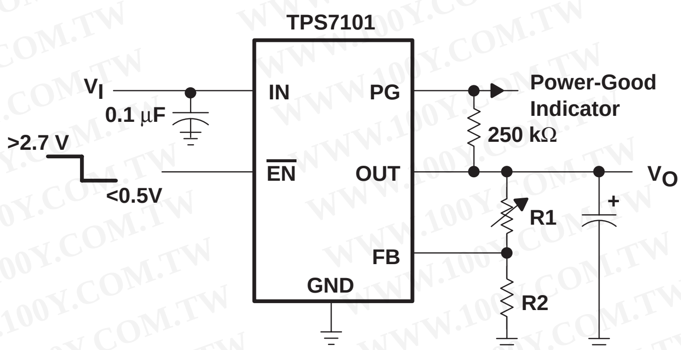
V_{ref} = reference voltage, 1.178 V typ

APPLICATION INFORMATION

programming the TPS7101 adjustable LDO regulator (continued)

Resistors R1 and R2 should be chosen for approximately 7-μA divider current. A recommended value for R2 is 169 kΩ with R1 adjusted for the desired output voltage. Smaller resistors can be used, but offer no inherent advantage and consume more power. Larger values of R1 and R2 should be avoided as leakage currents at FB will introduce an error. Solving equation 1 for R1 yields a more useful equation for choosing the appropriate resistance:

$$R1 = \left(\frac{V_O}{V_{ref}} - 1 \right) \cdot R2$$



OUTPUT VOLTAGE PROGRAMMING GUIDE

OUTPUT VOLTAGE	R1	R2	UNIT
2.5 V	191	169	kΩ
3.3 V	309	169	kΩ
3.6 V	348	169	kΩ
4 V	402	169	kΩ
5 V	549	169	kΩ
6.4 V	750	169	kΩ

Figure 44. TPS7101 Adjustable LDO Regulator Programming

power-good indicator

The TPS71xx features a power-good (PG) output that can be used to monitor the status of the regulator. The internal comparator monitors the output voltage: when the output drops to between 92% and 98% of its nominal regulated value, the PG output transistor turns on, taking the signal low. The open-drain output requires a pullup resistor. If not used, it can be left floating. PG can be used to drive power-on reset circuitry or as a low-battery indicator. PG does not assert itself when the regulated output voltage falls outside the specified 2% tolerance, but instead reports an output voltage low, relative to its nominal regulated value.

regulator protection

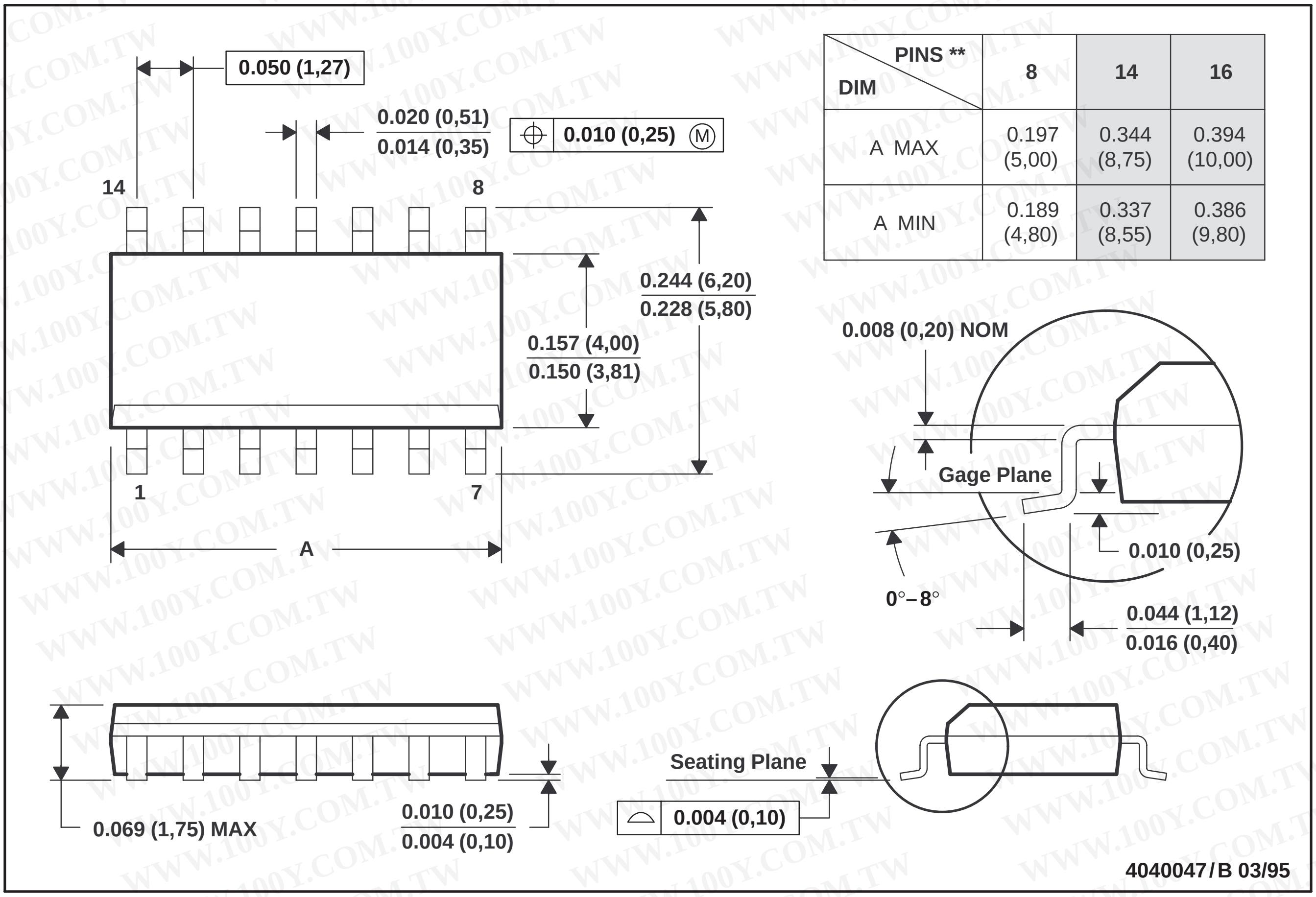
The TPS71xx PMOS-pass transistor has a built-in back diode that safely conducts reverse currents when the input voltage drops below the output voltage (e.g., during power down). Current is conducted from the output to the input and is not internally limited. When extended reverse voltage is anticipated, external limiting may be appropriate.

The TPS71xx also features internal current limiting and thermal protection. During normal operation, the TPS71xx limits output current to approximately 1 A. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds 165°C, thermal-protection circuitry shuts it down. Once the device has cooled, regulator operation resumes.

MECHANICAL DATA

D (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN

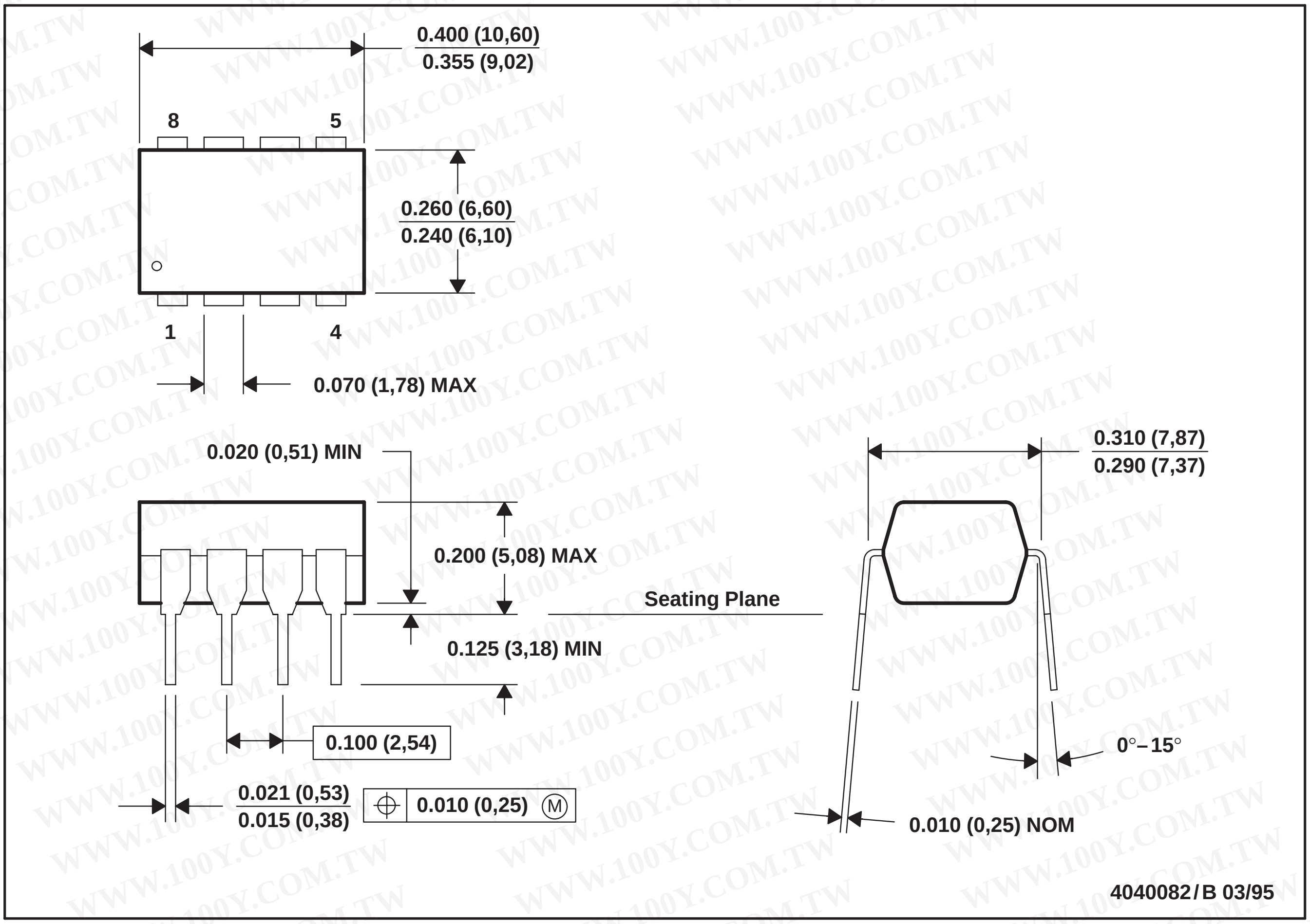


DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

NOTES:
B. All linear dimensions are in inches (millimeters).
C. This drawing is subject to change without notice.
D. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
E. Four center pins are connected to die mount pad.
F. Falls within JEDEC MS-012

MECHANICAL DATA

P (R-PDIP-T8) **PLASTIC DUAL-IN-LINE PACKAGE**

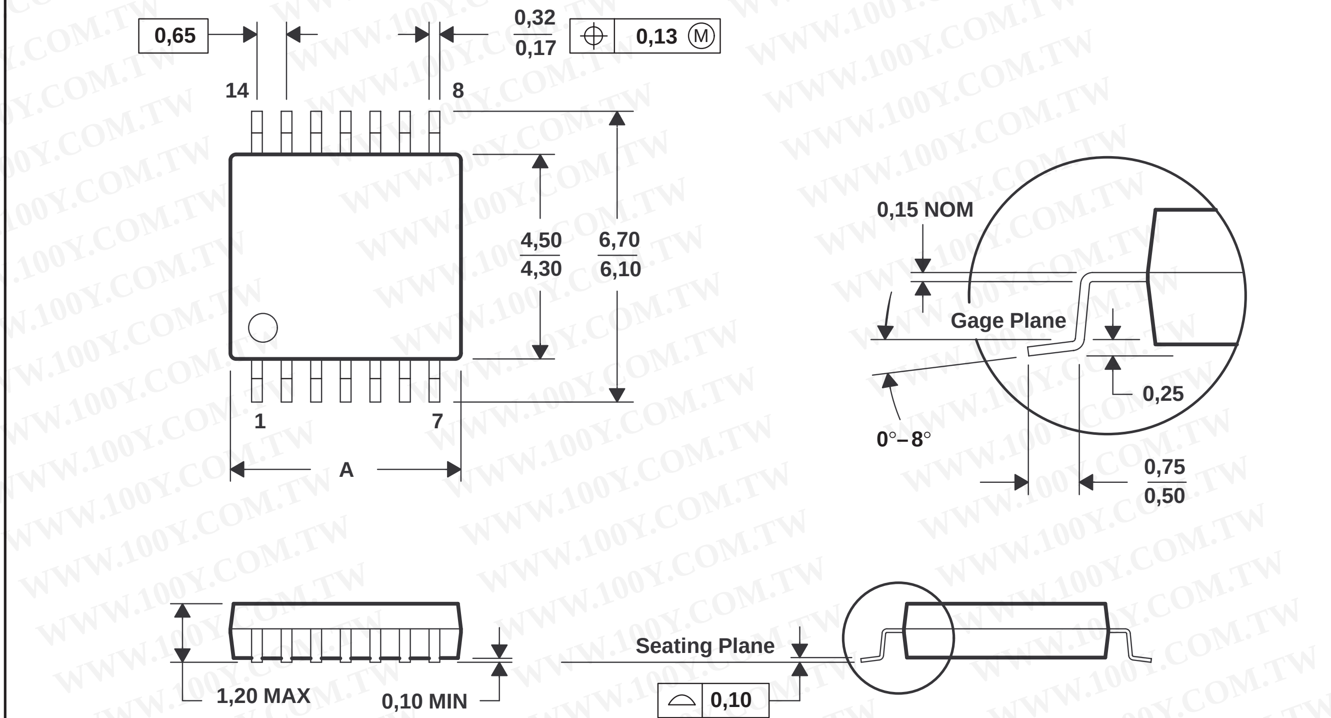


NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001

MECHANICAL DATA

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN



PINS ** / DIM	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064 / D 10/95

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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