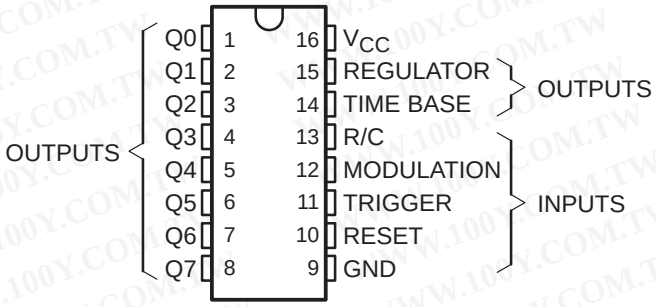
SLFS045 – JUNE 1978 – REVISED MAY 1988

- **Accurate Timing From Microseconds to Days**
- **Programmable Delays From 1 Time Constant to 255 Time Constants**
- **Outputs Compatible With TTL and CMOS**
- **Wide Supply-Voltage Range**
- **External Sync and Modulation Capability**

N PACKAGE
(TOP VIEW)



description

The uA2240C consists of a time-base oscillator, an 8-bit counter, a control flip-flop, and a voltage regulator. The frequency of the time-base oscillator is set by the time constant of an external resistor and capacitor at R/C and can be synchronized or modulated by signals applied to the modulation input. The output of the time-base section is applied directly to the input of the counter section and also appears at (TIME BASE). TIME BASE may be used to monitor the frequency of the oscillator, to provide an output pulse to other circuitry, or (with the time-base section disabled) to drive the counter input from an external source. The counter input is activated on a negative-going transition. The reset input stops the time-base oscillator and sets each binary output, Q0–Q7, and the time-base output to a TTL high level. After resetting, the trigger input starts the oscillator and all Q outputs go low. Once triggered, the uA2240C will ignore any signals at the trigger input until it is reset.

The uA2240C timer/counter may be operated in the free-running mode or with output-signal feedback to the reset input for automatic reset. Two or more binary outputs may be connected together to generate complex pulse patterns, or each output may be used separately to provide eight output frequencies. Using two circuits in cascade can provide precise time delays of up to three years.

The uA2240C is characterized for operation from 0°C to 70°C.

AVAILABLE OPTIONS

SYMBOLIZATION		OPERATING TEMPERATURE RANGE	V_T max AT 25°C
DEVICE	PACKAGE SUFFIX		
uA2240C	N	0°C to 70°C	2 V

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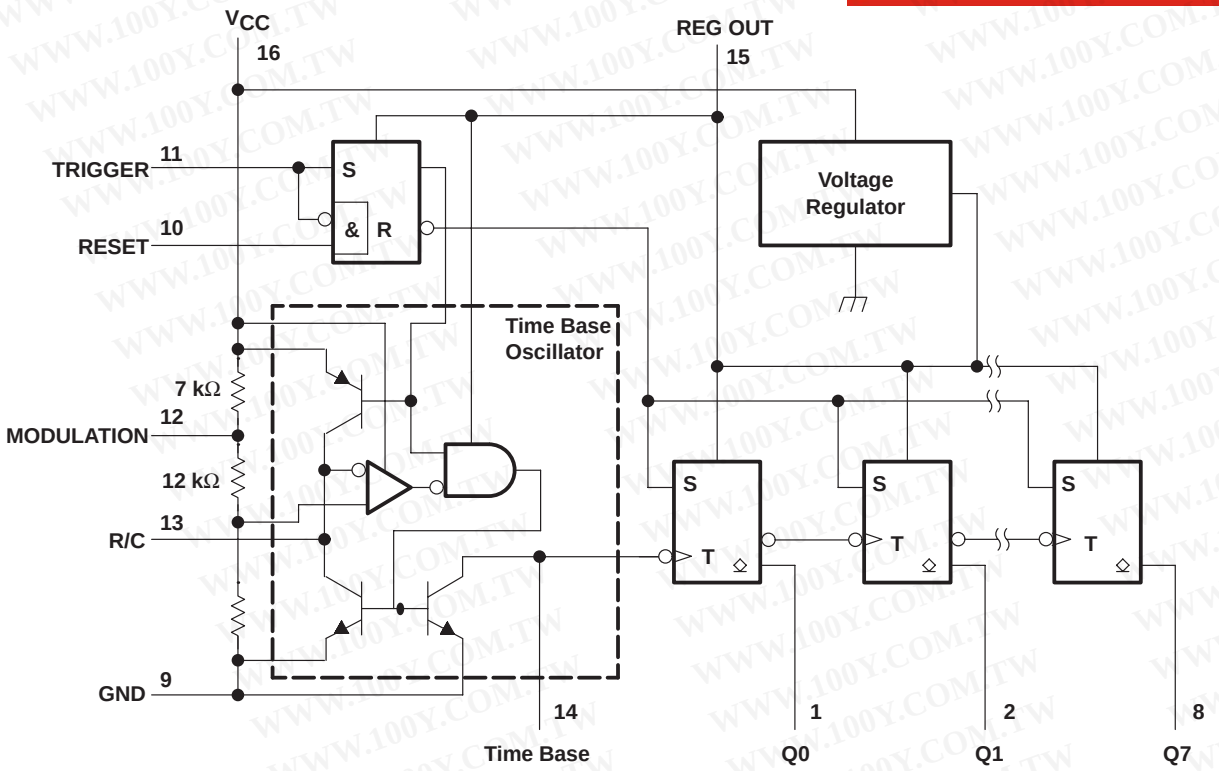
functional block diagram



◇ = open-collector outputs

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 18 V
Output voltage: Q0–Q7 . . . . . 18 V
Output current: Q0–Q7 . . . . . 10 mA
Regulator output current . . . . . –5 mA
Continuous total dissipation at (or below) 25°C free-air temperature . . . . . 650 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTE 1: Voltage values are with respect to the network ground terminal.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC} (see Note 2)	4		14	V
Timing resistor	0.001		10	MΩ
Timing capacitor	0.01		1000	µF
Counter input frequency (Pin 14)		1.5		MHz
Pull-up resistor, time-based output		20		kΩ
Trigger and reset input pulse voltage	2	3		V
Trigger and reset input pulse duration	2			µs
External clock input pulse voltage	3			V
External clock input pulse duration	1			µs

NOTE 2: For operation with $V_{CC} \leq 4.5$ V, short regulator output to V_{CC}.

electrical characteristics at 25°C free-air temperature

PARAMETER	TEST CIRCUIT	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Regulator output voltage	1	V_{CC} = 5 V, TRIGGER and RESET open or grounded	3.9	4.4		V
	2	V_{CC} = 15 V, TRIGGER and RESET open or grounded	5.8	6.3	6.8	
Modulation input open circuit voltage	1	V_{CC} = 5 V, TRIGGER and RESET open or grounded	2.8	3.5	4.2	V
		V_{CC} = 15 V, TRIGGER and RESET open or grounded		10.5		
Trigger threshold voltage	1	V_{CC} = 5 V, RESET at 0 V		1.4	2	V
High-level trigger current	1	V_{CC} = 5 V, TRIGGER at 2 V, RESET at 0 V		10		µA
Reset threshold voltage	1	V_{CC} = 5 V, TRIGGER at 0 V		1.4	2	V
High-level reset current	1	V_{CC} = 5 V, TRIGGER at 0 V		10		µA
Counter input (time base) threshold voltage	2	V_{CC} = 5 V, TRIGGER and RESET open or grounded	1	1.4		V
Low-level output current, Q0–Q7	2	V_{CC} = 5 V, V_{OL} < 0.4 V, TRIGGER at 2 V, RESET at 0 V,	2	4		mA
High-level output current, Q0–Q7	2	V_{OH} = 15 V, RESET at 2 V, TRIGGER at 0 V		0.01	15	µA
Supply current	1	V_{CC} = 5 V, TRIGGER at 0 V, RESET at 5 V		4	7	mA
	1	V_{CC} = 15 V, TRIGGER at 0 V, RESET at 5 V		13	18	
	3	V+ = 4 V		1.5		

operating characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER	TEST CIRCUIT	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
Initial error of time base‡	1	V_{CC} = 5 V, TRIGGER at 5 V, RESET at 0 V			±0.5	±5	%
Temperature coefficient of time-base period	1	T_A = 0°C to 70°C	V_{CC} = 5 V		–200		ppm/°C
			V_{CC} = 15 V		–80		
Supply voltage sensitivity of time-base period	1	V_{CC} ≥ 8 V			–0.08	–0.3	%/V
Time-base output frequency	1	V_{CC} = 5 V, R = MIN, C = MIN			130		kHz
Propagation delay time		See Note 3	From TRIGGER input		1		µs
			From RESET input		0.8		
Output rise time	2	R_L = 3 kΩ, C_L = 10 pF	Q0–Q7		180		ns
Output fall time					180		

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ This is the time-base period error due only to the uA2240C and expressed as a percentage of nominal (1.00 RC).
NOTE 3: Propagation delay time is measured from the 50% point on the leading edge of an input pulse to the 50% point on the leading edge of the resulting change of state at Q0.

PARAMETER MEASUREMENT INFORMATION

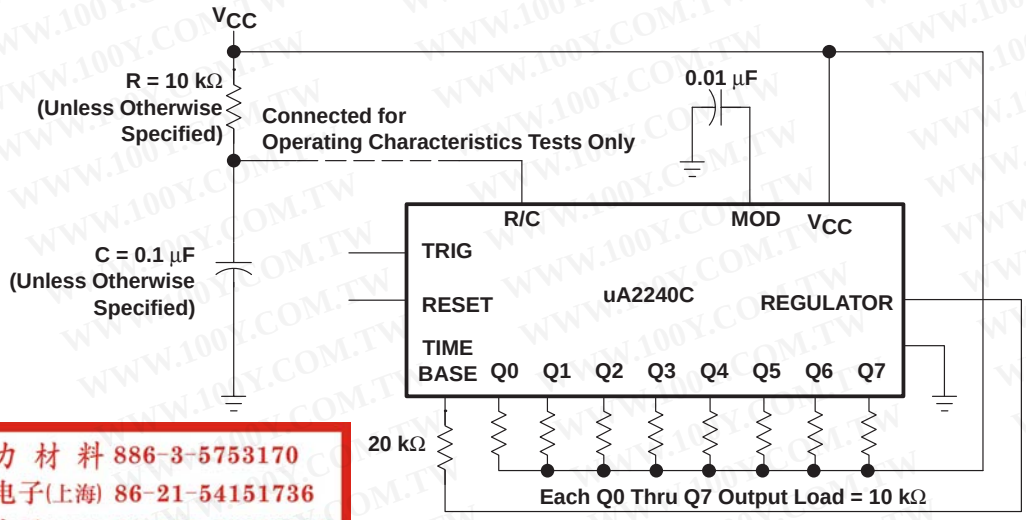


Figure 1. General Test Circuit

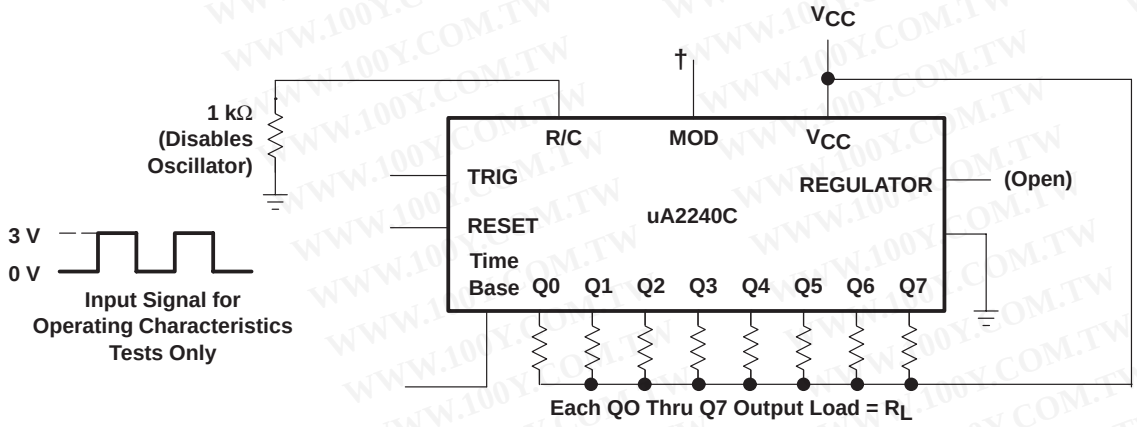
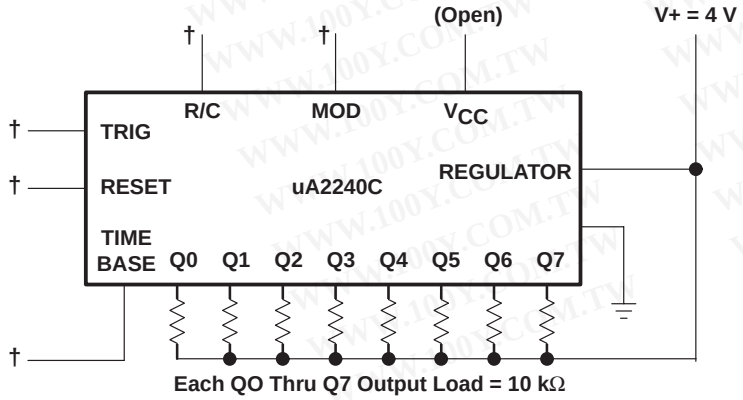


Figure 2. Counter Test Circuit



† These connections may be open or ungrounded for this test.

Figure 3. Reduced-Power Test Circuit (Time Base Disabled)

TYPICAL CHARACTERISTICS

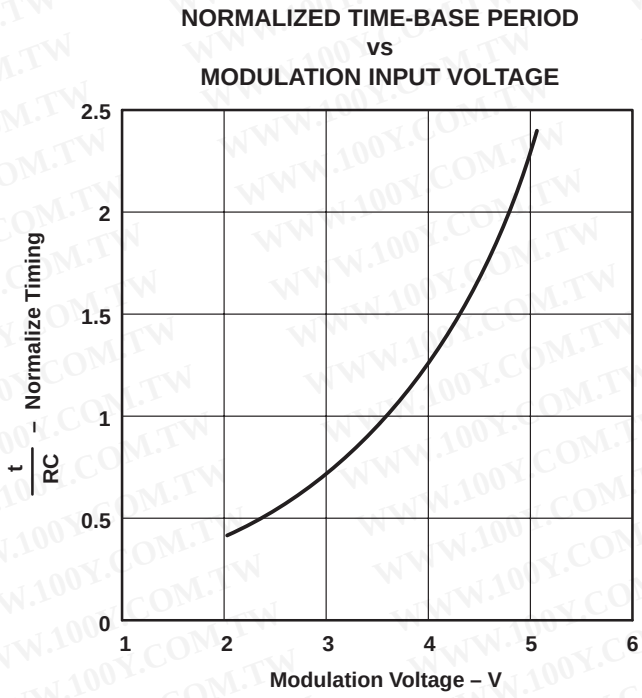


Figure 4

APPLICATION INFORMATION

Figure 5 shows voltage waveforms for typical operation of the uA2240C. If both RESET and TRIGGER are low during power up, the timer/counter will be in a reset state with all binary (Q) outputs high and the oscillator stopped. In this state, a high level on the trigger input starts the time-base oscillator. The initial negative-going pulse from the oscillator sets the Q outputs to low logic levels at the beginning of the first time-base period. The uA2240C will ignore any further signals at the TRIGGER until after a reset signal is applied to RESET. With TRIGGER low, a high level at the reset input will set Q outputs high and stop the time-base oscillator. If the reset signal occurs while TRIGGER is high, the reset is ignored. If RESET remains high when TRIGGER goes low, the uA2240C will reset.

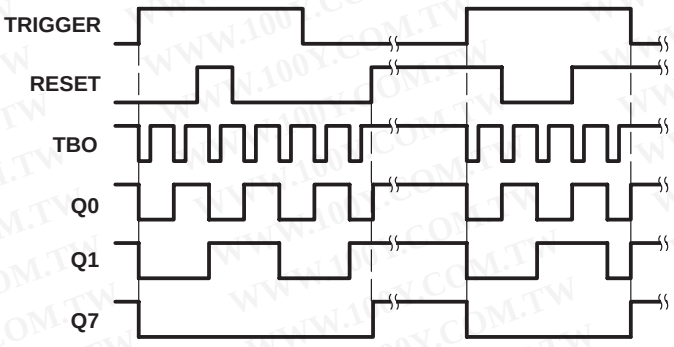


Figure 5. Timing Diagram of Output Waveform

APPLICATION INFORMATION

In monostable applications of the uA2240C, one or more of the binary outputs will be connected to RESET as shown in Figure 6. The binary outputs are open-collector stages that can be connected together to a common pullup resistor to provide a wired-OR function. The combined output will be low as long as any one of the outputs is low. This type of arrangement can be used for time delays that are integer multiples of the time-base period. For example, if Q5 ($2^5 = 32$) only is connected to the reset input, every trigger pulse will generate a 32-period active-low output. Similarly, if Q0, Q4, and Q5 are connected to RESET, each trigger pulse creates a 49-period delay.

In astable operation, the uA2240C will free-run from the time it is triggered until it receives an external reset signal.

The period of the time-base oscillator is equal to the RC time constant of an external resistor and capacitor connected as shown in Figure 6 when the modulation input is open (approximately 3.5 V internal, (see Figure 4). Under conditions of high supply voltage ($V_{CC} > 7$ V) and low value of timing capacitor ($C < 0.1\ \mu F$), the pulse duration of the time-base oscillator may be too short to properly trigger the counters. This situation can be corrected by adding a 300-pF capacitor between the time-base output and ground. The time-base output (TBO) is an open-collector output that requires a 20-kΩ pullup resistor in V_{REG} for proper operation. The time-base pin may also be used as an input to the counters for an external timebase or as an active-low inhibit to interrupt counting without resetting.

The modulation input varies the ratio of the time-base period to the RC time constant as a function of the DC bias voltage (see Figure 4). It can also be used to synchronize the timer/counter to an external clock or sync signal.

The regulator output is used internally to drive the binary counters and the control logic. This terminal can be used to supply voltage to additional uA2240C devices to minimize power dissipation when several timer circuits are cascaded. For circuit operation with an external clock, the regulator output can be used as the V_{CC} input terminal to power down the internal time base and reduce power dissipation. When supply voltages less than 4.5 V are used with the internal time base, V_{REG} should be shorted to V_{CC}.

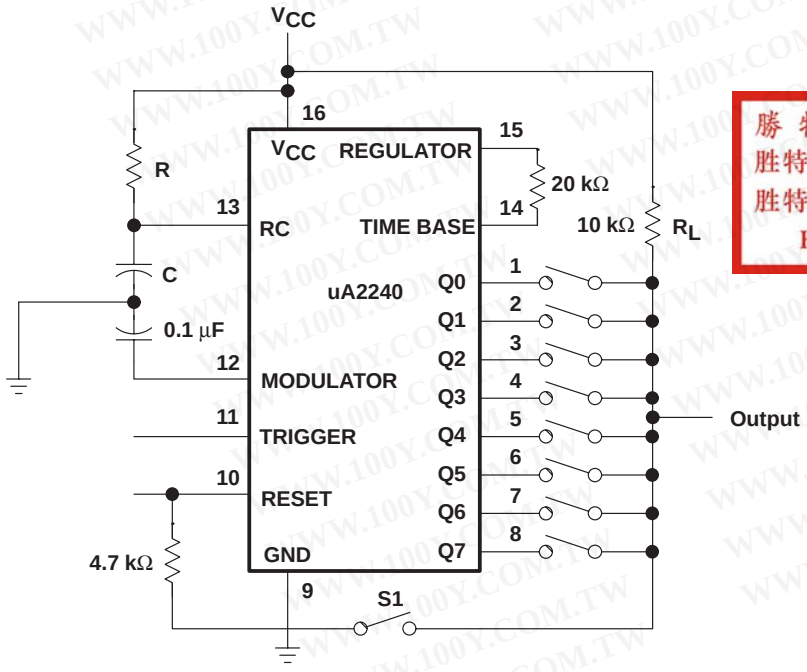


Figure 6. Basic Connections for Timing Applications

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
UA2240CN	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.