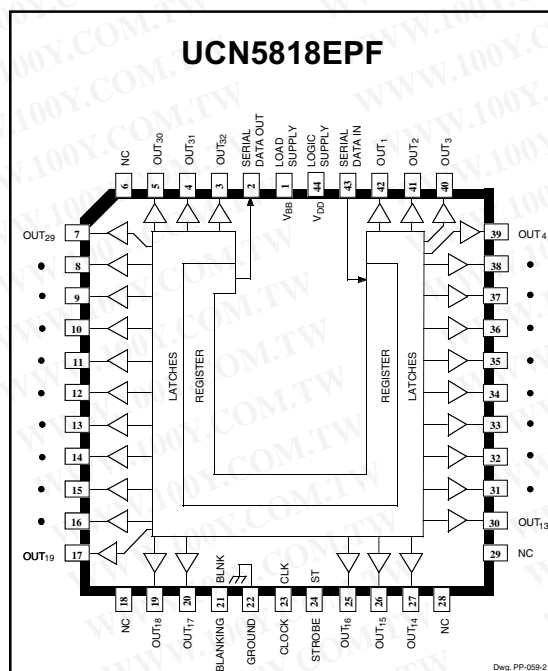


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# 5818-F

## BiMOS II 32-BIT SERIAL-INPUT, LATCHED SOURCE DRIVERS WITH ACTIVE-DMOS PULL-DOWNS



### ABSOLUTE MAXIMUM RATINGS at $T_A = 25^\circ\text{C}$

|   |                            |
|---|----------------------------|
| Logic Supply Voltage, $V_{DD}$ .....                  | 15 V                       |
| Driver Supply Voltage, $V_{BB}$ .....                 | 60 V                       |
| Continuous Output Current,<br>$I_{OUT}$ .....         | -40 mA to +15 mA           |
| Input Voltage Range,<br>$V_{IN}$ .....                | -0.3 V to $V_{DD} + 0.3$ V |
| Package Power Dissipation, $P_D$<br>(UCN5818AF) ..... | 3.5 W*                     |
| (UCN5818EPF) .....                                    | 2.7 W†                     |
| Operating Temperature Range,<br>$T_A$ .....           | -20°C to +85°C             |
| Storage Temperature Range,<br>$T_S$ .....             | -55°C to +150°C            |

\* Derate at rate of 28 mW/°C above  $T_A = +25^\circ\text{C}$   
 † Derate at rate of 22 mW/°C above  $T_A = +25^\circ\text{C}$

Caution: CMOS devices have input static protection but are susceptible to damage when exposed to extremely high static electrical charges.

Designed primarily for use with vacuum-fluorescent displays, the UCN5818AF and UCN5818EPF smart power BiMOS II drivers combine CMOS shift registers, data latches, and control circuitry, with bipolar high-speed sourcing outputs and DMOS active pull-down circuitry. The high-speed shift register and data latches allow direct interfacing with microprocessor LSI-based systems. A CMOS serial data output enables cascade connections in applications requiring additional drive lines. Both devices feature 60 V and -40 mA output ratings, allowing them to be used in many other peripheral power driver applications.

These smart power drivers have been designed with BiMOS II logic for improved data entry rates. With a 5 V supply, it will operate to at least 3.3 MHz. At 12 V, higher speeds are possible. Use of these devices with TTL may require the use of appropriate pull-up resistors to ensure an input logic high. All devices can be operated over the ambient temperature range of -20°C to +85°C. The UCN5818AF is supplied in a 40-pin plastic dual in-line package with 0.600" (15.24 mm) row spacing. A copper lead frame, reduced supply current requirement, and low output saturation voltage permits operation with minimum junction temperature rise. The 'A' package allows all 32 outputs to be operated at -25 mA continuously over the operating temperature range.

For high-density packaging applications, the UCN5818EPF is furnished in a 44-lead plastic chip carrier (quad pack) for surface mounting on solder lands with 0.050" (1.27 mm) centers. The PLCC allows -25 mA continuous operation of all outputs simultaneously at ambient temperatures to 60°C. Similar devices are available as the UCN5810AF/LWF (10 bits), UCN5811A (12 bits), and UCN5812AF/EPF (20 bits).

### FEATURES

- 60 V Source Outputs
- High-Speed Source Drivers
- To 3.3 MHz Data Input Rate
- Low-Output Saturation Voltages
- Active DMOS Pull-Downs
- Low-Power CMOS Logic and Latches
- Reduced Supply Current Requirements
- Improved Replacements for SN75518N/FN

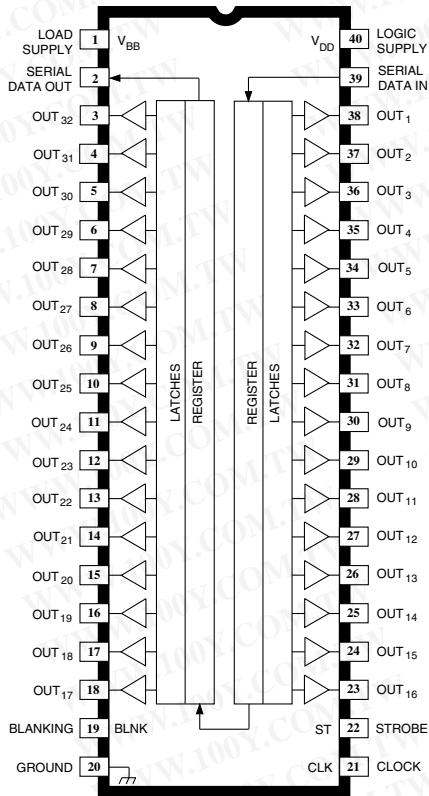
Always order by complete part number, e.g., **UCN5818EPF**.

# 5818-F

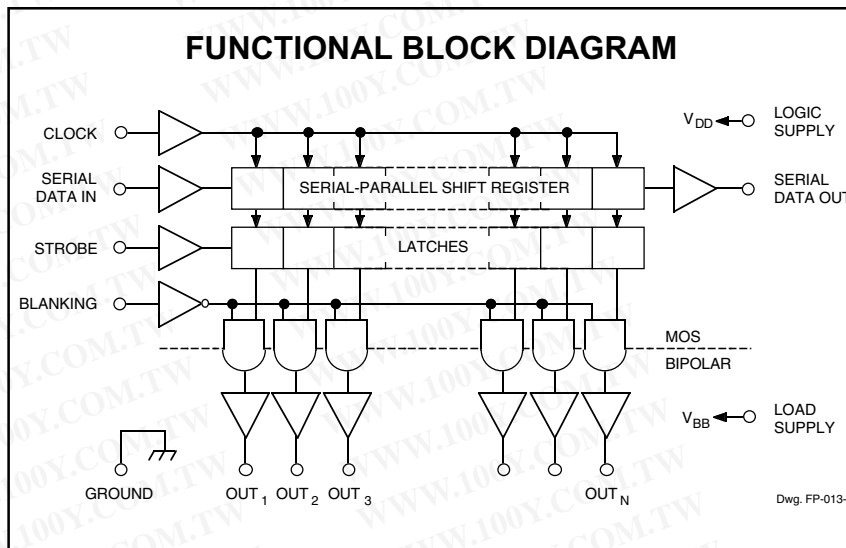
## 32-BIT SERIAL-INPUT, LATCHED SOURCE DRIVERS WITH ACTIVE-DMOS PULL-DOWNS

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**UCN5818AF**

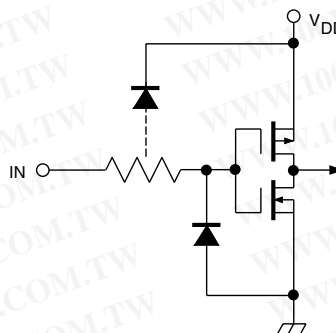


Dwg. PP-029-4



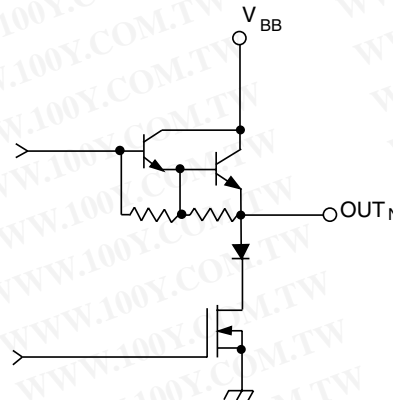
Dwg. FP-013-1

### TYPICAL INPUT CIRCUIT

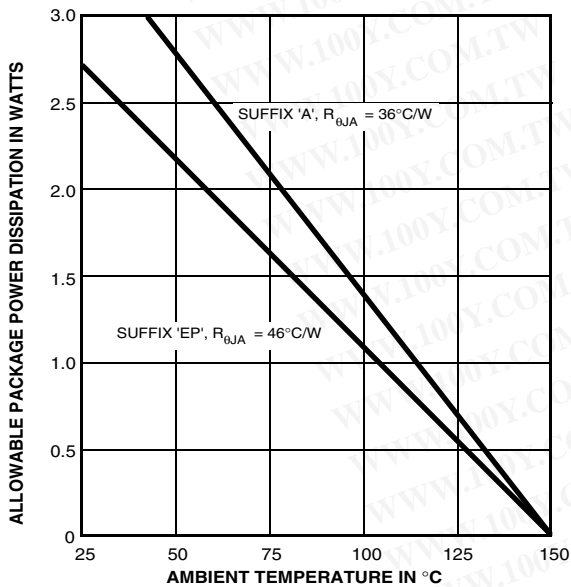


Dwg. EP-010-5

### TYPICAL OUTPUT DRIVER



Dwg. No. A-14,219



Dwg. GP-025A

Dwg. GP-025A



# 5818-F

## 32-BIT SERIAL-INPUT, LATCHED SOURCE DRIVERS WITH ACTIVE-DMOS PULL-DOWNS

**ELECTRICAL CHARACTERISTICS at  $T_A = +25^\circ\text{C}$ ,  $V_{BB} = 60\text{ V}$  unless otherwise noted.**

| Characteristic             | Symbol       | Test Conditions                                    | Limits @ $V_{DD} = 5\text{ V}$ |       |      | Limits @ $V_{DD} = 12\text{ V}$ |      |      | Units         |
|----------------------------|--------------|--|--------------------------------|-------|------|---------------------------------|------|------|---------------|
|                            |              |  | Min.                           | Typ.  | Max. | Min.                            | Typ. | Max. |               |
| Output Leakage Current     | $I_{CEX}$    | $V_{OUT} = 0\text{ V}$ , $T_A = +70^\circ\text{C}$ | —                              | -5.0  | -15  | —                               | -5.0 | -15  | $\mu\text{A}$ |
| Output Voltage             | $V_{OUT(1)}$ | $I_{OUT} = -25\text{ mA}$                          | 58                             | 58.5  | —    | 58                              | 58.5 | —    | V             |
|                            | $V_{OUT(0)}$ | $I_{OUT} = 1\text{ mA}$                            | —                              | 2.0   | 3.0  | —                               | —    | —    | V             |
|                            |              | $I_{OUT} = 2\text{ mA}$                            | —                              | —     | —    | —                               | 2.0  | 3.5  | V             |
| Output Pull-Down Current   | $I_{OUT(0)}$ | $V_{OUT} = 5\text{ V to }V_{BB}$                   | 2.0                            | 3.5   | —    | —                               | —    | —    | mA            |
|                            |              | $V_{OUT} = 20\text{ V to }V_{BB}$                  | —                              | —     | —    | 8.0                             | 13   | —    | mA            |
| Input Voltage              | $V_{IN(1)}$  |  | 3.5                            | —     | 5.3  | 10.5                            | —    | 12.3 | V             |
|                            | $V_{IN(0)}$  |  | -0.3                           | —     | +0.8 | -0.3                            | —    | +0.8 | V             |
| Input Current              | $I_{IN(1)}$  | $V_{IN} = V_{DD}$                                  | —                              | 0.05  | 0.5  | —                               | 0.1  | 1.0  | $\mu\text{A}$ |
|                            | $I_{IN(0)}$  | $V_{IN} = 0.8\text{ V}$                            | —                              | -0.05 | -0.5 | —                               | -0.1 | -1.0 | $\mu\text{A}$ |
| Serial Data Output Voltage | $V_{OUT(1)}$ | $I_{OUT} = -200\ \mu\text{A}$                      | 4.5                            | 4.7   | —    | 11.7                            | 11.8 | —    | V             |
|                            | $V_{OUT(0)}$ | $I_{OUT} = 200\ \mu\text{A}$                       | —                              | 200   | 250  | —                               | 100  | 200  | mV            |
| Maximum Clock Frequency    | $f_{clk}$    |  | 3.3*                           | —     | —    | —                               | —    | —    | MHz           |
| Supply Current             | $I_{DD(1)}$  | All Outputs High                                   | —                              | 100   | 300  | —                               | 200  | 500  | $\mu\text{A}$ |
|                            | $I_{DD(0)}$  | All Outputs Low                                    | —                              | 100   | 300  | —                               | 200  | 500  | $\mu\text{A}$ |
|                            | $I_{BB(1)}$  | Outputs High, No Load                              | —                              | 3.0   | 6.0  | —                               | 3.0  | 6.0  | mA            |
|                            | $I_{BB(0)}$  | Outputs Low  | —                              | 10    | 100  | —                               | 10   | 100  | $\mu\text{A}$ |
| Blanking to Output Delay   | $t_{PHL}$    | $C_L = 30\text{ pF}$ , 50% to 50%                  | —                              | 2000  | —    | —                               | 1000 | —    | ns            |
|                            | $t_{PLH}$    | $C_L = 30\text{ pF}$ , 50% to 50%                  | —                              | 1000  | —    | —                               | 850  | —    | ns            |
| Output Fall Time           | $t_f$        | $C_L = 30\text{ pF}$ , 90% to 10%                  | —                              | 1450  | —    | —                               | 650  | —    | ns            |
| Output Rise Time           | $t_r$        | $C_L = 30\text{ pF}$ , 10% to 90%                  | —                              | 650   | —    | —                               | 700  | —    | ns            |

Negative current is defined as coming out of (sourcing) the specified device terminal.

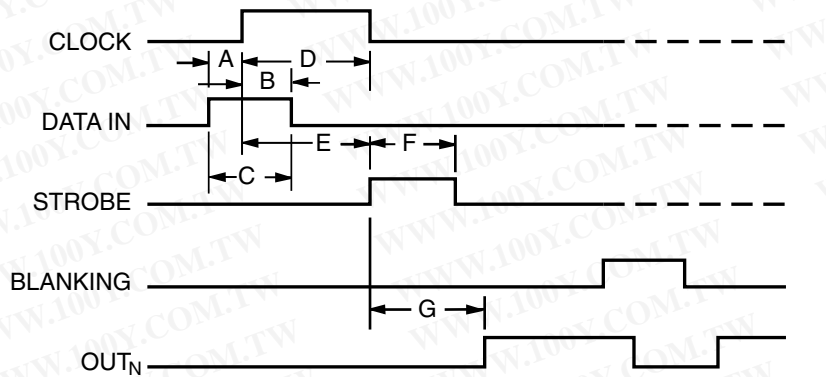
\* Operation at a clock frequency greater than the specified minimum value is possible but not warranted.

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# 5818-F

## 32-BIT SERIAL-INPUT, LATCHED SOURCE DRIVERS WITH ACTIVE-DMOS PULL-DOWNS

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Dwg. No. A-12,649A

### TIMING REQUIREMENTS

( $T_A = +25^\circ\text{C}$ ,  $V_{DD} = 5\text{ V}$ , Logic Levels are  $V_{DD}$  and Ground)

- A. Minimum Data Active Time Before Clock Pulse (Data Set-Up Time) ..... **75 ns**
- B. Minimum Data Active Time After Clock Pulse (Data Hold Time) ..... **75 ns**
- C. Minimum Data Pulse Width ..... **150 ns**
- D. Minimum Clock Pulse Width ..... **150 ns**
- E. Minimum Time Between Clock Activation and Strobe ..... **300 ns**
- F. Minimum Strobe Pulse Width ..... **100 ns**
- G. Typical Time Between Strobe Activation and Output Transistion ..... **500 ns**

Timing is representative of a 3.3 MHz clock. Higher speeds may be attainable with increased supply voltage; operation at high temperatures will reduce the specified maximum clock frequency.

### TRUTH TABLE

| Serial Data Input | Clock Input | Shift Register Contents |                |                |     |                  |                  | Serial Data Output | Strobe Input | Latch Contents |                |                |     |                  |                | Blanking | Output Contents |                |                |     |                  |                |
|-------------------|-------------|-------------------------|----------------|----------------|-----|------------------|------------------|--------------------|--------------|----------------|----------------|----------------|-----|------------------|----------------|----------|-----------------|----------------|----------------|-----|------------------|----------------|
|                   |             | I <sub>1</sub>          | I <sub>2</sub> | I <sub>3</sub> | ... | I <sub>N-1</sub> | I <sub>N</sub>   |                    |              | I <sub>1</sub> | I <sub>2</sub> | I <sub>3</sub> | ... | I <sub>N-1</sub> | I <sub>N</sub> |          | I <sub>1</sub>  | I <sub>2</sub> | I <sub>3</sub> | ... | I <sub>N-1</sub> | I <sub>N</sub> |
| H                 | ┌           | H                       | R <sub>1</sub> | R <sub>2</sub> | ... | R <sub>N-2</sub> | R <sub>N-1</sub> | R <sub>N-1</sub>   |              |                |                |                |     |                  |                |          |                 |                |                |     |                  |                |
| L                 | ┐           | L                       | R <sub>1</sub> | R <sub>2</sub> | ... | R <sub>N-2</sub> | R <sub>N-1</sub> | R <sub>N-1</sub>   |              |                |                |                |     |                  |                |          |                 |                |                |     |                  |                |
| X                 | └           | R <sub>1</sub>          | R <sub>2</sub> | R <sub>3</sub> | ... | R <sub>N-1</sub> | R <sub>N</sub>   | R <sub>N</sub>     |              |                |                |                |     |                  |                |          |                 |                |                |     |                  |                |
|                   |             | X                       | X              | X              | ... | X                | X                | X                  | L            | R <sub>1</sub> | R <sub>2</sub> | R <sub>3</sub> | ... | R <sub>N-1</sub> | R <sub>N</sub> |          |                 |                |                |     |                  |                |
|                   |             | P <sub>1</sub>          | P <sub>2</sub> | P <sub>3</sub> | ... | P <sub>N-1</sub> | P <sub>N</sub>   | P <sub>N</sub>     | H            | P <sub>1</sub> | P <sub>2</sub> | P <sub>3</sub> | ... | P <sub>N-1</sub> | P <sub>N</sub> | L        |                 |                |                |     |                  |                |
|                   |             |                         |                |                |     |                  |                  |                    |              | X              | X              | X              | ... | X                | X              | H        | L               | L              | L              | ... | L                | L              |

L = Low Logic Level H = High Logic Level X = Irrelevant P = Present State R = Previous State

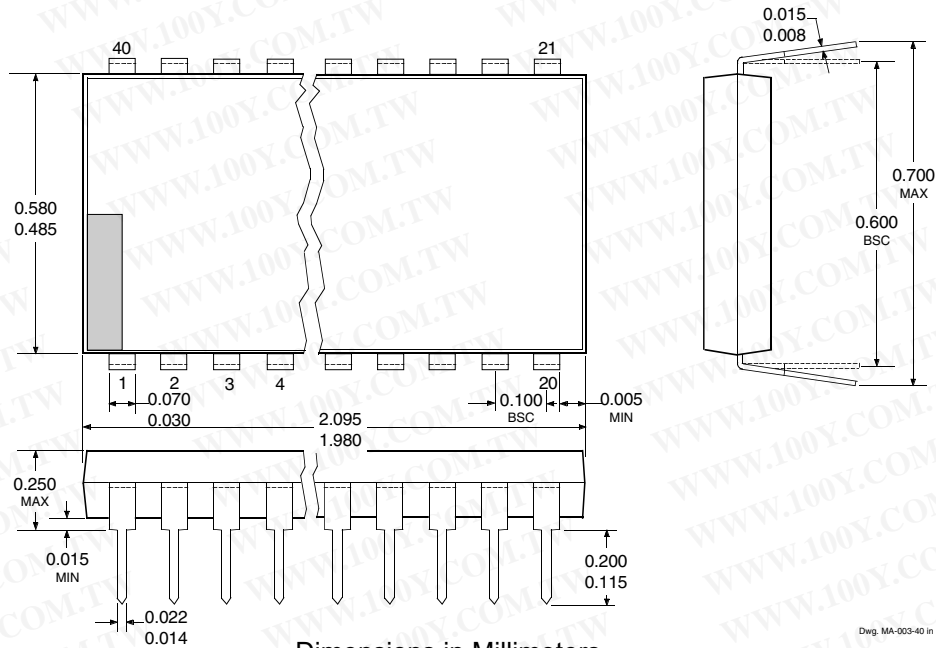


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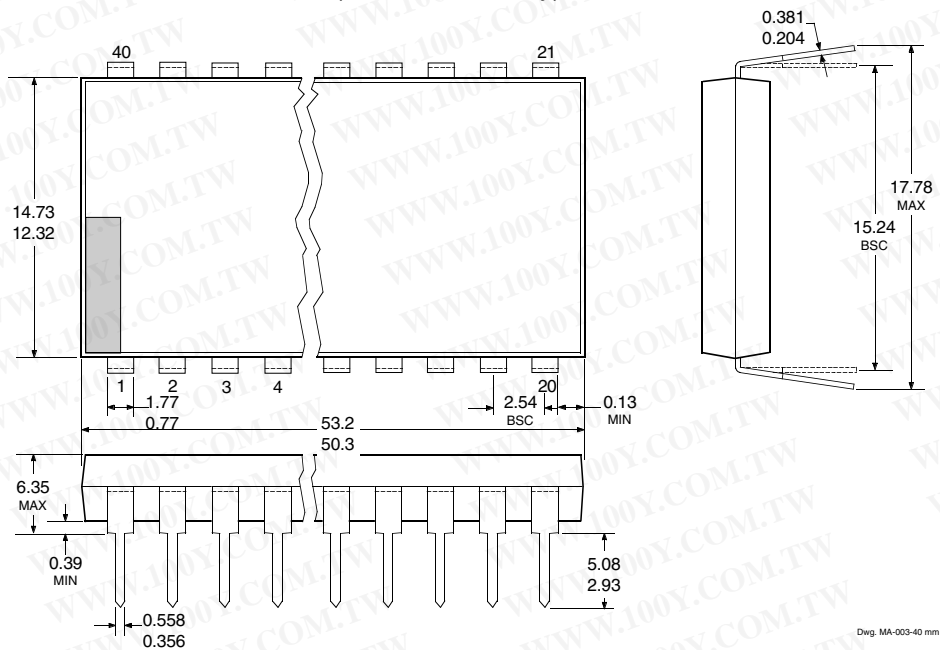
# 5818-F 32-BIT SERIAL-INPUT, LATCHED SOURCE DRIVERS WITH ACTIVE-DMOS PULL-DOWNS

## UCN5818AF

Dimensions in Inches  
(controlling dimensions)



Dimensions in Millimeters  
(for reference only)

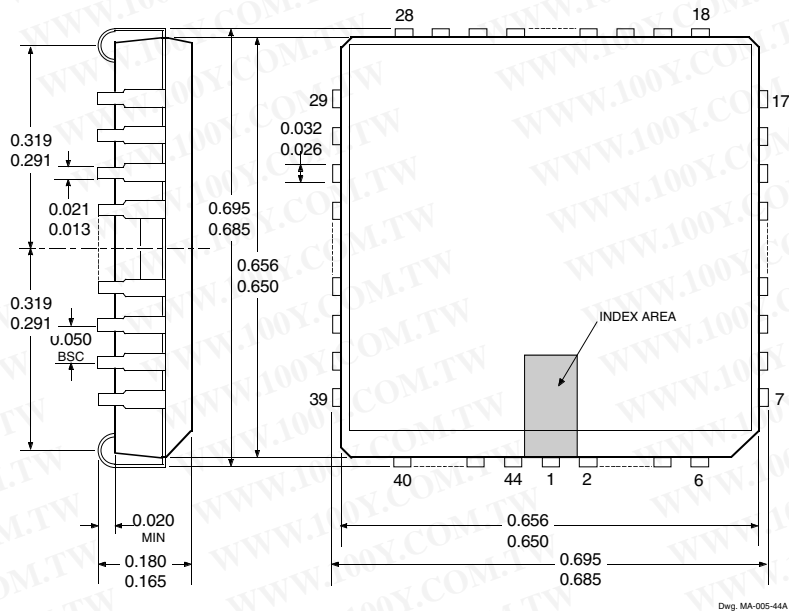


- NOTES: 1. Exact body and lead configuration at vendor's option within limits shown.  
2. Lead spacing tolerance is non-cumulative.  
3. Lead thickness is measured at seating plane or below.  
4. Supplied in standard sticks/tubes of 9 devices.

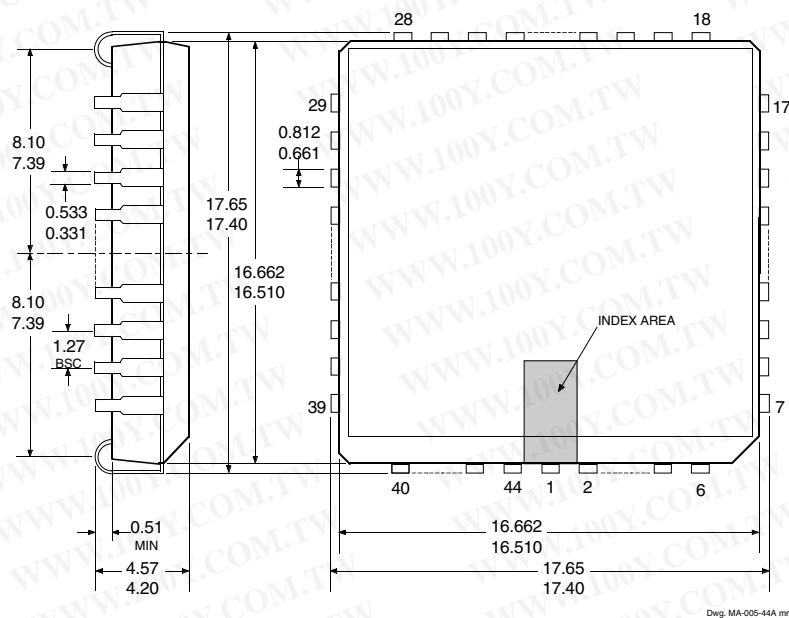
**5818-F**  
**32-BIT SERIAL-INPUT,**  
**LATCHED SOURCE DRIVERS**  
**WITH ACTIVE-DMOS PULL-DOWNS**

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**UCN5818EPF**  
 Dimensions in Inches  
 (controlling dimensions)



Dimensions in Millimeters  
 (for reference only)



- NOTES: 1. Exact body and lead configuration at vendor's option within limits shown.  
 2. Lead spacing tolerance is non-cumulative.  
 3. Supplied in standard sticks/tubes of 27 devices or add "TR" to part number for tape and reel.



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**POWER**  
**INTERFACE DRIVERS**

| Function                                 | Output Ratings* |       | Part Number†       |
|--|-----------------|-------|--------------------|
| <b>SERIAL-INPUT LATCHED DRIVERS</b>      |                 |       |                    |
| 8-Bit (saturated drivers)                | -120 mA         | 50 V‡ | 5895               |
| 8-Bit                                    | 350 mA          | 50 V  | 5821               |
| 8-Bit                                    | 350 mA          | 80 V  | 5822               |
| 8-Bit                                    | 350 mA          | 50 V‡ | 5841               |
| 8-Bit                                    | 350 mA          | 80 V‡ | 5842               |
| 8-Bit (constant-current LED driver)      | 75 mA           | 17 V  | 6275               |
| 8-Bit (DMOS drivers)                     | 250 mA          | 50 V  | 6595               |
| 8-Bit (DMOS drivers)                     | 350 mA          | 50 V‡ | 6A595              |
| 8-Bit (DMOS drivers)                     | 100 mA          | 50 V  | 6B595              |
| 10-Bit (active pull-downs)               | -25 mA          | 60 V  | 5810-F and 6809/10 |
| 12-Bit (active pull-downs)               | -25 mA          | 60 V  | 5811 and 6811      |
| 16-Bit (constant-current LED driver)     | 75 mA           | 17 V  | 6276               |
| 20-Bit (active pull-downs)               | -25 mA          | 60 V  | 5812-F and 6812    |
| 32-Bit (active pull-downs)               | -25 mA          | 60 V  | 5818-F and 6818    |
| 32-Bit                                   | 100 mA          | 30 V  | 5833               |
| 32-Bit (saturated drivers)               | 100 mA          | 40 V  | 5832               |
| <b>PARALLEL-INPUT LATCHED DRIVERS</b>    |                 |       |                    |
| 4-Bit                                    | 350 mA          | 50 V‡ | 5800               |
| 8-Bit                                    | -25 mA          | 60 V  | 5815               |
| 8-Bit                                    | 350 mA          | 50 V‡ | 5801               |
| 8-Bit (DMOS drivers)                     | 100 mA          | 50 V  | 6B273              |
| 8-Bit (DMOS drivers)                     | 250 mA          | 50 V  | 6273               |
| <b>SPECIAL-PURPOSE DEVICES</b>           |                 |       |                    |
| Unipolar Stepper Motor Translator/Driver | 1.25 A          | 50 V‡ | 5804               |
| Addressable 8-Bit Decoder/DMOS Driver    | 250 mA          | 50 V  | 6259               |
| Addressable 8-Bit Decoder/DMOS Driver    | 350 mA          | 50 V‡ | 6A259              |
| Addressable 8-Bit Decoder/DMOS Driver    | 100 mA          | 50 V  | 6B259              |
| Addressable 28-Line Decoder/Driver       | 450 mA          | 30 V  | 6817               |

\* Current is maximum specified test condition, voltage is maximum rating. See specification for sustaining voltage limits. Negative current is defined as coming out of (sourcing) the output.

† Complete part number includes additional characters to indicate operating temperature range and package style.

‡ Internal transient-suppression diodes included for inductive-load protection.

