

MOS FIELD EFFECT TRANSISTOR
 μ PA672T

N-CHANNEL MOS FET ARRAY
 FOR SWITCHING

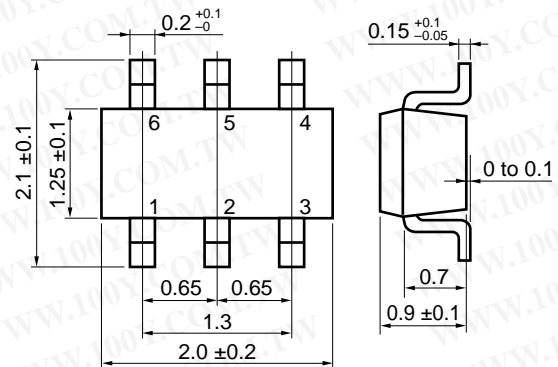
勝特力材料 886-3-5753170
 勝特力电子(上海) 86-21-54151736
 勝特力电子(深圳) 86-755-83298787
[Http://www.100y.com.tw](http://www.100y.com.tw)

The μ PA672T is a super-mini-mold device provided with two MOS FET elements. It achieves high-density mounting and saves mounting costs.

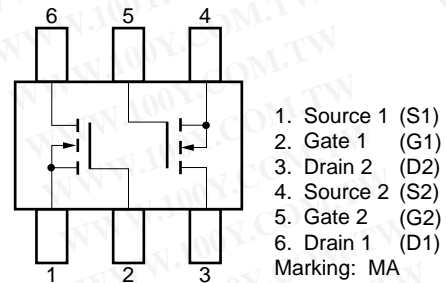
FEATURES

- Two MOS FET circuits in package the same size as SC-70
- Automatic mounting supported

PACKAGE DIMENSIONS (in millimeters)



PIN CONNECTION



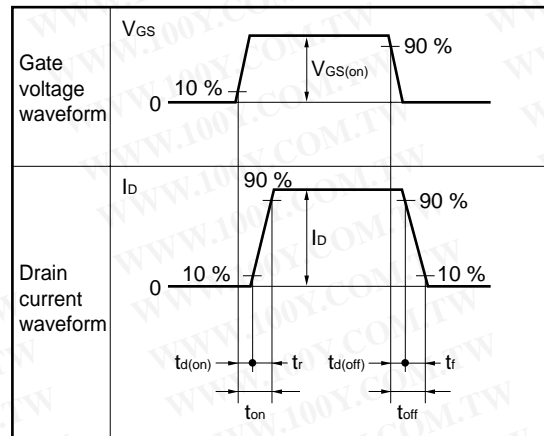
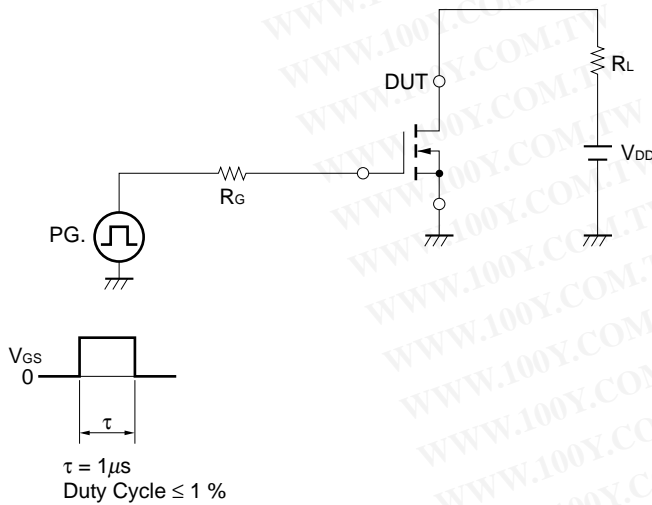
ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C)

PARAMETER	SYMBOL	TEST CONDITIONS	RATINGS	UNIT
Drain to Source Voltage	V _{DSS}		50	V
Gate to Source Voltage	V _{GSS}		±7.0	V
Drain Current (DC)	I _{D(DC)}		100	mA
Drain Current (pulse)	I _{D(pulse)}	PW ≤ 10 ms, Duty Cycle ≤ 50 %	200	mA
Total Power Dissipation	P _T		200 (Total)	mW
Channel Temperature	T _{ch}		150	°C
Storage Temperature	T _{stg}		-55 to +150	°C

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

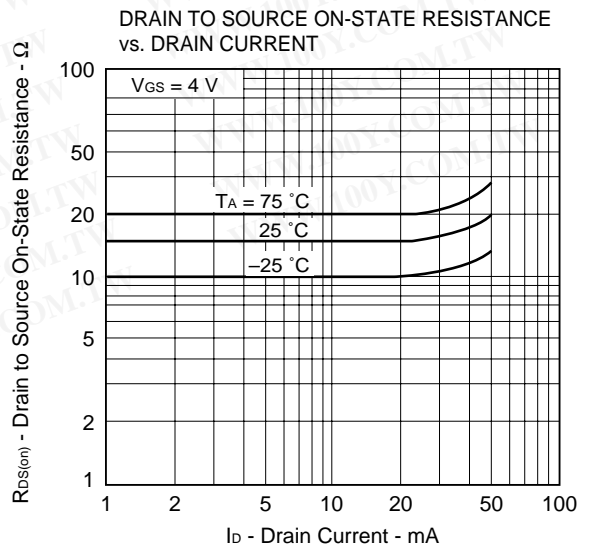
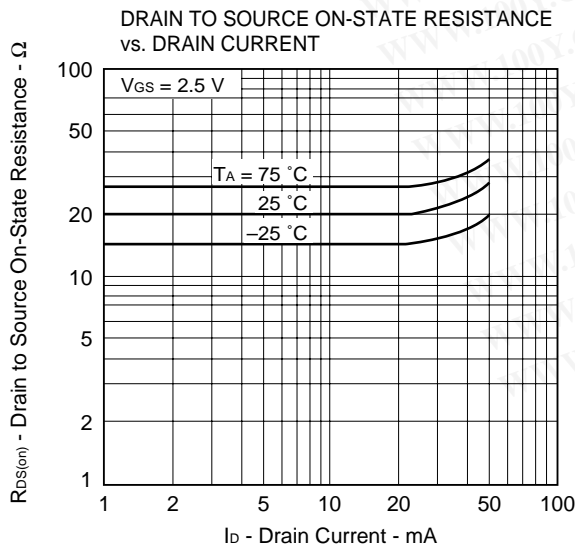
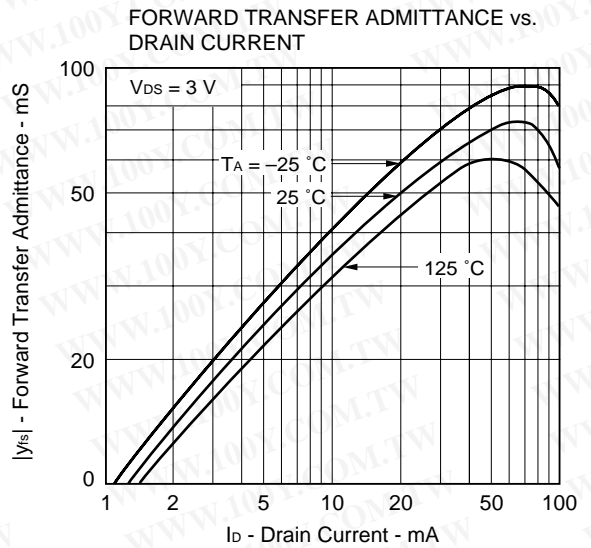
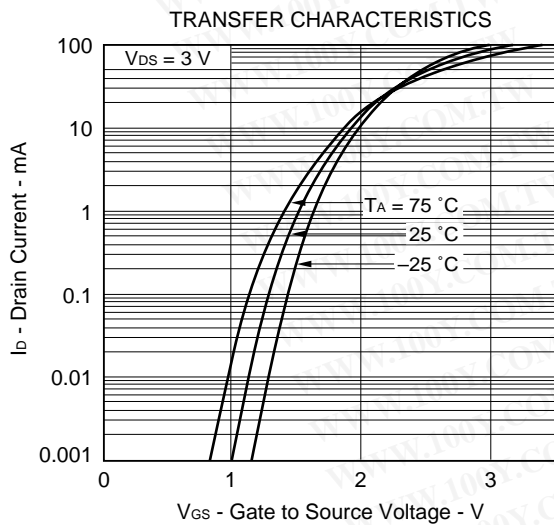
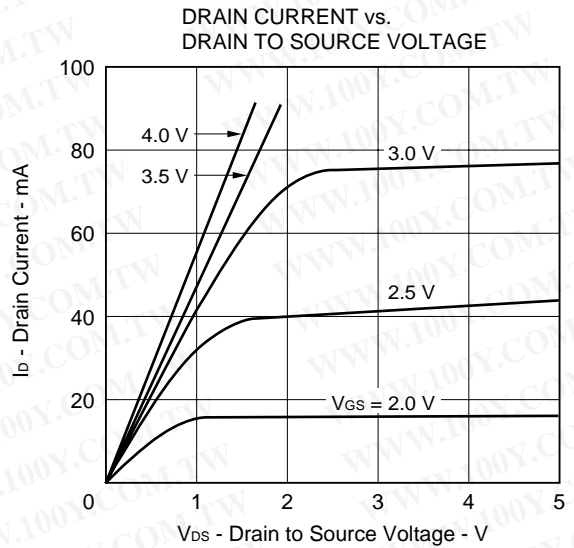
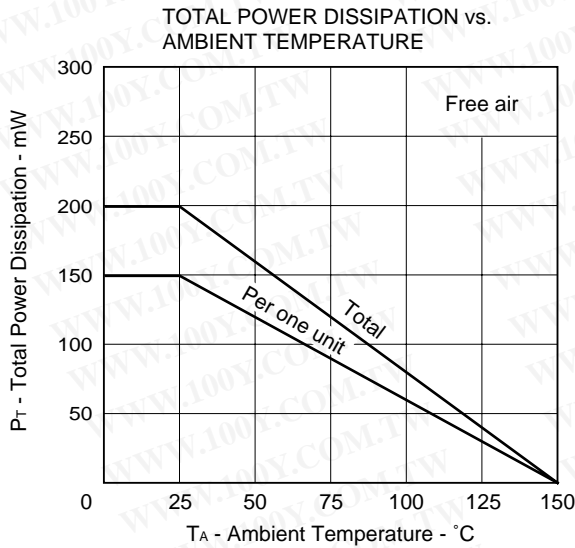
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain Cut-off Current	I_{DSS}	$V_{DS} = 50\text{ V}, V_{GS} = 0$			10	μA
Gate Leakage Current	I_{GSS}	$V_{GS} = \pm 7.0\text{ V}, V_{DS} = 0$			± 5.0	μA
Gate Cut-off Voltage	$V_{GS(off)}$	$V_{DS} = 3.0\text{ V}, I_D = 1.0\ \mu\text{A}$	0.7	1.0	1.5	V
Forward Transfer Admittance	$ y_{fs} $	$V_{DS} = 3.0\text{ V}, I_D = 10\text{ mA}$	20			mS
Drain to Source On-State Resistance	$R_{DS(on)1}$	$V_{GS} = 2.5\text{ V}, I_D = 10\text{ mA}$		20	40	Ω
Drain to Source On-State Resistance	$R_{DS(on)2}$	$V_{GS} = 4.0\text{ V}, I_D = 10\text{ mA}$		15	20	Ω
Input Capacitance	C_{iss}	$V_{DS} = 3.0\text{ V}, V_{GS} = 0, f = 1.0\text{ MHz}$		6		pF
Output Capacitance	C_{oss}			8		pF
Reverse Transfer Capacitance	C_{rss}			1.2		pF
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 3\text{ V}, I_D = 20\text{ mA}, V_{GS(on)} = 3\text{ V}, R_G = 10\ \Omega, R_L = 120\ \Omega$		9		ns
Rise Time	t_r			50		ns
Turn-Off Delay Time	$t_{d(off)}$			20		ns
Fall Time	t_f			40		ns

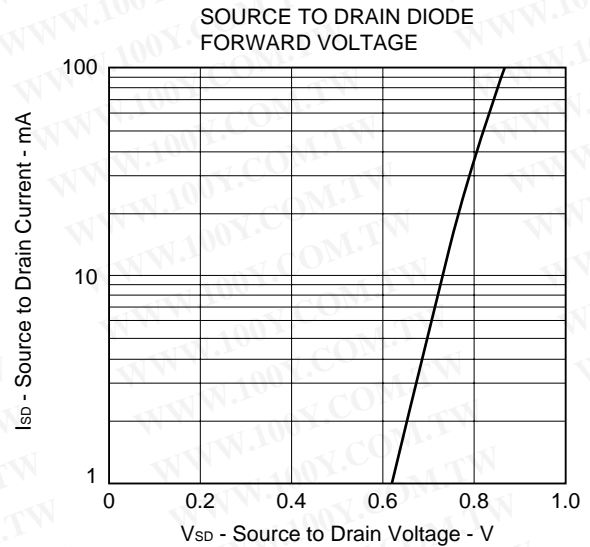
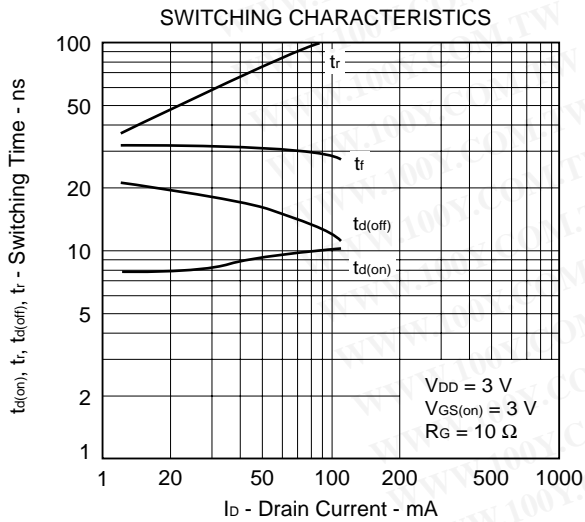
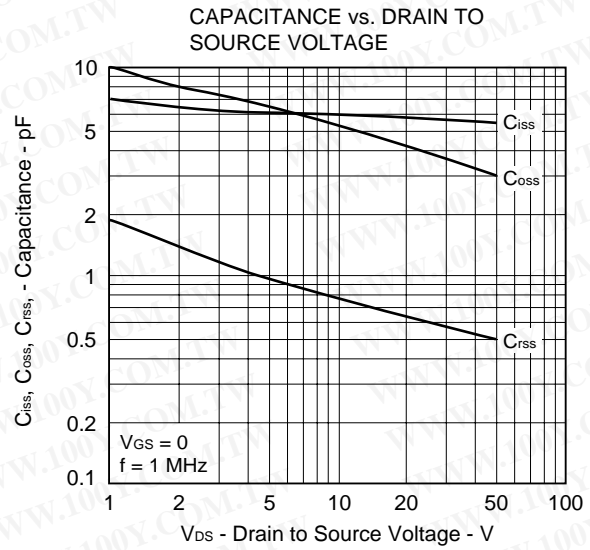
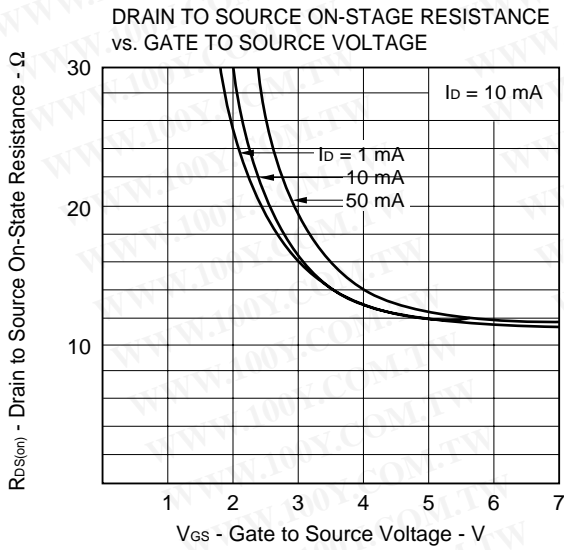
SWITCHING TIME MEASUREMENT CIRCUIT AND CONDITIONS



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TYPICAL CHARACTERISTICS (TA = 25 °C)





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REFERENCE

Document Name	Document No.
NEC semiconductor device reliability/quality control system	TEI-1202
Quality grade on NEC semiconductor devices	IEI-1209
Semiconductor device mounting technology manual	C10535E
Guide to quality assurance for semiconductor devices	MEI-1202
Semiconductor selection guide	X10679E

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Anti-radioactive design is not implemented in this product.