

N-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

BV _{DSS} /	R _{DS(ON)}	I _{D(ON)}	Order Number / Package		
BV _{DGS}	(max)	(min)	TO-92		
240V	6.0Ω	1.0A	VN2406L		
240V	10Ω	1.0A	VN2410L		

Features

- Free from secondary breakdown
- Low power drive requirement
- Ease of paralleling
- □ Low C_{ISS} and fast switching speeds
- Excellent thermal stability
- Integral Source-Drain diode
- □ High input impedance and high gain
- Complementary N- and P-channel devices

Applications

- Motor controls
- Converters
- Amplifiers
- Switches
- Dever supply circuits
- Drivers (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

Absolute Maximum Ratings

Drain-to-Source Voltage	BV _{DSS}
Drain-to-Gate Voltage	BV _{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C
4	

* Distance of 1.6 mm from case for 10 seconds.

Advanced DMOS Technology

These enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Option



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Thermal Characteristics

Package	I _D (continuous)*	htinuous)* I_D (pulsed) Power Dissipation @ $T_C = 25^{\circ}C$		θ _{jc} °C/W					
TO-92	0.9A	5.0A	1.0W	125	170	0.18A	1.7A		

* I_{D} (continuous) is limited by max rated T_{i} .

Electrical Characteristics (@ 25°C unless otherwise specified)

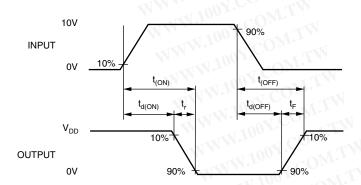
Symbol	Parameter		Min	Тур	Max	Unit	Conditions
BV _{DSS}	Drain-to-Source Breakdown Voltage		240	W	NWN.	00 V.CO	$V_{GS} = 0V, I_D = 0.1mA$
V _{GS(th)}	Gate Threshold Voltage		0.8		2	V	$V_{GS} = V_{DS}, I_D = 1mA$
I _{GSS}	Gate Body Leakage		1.14		100	nA	$V_{GS} = 20V, V_{DS} = 0V$
I _{DSS}	Zero Gate Voltage Drain Current		M.TV		10	W.1001	$V_{GS} = 0V, V_{DS} = 120V$
W.100Y.	COM.TW WWW.100Y.C		OM.T	N N	500	μΑ	$V_{GS} = 0V, V_{DS} = 120V$ $T_A = 125^{\circ}C$
I _{D(ON)}	ON-State Drain Current		1.0	W	1	A	V _{GS} = -10V, V _{DS} = 15V
R _{DS(ON)}	Static Drain-to-Source ON-State Resistance	All	COM	. L	10	Ω	$V_{GS} = 2.5V, I_{D} = 0.1A$
		VN2410	100	U.L.	10		$V_{GS} = 10V, I_{D} = 0.5A$
		VN2406		W.LA	6		$V_{GS} = 10V, I_{D} = 0.5A$
$\Delta R_{DS(ON)}$	Change in R _{DS(ON)} with Temperature		01.0	1.0	1.4	%/°C	V _{GS} = 10V, I _D = 0.55A
G _{FS}	Forward Transconductance		300	T.Mo		თთ	$V_{DS} = 10V, I_{D} = 0.5A$
C _{ISS}	Input Capacitance		100%		125	pF	V _{GS} = 0V, V _{DS} = 25V f = 1 MHz
C _{oss}	Common Source Output Capacitance		Yon	COL	50		
C _{RSS}	Reverse Transfer Capacitance		N.12	V.COM	20		
t _{d(ON)}	Turn-ON Delay Time		1.10	V.CO	8	ns	$V_{DD} = 60V$ $I_D = 0.4A$ $R_{GEN} = 25\Omega$
t _r	Rise Time		NN.IO	N.CC	8		
t _{d(OFF)}	Turn-OFF Delay Time		L.WW.1	10 ×	23		
t _f	Fall Time		W	1001.	24		
V _{SD}	Diode Forward Voltage Drop VN2410 VN2406			1.2	COM	V	V _{GS} = 0V, I _{SD} = 0.19A
			A.M.	1.2		V	$V_{GS} = 0V, I_{SD} = 0.8A$

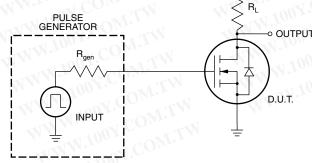
Notes:

1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)

2. All A.C. parameters sample tested.

Switching Waveforms and Test Circuit





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