

勝特力材料 886-3-5753170  
 勝特力电子(上海) 86-21-34970699  
 勝特力电子(深圳) 86-755-83298787  
 Http://www.100y.com.tw

**FAIRCHILD**  
 SEMICONDUCTOR™

September 1983  
 Revised July 2003

## MM74HC154 4-to-16 Line Decoder

### General Description

The MM74HC154 decoder utilizes advanced silicon-gate CMOS technology, and is well suited to memory address decoding or data routing applications. It possesses high noise immunity, and low power consumption of CMOS with speeds similar to low power Schottky TTL circuits.

The MM74HC154 have 4 binary select inputs (A, B, C, and D). If the device is enabled these inputs determine which one of the 16 normally HIGH outputs will go LOW. Two active LOW enables (G1 and G2) are provided to ease cascading of decoders with little or no external logic.

Each output can drive 10 low power Schottky TTL equivalent loads, and is functionally and pin equivalent to the 74LS154. All inputs are protected from damage due to static discharge by diodes to  $V_{CC}$  and ground.

### Features

- Typical propagation delay: 21 ns
- Power supply quiescent current: 80  $\mu$ A
- Wide power supply voltage range: 2–6V
- Low input current: 1  $\mu$ A maximum

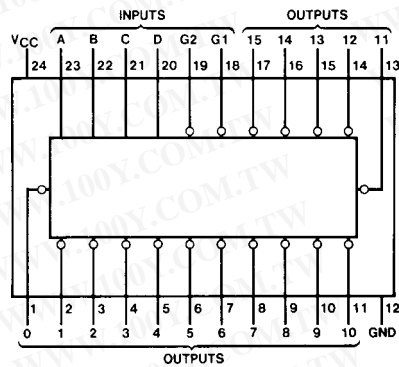
### Ordering Code:

Order Number	Package Number	Package Description
MM74HC154WM	M24B	24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
MM74HC154MTC	MTC24	24-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HC154N	N24C	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

### Connection Diagram

Pin Assignments for DIP, SOIC and TSSOP



### Truth Table

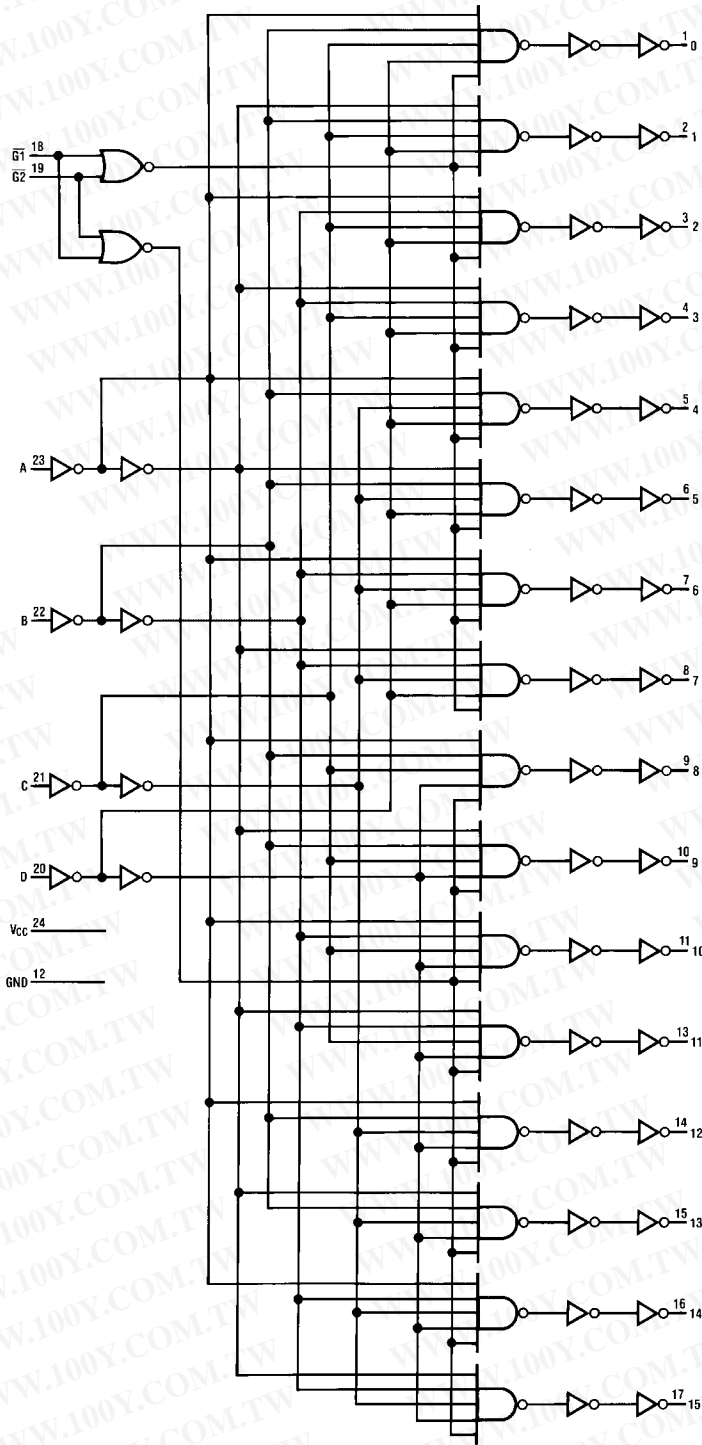
		Inputs				Low Output (Note 1)
$\overline{G1}$	$\overline{G2}$	D	C	B	A	
L	L	L	L	L	L	0
L	L	L	L	L	H	1
L	L	L	L	H	L	2
L	L	L	L	H	H	3
L	L	L	H	L	L	4
L	L	L	H	L	H	5
L	L	L	H	H	L	6
L	L	L	H	H	H	7
L	L	H	L	L	L	8
L	L	H	L	L	H	9
L	L	H	L	H	L	10
L	L	H	L	H	H	11
L	L	H	H	L	L	12
L	L	H	H	L	H	13
L	L	H	H	H	L	14
L	L	H	H	H	H	15
L	H	X	X	X	X	—
H	L	X	X	X	X	—
H	H	X	X	X	X	—

Note 1: All others HIGH

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### Logic Diagram



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**Absolute Maximum Ratings**(Note 2)

(Note 3)

Supply Voltage ( $V_{CC}$ )	-0.5 to +7.0V
DC Input Voltage ( $V_{IN}$ )	-1.5 to $V_{CC} + 1.5V$
DC Output Voltage ( $V_{OUT}$ )	-0.5 to $V_{CC} + 0.5V$
Clamp Diode Current ( $I_{IK}, I_{OK}$ )	$\pm 20$ mA
DC Output Current, per pin ( $I_{OUT}$ )	$\pm 25$ mA
DC $V_{CC}$ or GND Current, per pin ( $I_{CC}$ )	$\pm 50$ mA
Storage Temperature Range ( $T_{STG}$ )	-65°C to +150°C
Power Dissipation ( $P_D$ )	
(Note 4)	600 mW
S.O. Package only	500 mW
Lead Temperature ( $T_L$ )	
(Soldering 10 seconds)	260°C

**Recommended Operating Conditions**

	Min	Max	Units
Supply Voltage ( $V_{CC}$ )	2	6	V
DC Input or Output Voltage ( $V_{IN}, V_{OUT}$ )	0	$V_{CC}$	V
Operating Temperature Range ( $T_A$ )	-40	+85	°C
Input Rise or Fall Times			
( $t_r, t_f$ ) $V_{CC} = 2.0V$		1000	ns
$V_{CC} = 4.5V$		500	ns
$V_{CC} = 6.0V$		400	ns

**Note 2:** Absolute Maximum Ratings are those values beyond which damage to the device may occur.**Note 3:** Unless otherwise specified all voltages are referenced to ground.**Note 4:** Power Dissipation temperature derating — plastic "N" package: -12 mW/°C from 65°C to 85°C.**DC Electrical Characteristics** (Note 5)

Symbol	Parameter	Conditions	$V_{CC}$	$T_A = 25^\circ C$		$T_A = -40$ to $85^\circ C$		Units
				Typ	Guaranteed Limits			
$V_{IH}$	Minimum HIGH Level Input Voltage		2.0V		1.5	1.5	V	
			4.5V		3.15	3.15		
			6.0V		4.2	4.2		
$V_{IL}$	Maximum LOW Level Input Voltage		2.0V		0.5	0.5	V	
			4.5V		1.35	1.35		
			6.0V		1.8	1.8		
$V_{OH}$	Minimum HIGH Level Output Voltage	$V_{IN} = V_{IH}$ or $V_{IL}$ $I_{OUT} \leq 20 \mu A$	2.0V	2.0	1.9	1.9	V	
			4.5V	4.5	4.4	4.4		
			6.0V	6.0	5.9	5.9		
		$V_{IN} = V_{IH}$ or $V_{IL}$ $I_{OUT} \leq 4.0$ mA $I_{OUT} \leq 5.2$ mA	4.5V	4.2	3.98	3.84	V	
			6.0V	5.7	5.48	5.34		
$V_{OL}$	Maximum LOW Level Output Voltage	$V_{IN} = V_{IH}$ or $V_{IL}$ $I_{OUT} \leq 20 \mu A$	2.0V	0	0.1	0.1	V	
			4.5V	0	0.1	0.1		
			6.0V	0	0.1	0.1		
		$V_{IN} = V_{IH}$ or $V_{IL}$ $I_{OUT} \leq 4.0$ mA $I_{OUT} \leq 5.2$ mA	4.5V	0.2	0.26	0.33	V	
			6.0V	0.2	0.26	0.33		
$I_{IN}$	Maximum Input Current	$V_{IN} = V_{CC}$ or GND	6.0V		$\pm 0.1$	$\pm 1.0$	$\mu A$	
$I_{CC}$	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND $I_{OUT} = 0 \mu A$	6.0V		8.0	80	$\mu A$	

**Note 5:** For a power supply of 5V  $\pm 10\%$  the worst case output voltages ( $V_{OH}$ , and  $V_{OL}$ ) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case  $V_{IH}$  and  $V_{IL}$  occur at  $V_{CC} = 5.5V$  and 4.5V respectively. (The  $V_{IH}$  value at 5.5V is 3.85V.) The worst case leakage current ( $I_{IN}$ ,  $I_{CC}$ , and  $I_{OZ}$ ) occur for CMOS at the higher voltage and so the 6.0V values should be used.

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**AC Electrical Characteristics** $V_{CC} = 5V$ ,  $T_A = 25^\circ C$ ,  $C_L = 15 \text{ pF}$ ,  $t_r = t_f = 6 \text{ ns}$ 

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
$t_{PHL}$ , $t_{PLH}$	Maximum Propagation Delay, $\overline{G1}$ , $\overline{G2}$ or A, B, C, D		21	32	ns

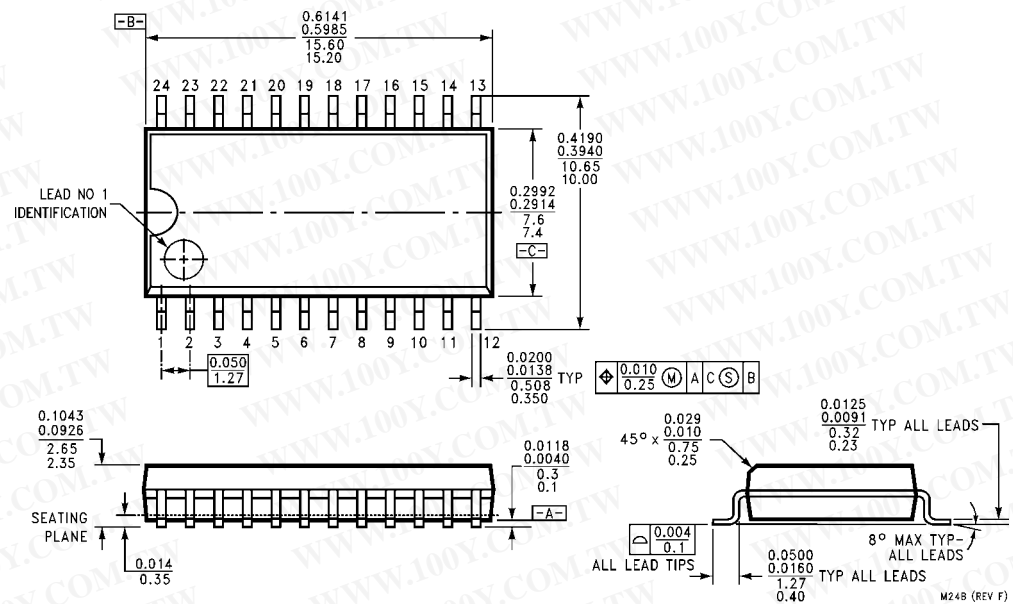
**AC Electrical Characteristics** $V_{CC} = 2.0V$  to  $6.0V$ ,  $C_L = 50 \text{ pF}$ ,  $t_r = t_f = 6 \text{ ns}$  (unless otherwise specified)

Symbol	Parameter	Conditions	$V_{CC}$	$T_A = 25^\circ C$		$T_A = -40 \text{ to } 85^\circ C$		Units
				Typ	Guaranteed Limits	Typ	Guaranteed Limits	
$t_{PHL}$ , $t_{PLH}$	Maximum Propagation Delay, $\overline{G1}$ or $\overline{G2}$ or A, B, C, D		2.0V	63	160	190	ns	
			4.5V	24	36	42		
			6.0V	20	30	35		
$t_{TLH}$ , $t_{THL}$	Maximum Output Rise and Fall Time		2.0V	25	75	95	ns	
			4.5V	7	15	19		
			6.0V	6	13	16		
$C_{PD}$	Power Dissipation Capacitance (Note 6)			90			pF	
$C_{IN}$	Maximum Input Capacitance			5	10	10	pF	

**Note 6:**  $C_{PD}$  determines the no load dynamic power consumption,  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ , and the no load dynamic current consumption,  $I_S = C_{PD} V_{CC} f + I_{CC}$ .

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**Physical Dimensions** inches (millimeters) unless otherwise noted

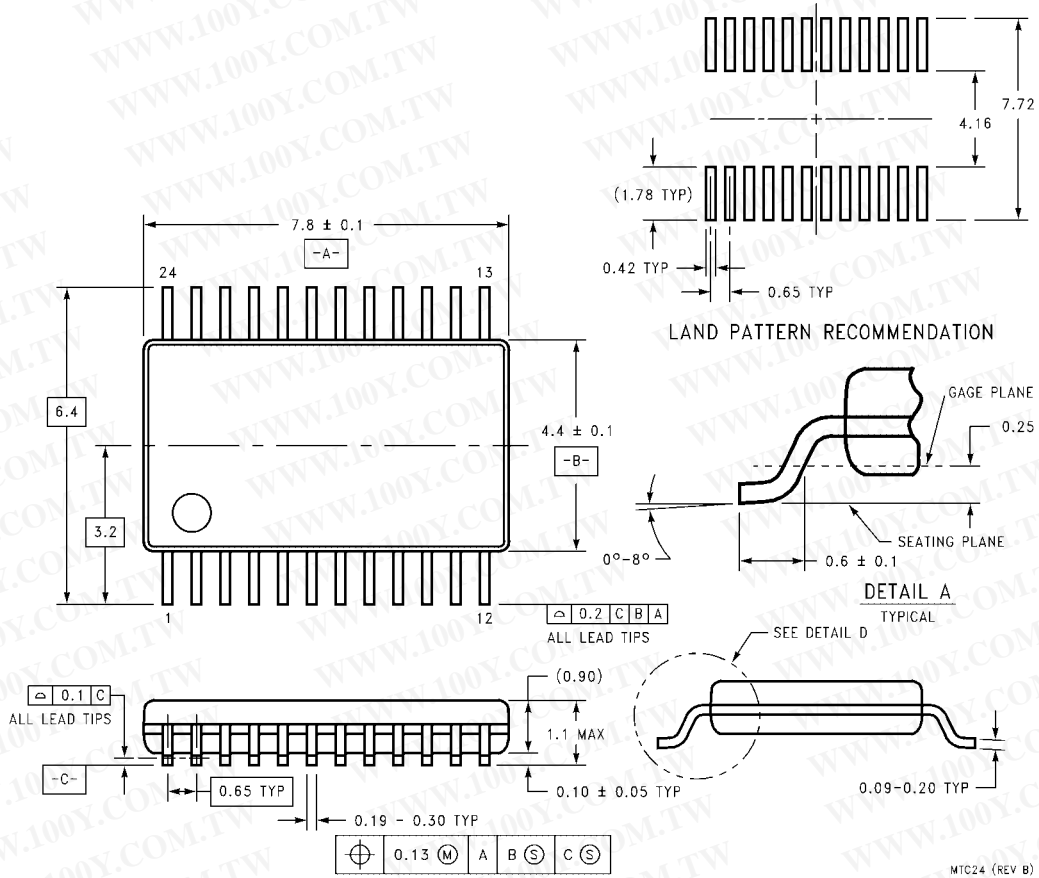


24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide  
Package Number M24B

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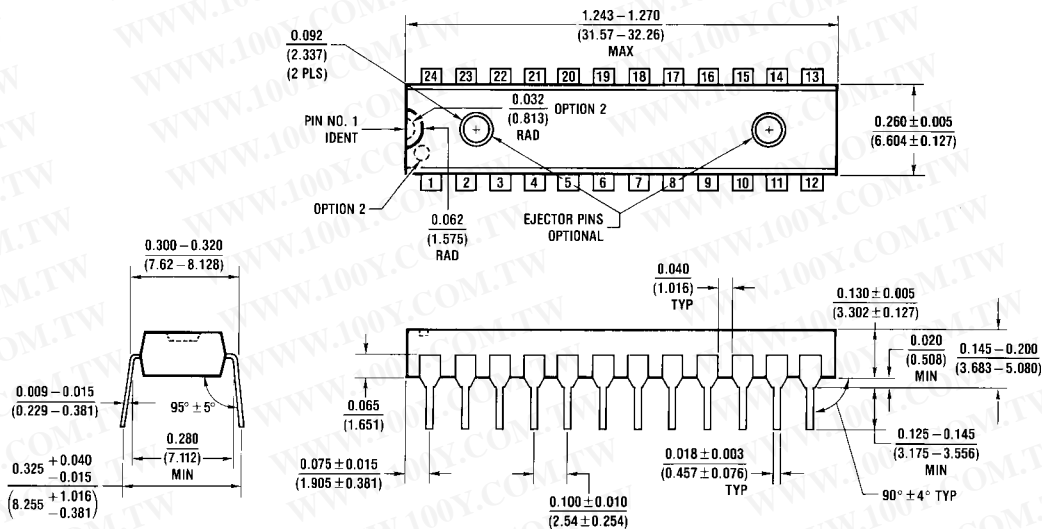
**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



24-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide  
Package Number MTC24

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**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide  
Package Number N24C

N24C (REV F)

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