

# HD74LS257 • Quadruple 2-line-to-1-line Data Selectors/Multiplexers (with non inverted 3-state outputs)

This multiplexer features three-state outputs that can interface directly with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at a high-impedance state) the low impedance of the single enabled output will drive the bus line to a high or low logic level.

To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output-enable circuitry is designed such that the output disable times are shorter than the output enable times.

## ■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Ratings	Unit
Supply voltage	$V_{CC}$	7.0	V
Input voltage	$V_{IN}$	7.0	V
Output voltage (off-state)	$V_{O(off)}$	5.5	V
Operating temperature range	$T_{opr}$	-20 ~ +75	°C
Storage temperature range	$T_{stg}$	-65 ~ +150	°C

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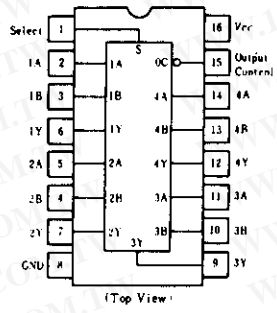
## ■ ELECTRICAL CHARACTERISTICS ( $T_a = -20 \sim +75^\circ\text{C}$ )

Item		Symbol	Test Conditions	min	typ*	max	Unit	
Input voltage		$V_{IH}$		2.0	—	—	V	
		$V_{IL}$		—	—	0.8	V	
Output voltage		$V_{OH}$	$V_{CC}=4.75\text{V}, V_{IH}=2\text{V}, V_{IL}=0.8\text{V}, I_{OH}=-2.6\text{mA}$	2.4	—	—	V	
		$V_{OL}$	$V_{CC}=4.75\text{V}, V_{IH}=2\text{V}, V_{IL}=0.8\text{V}$	$I_{OL}=8\text{mA}$	—	—	0.5	V
				$I_{OL}=4\text{mA}$	—	—	0.4	
Input current	S	$I_{IH}$	$V_{CC}=5.25\text{V}, V_I=2.7\text{V}$	—	—	40	$\mu\text{A}$	
	S except			—	—	20		
	S	$I_{IL}$	$V_{CC}=5.25\text{V}, V_I=0.4\text{V}$	—	—	-0.8	mA	
	S except			—	—	-0.4		
	S	$I_I$	$V_{CC}=5.25\text{V}, V_I=7\text{V}$	—	—	0.2	mA	
S except	—			—	0.1			
Output current		$I_{OZ}$	$V_{CC}=5.25\text{V}, V_{IH}=2\text{V}$	$V_O=2.4\text{V}$	—	—	20	$\mu\text{A}$
				$V_O=0.4\text{V}$	—	—	-20	
Short-circuit output current		$I_{OS}$	$V_{CC}=5.25\text{V}$	-30	—	-130	mA	
Supply current**	All outputs high	$I_{CC}$	$V_{CC}=5.25\text{V}$	—	5.9	10	mA	
	All outputs low			—	9.2	16		
	All outputs off			—	10	19		
Input clamp voltage		$V_{IK}$	$V_{CC}=4.75\text{V}, I_{IN}=-18\text{mA}$	—	—	-1.5	V	

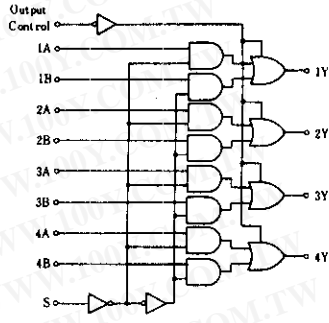
\*  $V_{CC}=5\text{V}, T_a=25^\circ\text{C}$

\*\*  $I_{CC}$  is measured with all outputs open and all possible inputs grounded while achieving the stated output conditions.

## ■ PIN ARRANGEMENT



## ■ BLOCK DIAGRAM



## ■ FUNCTION TABLE

OC	Inputs			Outputs
	S	A	B	
H	X	X	X	Z
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

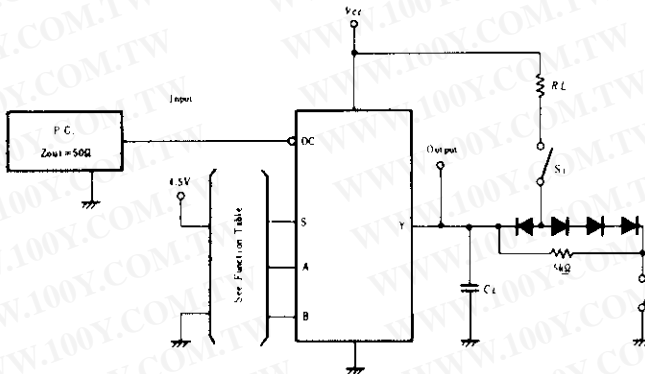
Note) H; high level, L; low level, X; irrelevant  
Z; off (high-impedance) state of a 3-state output

## SWITCHING CHARACTERISTICS ( $V_{CC}=5V, T_a=25^{\circ}C$ )

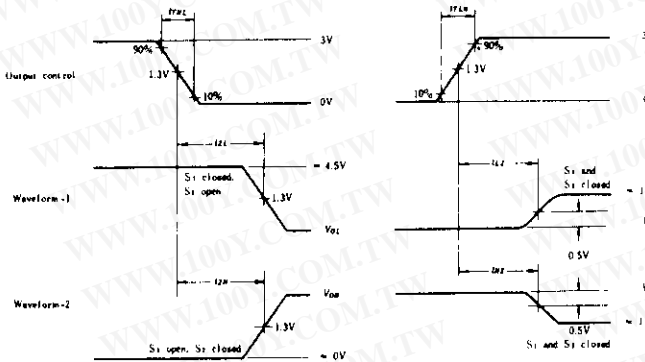
Item	Inputs	Output	Symbol	Test Conditions	min	typ	max	Unit
Propagation delay time	A, B	Y	$t_{PLH}$	$R_L = 2k\Omega$ $C_L = 15pF$	—	12	18	ns
			$t_{PHL}$		—	12	18	
	S	Y	$t_{PLH}$		—	14	21	ns
			$t_{PHL}$		—	14	21	
Output enable time	OC	Y	$t_{ZH}$	$R_L = 2k\Omega$ $C_L = 5pF$	—	20	30	ns
			$t_{ZL}$		—	20	30	
Output disable time	OC	Y	$t_{HZ}$	$R_L = 2k\Omega$ $C_L = 5pF$	—	18	30	ns
			$t_{LZ}$		—	16	25	

## TESTING METHOD

### 1) Test Circuit

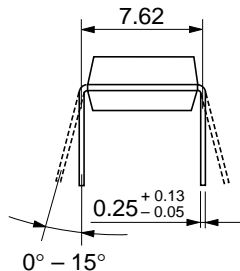
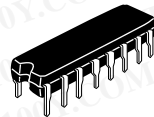
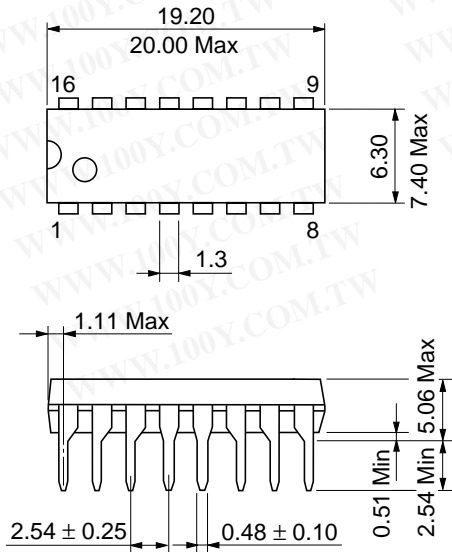


### Waveform



- Notes)
- Input pulse:  $t_{PLH} \leq 15ns, t_{PHL} \leq 6ns, PRR=1MHz,$  duty cycle = 50%.
  - $C_L$  includes probe and jig capacitance.
  - All diodes are 1S2074  $\oplus$ .
  - Waveform-1 is for an output with internal conditions such that the output is low except when disabled by the output control.
  - Waveform-2 is for an output with internal conditions such that the output is high except when disabled by the output control.

Unit: mm

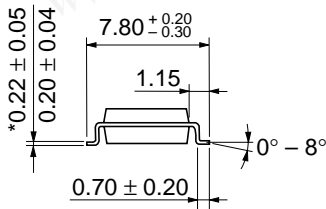
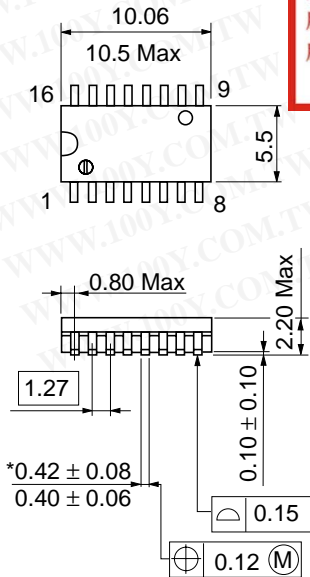
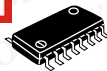


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Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	1.07 g

Unit: mm

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\*Dimension including the plating thickness  
 Base material dimension

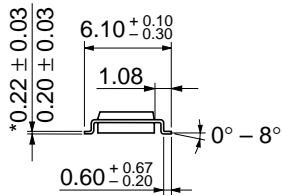
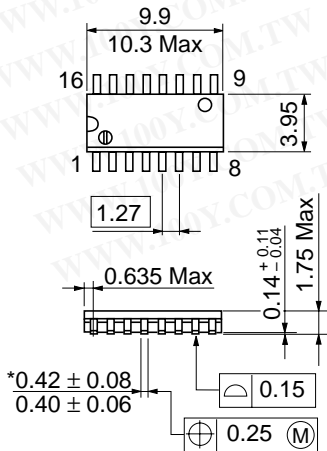
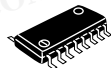
Hitachi Code	FP-16DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.24 g

Unit: mm

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\*Dimension including the plating thickness  
Base material dimension

Hitachi Code	FP-16DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.15 g

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