



February 1984
Revised February 1999

MM74HC4020 • MM74HC4040

14-Stage Binary Counter • 12-Stage Binary Counter

General Description

The MM74HC4020, MM74HC4040, are high speed binary ripple carry counters. These counters are implemented utilizing advanced silicon-gate CMOS technology to achieve speed performance similar to LS-TTL logic while retaining the low power and high noise immunity of CMOS.

The MM74HC4020 is a 14 stage counter and the MM74HC4040 is a 12-stage counter. Both devices are incremented on the falling edge (negative transition) of the input clock, and all their outputs are reset to a low level by applying a logical high on their reset input.

These devices are pin equivalent to the CD4020 and CD4040 respectively. All inputs are protected from damage due to static discharge by protection diodes to V_{CC} and ground.

Features

- Typical propagation delay: 16 ns
- Wide operating voltage range: 2–6V
- Low input current: 1 μ A maximum
- Low quiescent current: 80 μ A maximum (74HC Series)
- Output drive capability: 10 LS-TTL loads

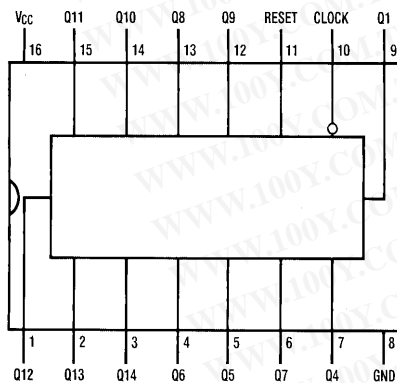
Ordering Code:

| Order Number | Package Number | Package Description |
|---------------|----------------|--|
| MM74HC4020M | M16A | 16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow |
| MM74HC4020SJ | M16D | 16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide |
| MM74HC4020MTC | MTC16 | 16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide |
| MM74HC4020N | N16E | 16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide |
| MM74HC4040M | M16A | 16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow |
| MM74HC4040SJ | M16D | 16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide |
| MM74HC4040MTC | MTC16 | 16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide |
| MM74HC4040N | N16E | 16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide |

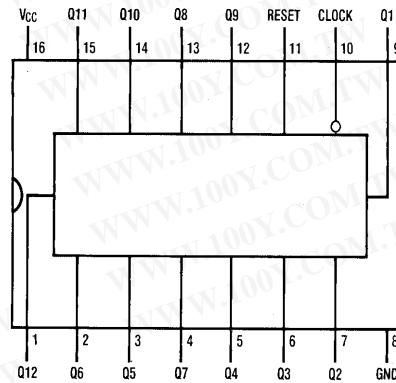
Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagrams

Pin Assignments for DIP, SOIC, SOP and TSSOP



TOP VIEW
MM74HC4020

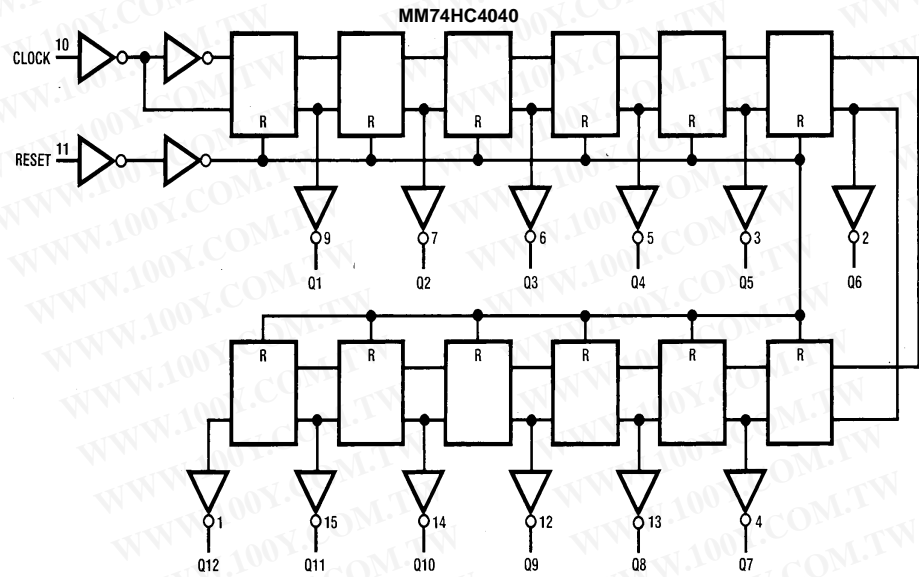
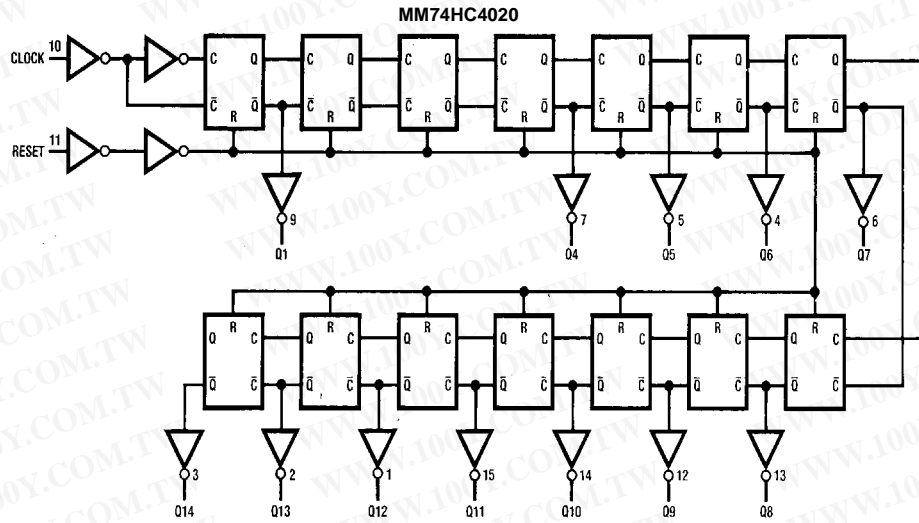


TOP VIEW
MM74HC4040

MM74HC4020 • MM74HC4040 14-Stage Binary Counter • 12-Stage Binary Counter

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Logic Diagrams



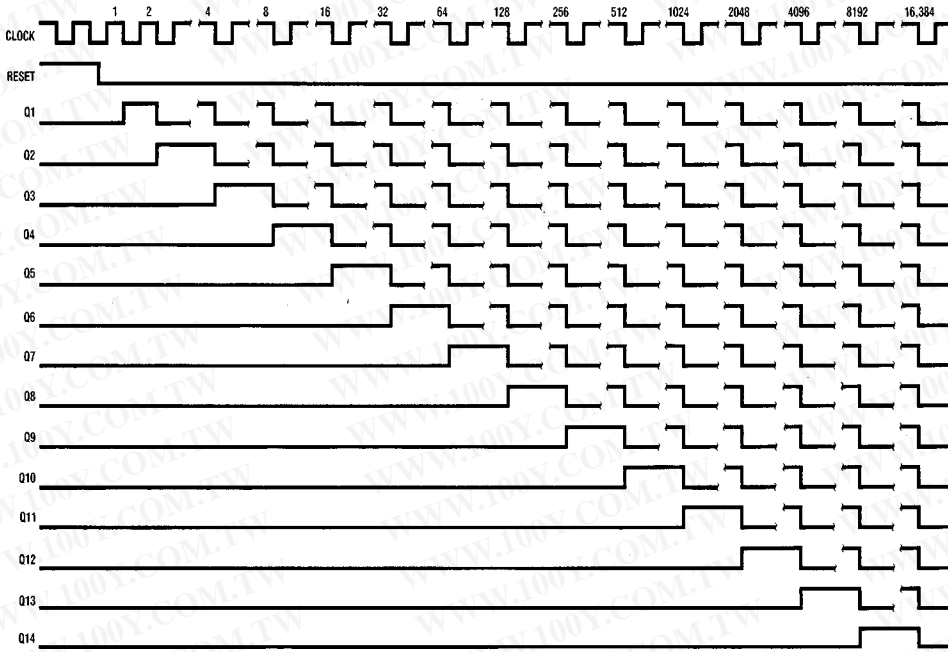
| Absolute Maximum Ratings (Note 1) | | | | Recommended Operating Conditions | | | | |
|---|-----------------------------------|--|---|----------------------------------|-------------------|------------|--------------|----|
| (Note 2) | | | | | Min | Max | Units | |
| Supply Voltage (V _{CC}) | | -0.5 to +7.0V | | 2 | 6 | V | | |
| DC Input Voltage (V _{IN}) | | -1.5 to V _{CC} +1.5V | Supply Voltage (V _{CC}) | 0 | V _{CC} | V | | |
| DC Output Voltage (V _{OUT}) | | -0.5 to V _{CC} +0.5V | DC Input or Output Voltage (V _{IN} , V _{OUT}) | | | | | |
| Clamp Diode Current (I _{CD}) | | ±20 mA | Operating Temperature Range (T _A) | -40 | +85 | °C | | |
| DC Output Current, per pin (I _{OUT}) | | ±25 mA | Input Rise or Fall Times (t _r , t _f) | | | | | |
| DC V _{CC} or GND Current, per pin (I _{CC}) | | ±50 mA | V _{CC} = 2.0V | | 1000 | ns | | |
| Storage Temperature Range (T _{STG}) | | -65°C to +150°C | V _{CC} = 4.5V | | 500 | ns | | |
| Power Dissipation (P _D) | | | V _{CC} = 6.0V | | 400 | ns | | |
| (Note 3) | | 600 mW | Note 1: Maximum Ratings are those values beyond which damage to the device may occur. | | | | | |
| S.O. Package only | | 500 mW | Note 2: Unless otherwise specified all voltages are referenced to ground. | | | | | |
| Lead Temperature (T _L) | | | Note 3: Power Dissipation temperature derating — plastic "N" package: -12 mW/°C from 65°C to 85°C. | | | | | |
| (Soldering 10 seconds) | | 260°C | | | | | | |
| DC Electrical Characteristics (Note 4) | | | | | | | | |
| Symbol | Parameter | Conditions | V _{CC} | T _A = 25°C | | | Units | |
| | | | | Typ | Guaranteed Limits | | | |
| V _{IH} | Minimum HIGH Level Input Voltage | | 2.0V | 1.5 | 1.5 | 1.5 | V | |
| | | | 4.5V | 3.15 | 3.15 | 3.15 | V | |
| | | | 6.0V | 4.2 | 4.2 | 4.2 | V | |
| V _{IL} | Maximum LOW Level Input Voltage | | 2.0V | 0.5 | 0.5 | 0.5 | V | |
| | | | 4.5V | 1.35 | 1.35 | 1.35 | V | |
| | | | 6.0V | 1.8 | 1.8 | 1.8 | V | |
| V _{OH} | Minimum HIGH Level Output Voltage | V _{IN} = V _{IH} or V _{IL} I _{OUT} ≤ 20 μA | 2.0V | 2.0 | 1.9 | 1.9 | V | |
| | | | 4.5V | 4.5 | 4.4 | 4.4 | V | |
| | | | 6.0V | 6.0 | 5.9 | 5.9 | V | |
| | | V _{IN} = V _{IH} or V _{IL} I _{OUT} ≤ 4.0 mA I _{OUT} ≤ 5.2 mA | 4.5V | 4.2 | 3.98 | 3.84 | 3.7 | V |
| | | | 6.0V | 5.7 | 5.48 | 5.34 | 5.2 | V |
| | | | | | | | | |
| V _{OL} | Maximum LOW Level Output Voltage | V _{IN} = V _{IH} or V _{IL} I _{OUT} ≤ 20 μA | 2.0V | 0 | 0.1 | 0.1 | V | |
| | | | 4.5V | 0 | 0.1 | 0.1 | V | |
| | | | 6.0V | 0 | 0.1 | 0.1 | V | |
| | | V _{IN} = V _{IH} or V _{IL} I _{OUT} ≤ 4.0 mA I _{OUT} ≤ 5.2 mA | 4.5V | 0.2 | .26 | 0.33 | 0.4 | V |
| | | | 6.0V | 0.2 | .26 | 0.33 | 0.4 | V |
| | | | | | | | | |
| I _{IN} | Maximum Input Current | V _{IN} = V _{CC} or GND | 6.0V | | ±0.1 | ±1.0 | ±1.0 | μA |
| I _{CC} | Maximum Quiescent Supply Current | V _{IN} = V _{CC} or GND I _{OUT} = 0 μA | 6.0V | | 8.0 | 80 | 160 | μA |
| Note 4: For a power supply of 5V ±10% the worst case output voltages (V _{OH} and V _{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V _{IH} and V _{IL} occur at V _{CC} = 5.5V and 4.5V respectively. (The V _{IH} value at 5.5V is 3.85V.) The worst case leakage current (I _{IN} , I _{CC} , and I _{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used. | | | | | | | | |

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| AC Electrical Characteristics | | | | | | | | | | |
|---|--|---------------|----------|--------------------|-------------------|-----------------------------|------|------------------------------|-----|-------|
| $V_{CC} = 5V, T_A = 25^\circ C, C_L = 15 pF, t_r = t_f = 6 ns$ | | | | | | | | | | |
| Symbol | Parameter | Conditions | Typ | Guaranteed Limit | Units | | | | | |
| f_{MAX} | Maximum Operating Frequency | | 50 | 30 | MHz | | | | | |
| t_{PHL}, t_{PLH} | Maximum Propagation Delay Clock to Q | (Note 5) | 17 | 35 | ns | | | | | |
| t_{PHL} | Maximum Propagation Delay Reset to any Q | | 16 | 40 | ns | | | | | |
| t_{REM} | Minimum Reset Removal Time | | 10 | 20 | ns | | | | | |
| t_W | Minimum Pulse Width | | 10 | 16 | ns | | | | | |
| <p>Note 5: Typical Propagation delay time to any output can be calculated using: $t_p = 17 + 12(N-1)$ ns; where N is the number of the output, Q_{Wp}, at $V_{CC} = 5V$.</p> | | | | | | | | | | |
| AC Electrical Characteristics | | | | | | | | | | |
| $V_{CC} = 2.0V$ to $6.0V, C_L = 50 pF, t_r = t_f = 6 ns$ (unless otherwise specified) | | | | | | | | | | |
| Symbol | Parameter | Conditions | V_{CC} | $T_A = 25^\circ C$ | | $T_A = -40$ to $85^\circ C$ | | $T_A = -55$ to $125^\circ C$ | | Units |
| | | | | Typ | Guaranteed Limits | | | | | |
| f_{MAX} | Maximum Operating Frequency | | 2.0V | 10 | 6 | 5 | 4 | | MHz | |
| | | | 4.5V | 40 | 30 | 24 | 20 | | MHz | |
| | | | 6.0V | 50 | 35 | 28 | 24 | | MHz | |
| t_{PHL}, t_{PLH} | Maximum Propagation Delay Clock to Q_1 | | 2.0V | 80 | 210 | 265 | 313 | | ns | |
| | | | 4.5V | 21 | 42 | 53 | 63 | | ns | |
| | | | 6.0V | 18 | 36 | 45 | 53 | | ns | |
| T_{PHL}, t_{PLH} | Maximum Propagation Delay Between Stages from Q_n to Q_{n+1} | | 2.0V | 80 | 125 | 156 | 188 | | ns | |
| | | | 4.5V | 18 | 25 | 31 | 38 | | ns | |
| | | | 6.0V | 15 | 21 | 26 | 31 | | ns | |
| t_{PHL} | Maximum Propagation Delay Reset to any Q (4020 and 4040) | | 2.0V | 72 | 240 | 302 | 358 | | ns | |
| | | | 4.5V | 24 | 48 | 60 | 72 | | ns | |
| | | | 6.0V | 20 | 41 | 51 | 61 | | ns | |
| t_{REM} | Minimum Reset Removal Time | | 2.0V | | 100 | 126 | 149 | | ns | |
| | | | 4.5V | | 20 | 25 | 50 | | ns | |
| | | | 6.0V | | 16 | 21 | 25 | | ns | |
| t_W | Minimum Pulse Width | | 2.0V | | 90 | 100 | 120 | | ns | |
| | | | 4.5V | | 16 | 20 | 24 | | ns | |
| | | | 6.0V | | 14 | 18 | 20 | | ns | |
| t_{TLH}, t_{THL} | Maximum Output Rise and Fall Time | | 2.0V | 30 | 75 | 95 | 110 | | ns | |
| | | | 4.5V | 10 | 15 | 19 | 22 | | ns | |
| | | | 6.0V | 9 | 13 | 16 | 19 | | ns | |
| t_r, t_f | Maximum Input Rise and Fall Time | | | | 1000 | 1000 | 1000 | | ns | |
| | | | | | 500 | 500 | 500 | | ns | |
| | | | | | 400 | 400 | 400 | | ns | |
| C_{PD} | Power Dissipation Capacitance (Note 6) | (per package) | | 55 | | | | | pF | |
| C_{IN} | Maximum Input Capacitance | | | 5 | 10 | 10 | 10 | | pF | |
| <p>Note 6: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.</p> | | | | | | | | | | |

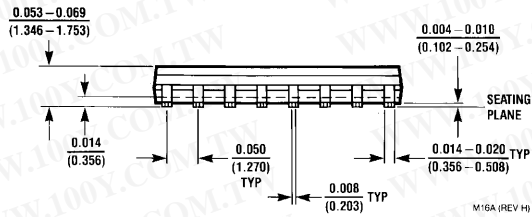
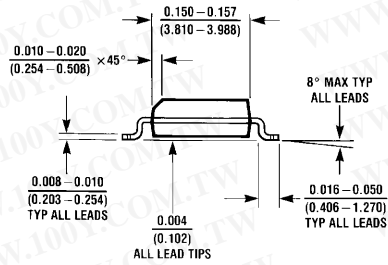
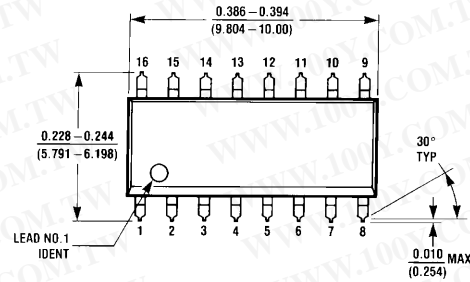
Timing Diagram



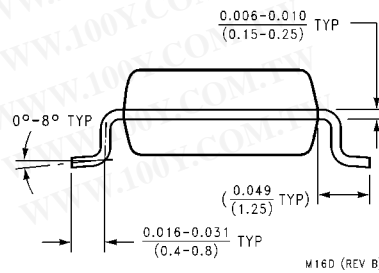
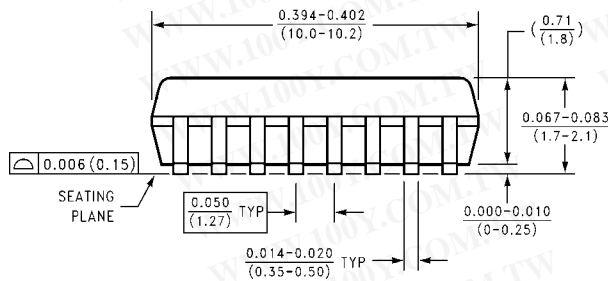
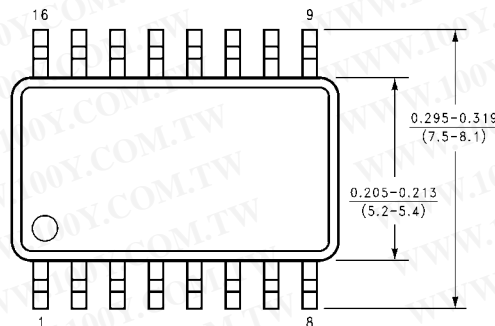
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Physical Dimensions inches (millimeters) unless otherwise noted



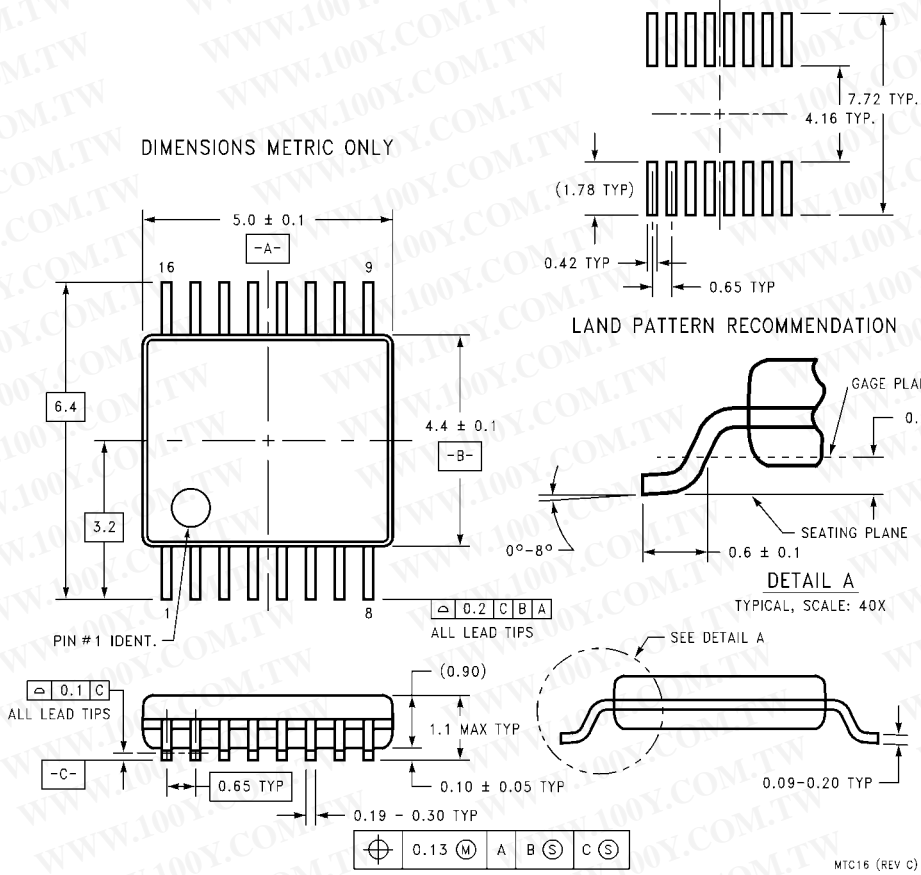
16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Package Number M16A



16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide Package Number M16D

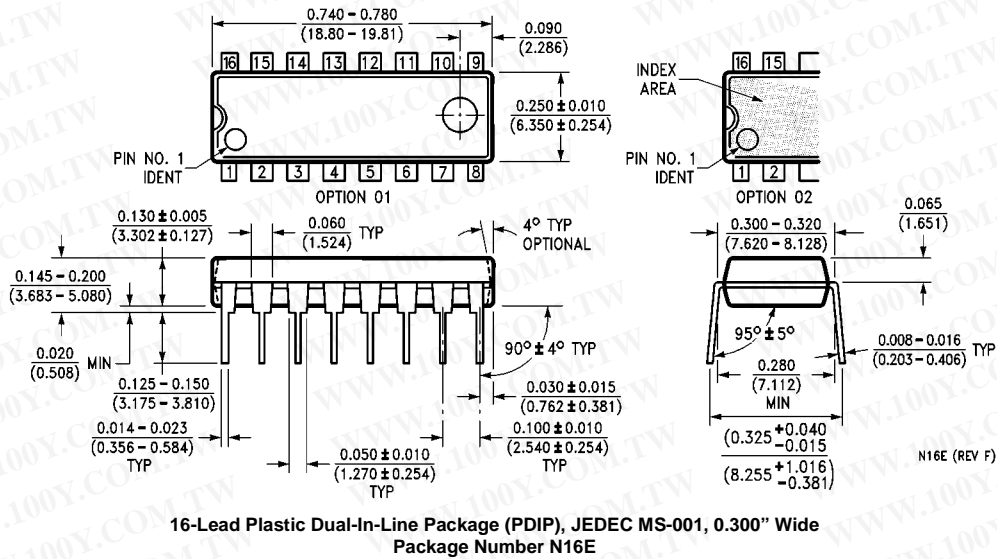
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Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



**16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC16**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



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